An Interface Circuit for Low-Voltage Low-Current Energy Harvesting Systems

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***Abstract*—In this paper we present an interface circuit designed to match low-power and low-voltage harvesters to generic electronic loads. The interface circuit consists of a power management unit, a supply regulation unit, and an energy storage module. The electric power delivered by the harvester is stored in a low leakage capacitor, converted to match the load electrical characteristics, and used cyclically to supply the load during fixed time-windows. The interface circuit is compatible with DC harvesters with a current of at least 2 μA at 0.5 V and exhibits an efficiency of 65% in the 1 μW−1 mW range. The supply regulation unit is a two-stage, self-starting boost circuit that steps-up the 0.5 V input voltage to 3 V. To test the interface circuit, an autonomous wireless sensor node has been realized; it exploits the little electric power delivered by a 385 μm × 245 μm photovoltaic harvester to sense and transmit information about the environment wirelessly. The harvester is implemented with a custom 0.35-μm BCD SOI chip. The system has been designed to be low-cost, fully autonomous and smaller of 9 cm^3.**

***Index Terms*—Energy harvesting, ultra-low-power, low-voltage, battery-less, wireless sensor network.**

I. Introduction

THE miniaturization and the power consumption down-scaling of electronic equipment has recently pushed the research to find alternative power supply for circuits. In this context, energy harvesting techniques represent a promising answer to the always larger demand for portability and battery-independence of electronic devices [1]–[6]. Fig. 1 shows the general block diagram of an energy harvesting system. An interface circuitry matches the harvester (i.e. the input) to the load (i.e. the output), ensuring the correct operation of the system.

Fig. 2 compares several energy harvesting systems that have been presented recently. All of them are characterized by an input power in the 1 μW−1 mW range. Each solution has been evaluated in terms of the minimum acceptable supply voltage and the minimum acceptable current that a generic harvester must deliver to allow the system to work properly. A first group of papers [7]–[9] considers harvesters that can deliver a very low current but at high input voltages (from 1.4 V to 3 V). In this case, the minimum supply voltage constraint for the load circuit is often intrinsically satisfied. Hence, the interface circuit is only asked to accumulate energy in order to sustain the operation of the load with a sufficient current.

A second group of papers [10]–[13] considers harvesters that can deliver a high current but at low input voltages (from 20 mV to 300 mV). In particular in [10]–[12] the harvester is organic, a Microbial Fuel Cell (MFC), while [13] exploits a Thermo-Electric Generator (TEG). This kind of harvesters cannot directly supply the load because their generated voltage is below the load requirements; on the contrary, the energy storage is tipically not necessary because enough current is available directly from the source. Hence, the main interface circuit function is voltage conversion and regulation.

The aim of this work is to design and implement an interface

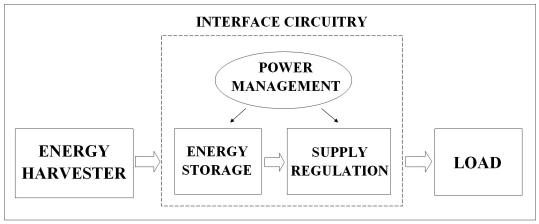

Fig. 1. Generic energy harvesting system

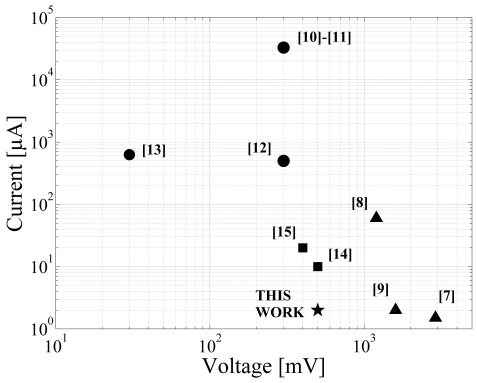

Fig. 2. Comparison between different energy harvesting systems

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circuit suitable for harvesters that are both low-voltage and low-current at the same time. Some authors [14], [15] face similar constraints using a buffer battery to provide the start-up voltage; since the battery provides limited energy packets it can last for a long time; still these systems are not fully autonomous. The interface circuit proposed in this paper works without batteries and is self-starting. It's architecture is flexible, suitable to work with various DC harvesters and to supply various loads and applications. It includes a capacitive energy storage stage and a voltage level conversion unit, based on a two-stage DC/DC converter. The harvester connected to the input charges a 140 mF supercapacitor up to a predetermined voltage, storing a well known amount of energy. Using a fraction of this energy, the interface circuit generates a low-voltage oscillating signal to drive a boost converter which charges an intermediate 2 μF capacitor to 2 V. Afterwards, a PIC microcontroller, supplied by the 2 μF capacitor, drives a second boost converter using the residual energy stored in the 140 mF supercapacitor to charge the output 470 μF capacitor from 0.5 V to 3 V or 5 V. At this point the load is triggered to carry out its operations and functions being supplied by the 470 μF capacitor.

The interface circuit has been tested with the same wireless temperature sensing application presented in [7]. Compared with those results, this new configuration allows a load-operation frequency four times higher, with the same solar irradiance and harvester area. Furthermore, the minimum light incident power required for proper operation of the system is one seventh than before.

The interface dimensions are dominated by capacitors and inductors, whose volume depends on the nominal capacitance or inductance and on the manufacturing technology. A trade-off between costs, circuital needs and dimensions has been sought and each of this components has been selected to be smaller than 1 cm^3. The volume of the complete system, including the external harvester and the RF antenna, has been estimated to be in the 6-9 cm^3 range (i.e. 3 cm $\times$ 3 cm $\times$ 1 cm).

Section II describes a first prototype based on a single boost converter while Section III presents the final double boost converter architecture. The sizing of the proposed system is described in Section IV, while Section V and Section VI present the complete wireless sensor node design and the achieved experimental results respectively.

II. Single Boost Converter Architecture

The starting point for this project was the know-how achieved in a previous research, that is the realization of a 3 V energy harvesting system [7]. In that case, a harvester charged a capacitor to a fixed voltage and then a power management circuit connected the capacitor to the load, using the stored energy to operate it. In this way, the harvester is only asked to charge the main storage capacitor and the load is decoupled from the source during the charging phase, allowing the system to be powered by a very low current. Moreover, the system is almost insensitive to the fluctuations of the power generated by the harvester, the only affected parameter being the frequency at which the load operation

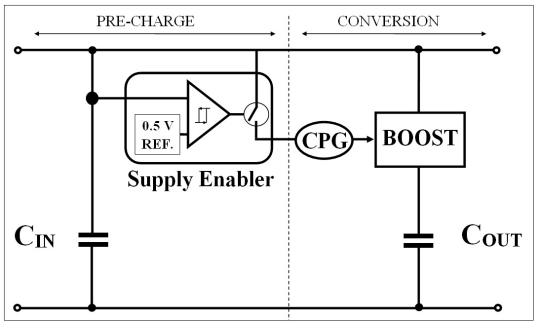


Fig. 3. Single boost converter interface circuit architecture

is triggered. In this paper the same strategy was used, with the difference that now the capacitor is charged to a lower voltage (0.5 V), thus an efficient means for stepping up the voltage to the level needed by the load is necessary. Before getting to the final version of the interface circuit, exploiting a double stage step-up conversion, a solution in which the output capacitor is charged by a single boost converter driven by a 0.5 V pulsed signal was considered. Fig. 3 summarizes the architecture of this first prototype of the system. The working cycle of the circuit is composed of two phases. Initially, the harvester charges the input storage capacitor C_{IN} while the boost converter is disconnected and the interface circuit is in an idle, low power consumption state. When the voltage across C_{IN} hits a preset threshold, the second phase starts and the boost converter is enabled, stepping-up the voltage. During the first phase, the only active part of the power management circuit is the Supply Enabler (SE), a custom circuit that senses the voltage across the capacitor and reacts when it reaches the threshold; as a consequence, the power consumption is minimized. Once C_{IN} is charged the SE enables the Custom Pulse Generator (CPG), an astable circuit that produces a signal at a fixed frequency and with a fixed duty cycle, used to drive the boost converter. During the second phase, the charge stored in C_{IN} is transferred to the output capacitor C_{OUT}, exploiting the input capacitor as a low-voltage generator but with a higher output current with respect to the harvester alone, a current suitable to sustain the boost conversion.

A. The Supply Enabler (SE)

The SE is a voltage-detection device coupled to a power switch. It is made of an hysteresis comparator, a fixed 0.5 V reference and the switch. When the voltage across C_{IN} reaches the 0.5 V threshold the comparator output goes high, turning the switch on. Therefore, the supply is coupled to the CPG and the conversion occurs.

B. The Custom Pulse Generator (CPG)

Fig. 4 shows the basic implementation of the CPG that drives the boost circuit. The gate of M_1 is connected to the central node of the voltage divider R_1-R_2: when the circuit is supplied, the voltage across R_1 is sufficient to turn M_1 on. The function of M_2 is to obtain a faster turn-on of M_1: as soon as the voltage across R_3 builds up M_2 starts to conduct

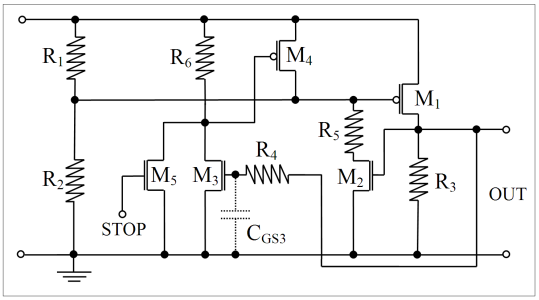


Fig. 4. Schematic of the Custom Pulse Generator (CPG)

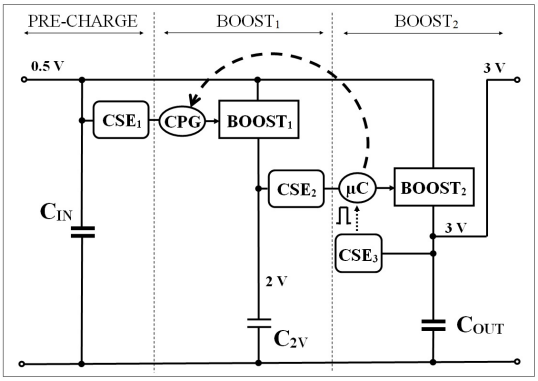


Fig. 5. Double boost converter interface circuit architecture

and pull the gate of M_1 down. The voltage across R_3 is also applied to the gate of M_3 but with a delay which depends on the R-C network made of R_4 and the parasitic gate capacitance of M_3, C_{GS3}; after this delay, M_3 - and consequently M_4 - turn on, turning M_1 off by zeroing its gate-source voltage. At this point the gate voltage of M_3 will fall down with a single time constant dynamics due to the R-C network made of the series of R_3, R_4 and C_{GS3}. This cycle will repeat indefinitely with a frequency and a duty cycle that depend on R_3, R_4, and C_{GS3}. The N-MOSFET M_5 is used to disable the circuit by means of an external signal.

C. Limitations of the Circuit

In the topolgy presented so far the signal used to drive the boost converter can be at most as high as the input voltage of the system. For instance, if the interface circuit is supplied by a low-voltage photovoltaic (PV) harvester, the signal produced by the CPG has a peak of about 500 mV: this value is not sufficient to turn on the N-MOSFET of the boost converter properly. As a consequence, during the on-state, the N-MOSFET exhibits a high drain-source resistance that heavily affects the global efficiency. Moreover, the raising and falling time of the impulse that controls the boost are imposed by the R-C networks of the CPG circuit. To limit the power consumption of the system, the resistance of R_3 of Fig. 4 should be as high as possible. However, this choice increases the time required to discharge C_{GS3}, which determines the slope of the impulse. Even with an optimal choice of the resistance and the use of ultra-low threshold MOSFETs, the circuit of Fig. 3 cannot charge an output capacitor of hundreds of μF to 3 V, thus limiting the applicability of the system.

III. Double Boost Converter Architecture

While the simple boost converter driven by the CPG at 0.5 V cannot charge to a suitable voltage a capacitor large enough to sustain a wireless transmission, it is able to charge a capacitor of few microfarads up to 2 V in a few seconds. For this reason, a double stage step-up conversion, whose block diagram is shown in Fig. 5, was adopted. The goal is still to transfer the energy from C_{IN} to C_{OUT} while performing a voltage step-up, but here the low efficiency boost converter driven by the CPG (called BOOST$_1$ in Fig. 5) is used to charge an auxiliary capacitor in the microfarad range (C_{2V}) to an intermediate voltage, e.g. 2 V. The amount of energy stored in C_{2V}, as small as it is, is enough to turn a low-power microcontroller (μC) on during the phase in which a second, higher-efficiency boost converter (BOOST$_2$, driven by the μC itself) is in charge of transferring energy from C_{IN} to C_{OUT}, charging it to 3 V. During this phase, the constant duty-cycle driving of the CPG is not able to maintain C_{2V} suitably charged because of the additional power consumption of the active μC; for this reason the μC takes control of BOOST$_1$ as well. The higher efficiency of BOOST$_2$ comes on one side from the fact that its N-MOSFET switch is driven by the μC with the more appropriate voltage of 2 V, on the other from the better quality (i.e. very short raising and falling times) of the driving signals generated by the μC. In other words, BOOST$_1$ can be viewed as a start-up circuit that creates the conditions to properly perform the high efficiency conversion of BOOST$_2$.

The various phases are sequenced by three Custom Supply Enablers (CSEs): the first one, CSE$_1$ monitors the input voltage and starts the operation of BOOST$_1$ as soon as the voltage across C_{IN} is 0.5 V; CSE$_2$ wakes the μC up, starting the operation of BOOST$_2$, when the auxiliary capacitor is charged up to 2 V; finally, CSE$_3$, monitors the voltage across C_{OUT} and generates an End-Of-Operations (EOO) signal when the 3 V threshold is reached, triggering the load. By enabling the various blocks only when needed, the CSEs contribute significantly in keeping the total power consumption of the circuit low; for instance the power consumption of the CPG and of BOOST$_1$ is negligible when they are not commutating: thanks to CSE$_1$ they will remain in this idle state as long as C_{IN} is charging, the only active part being CSE$_1$ itself. Similar considerations apply to the μC and BOOST$_2$. The principle of operation of the CSE and the peculiarities of each of the three are described in the following.

A. Custom Supply Enabler (CSE)

Fig. 6(a) shows the CSE functional diagram. The storing capacitor C represents the input of the circuit, while a generic load is connected at the output. The P-MOSFET M_1 with its pull-up resistor represents the load-enabling switch. The block called "Fixed Reference Voltage Comparator" (FRVC) has the functionality of a conventional voltage detector, raising its output when its supply voltage is above a fixed threshold. The FRVC controls the state of M_1 through the N-MOSFET

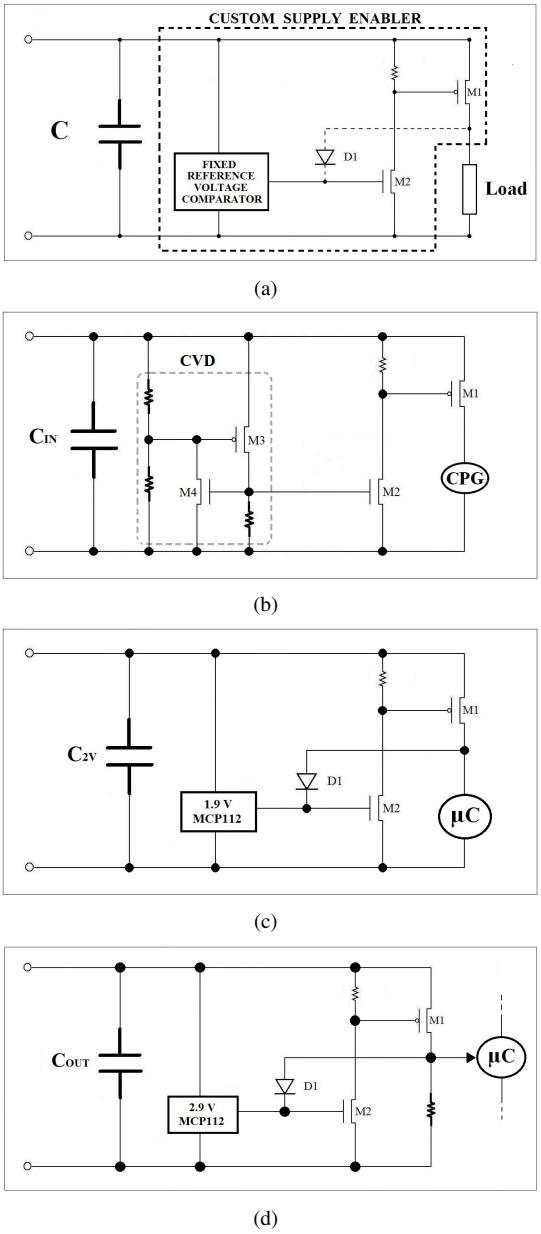


Fig. 6. CSE basic circuit (a) and circuital implementations of the Custom Supply Enablers CSE_1 (b), CSE_2 (c), and CSE_3 (d)

M_2: when the gate of M_2 is high, M_1 turns on, enabling the load. The diode D_1 is used to add an hysteresis: in fact, as soon as the capacitor is being discharged by the load, the FRVC would tend to lower its output, turning M_2 off; D_1 prevents this unwanted behaviour maintaining M_2 on until the voltage across C reaches a value equal to the threshold voltage of M_2 plus a diode drop. This circuit topology is suitable for integration through a basic comparator architecture with a low-voltage bandgap [16].

B. Custom Supply Enabler CSE_1

Fig. 6(b) shows the circuital implementation of CSE_1. This circuitry represents one of the most critical blocks of the system, since it is the only part connected to the harvester during the start-up phase (its input capacitor is C_{IN}). The FRVC is implemented with a Custom Voltage Detector (CVD) because of voltage detectors with a supply as low as 0.5 V are not available on the market. The CVD consists of two MOSFETs, M_3 and M_4, and a voltage divider that fixes the threshold. This solution exhibits an intrinsic hysteresis behavior, therefore diode D_1 of Fig. 6(a) is not included. However, this particular configuration introduces a small fluctuation of the threshold voltage caused by temperature, with a temperature coefficient of about 0.25 mV/°C.

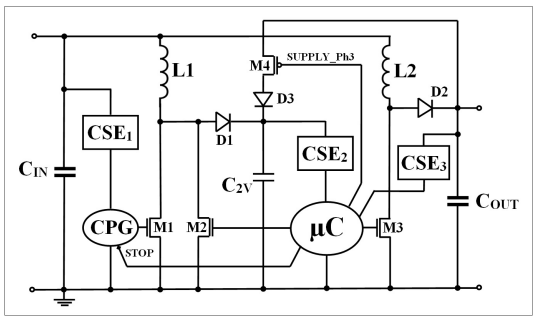


Fig. 7. μC-controlled subsystem

C. Custom Supply Enabler CSE_2

Fig. 6(c) shows the actual schematic of CSE_2. The circuit has C_{2V} at its input while the load is the μC. The FRVC is realized with a commercial voltage detector, the Microchip® MCP112-195. This component, usually exploited for μC power-monitoring and reset applications, has an internal voltage reference of 1.9 V and a low supply current ($<$1 μA typical), making it particularly suitable for low-power applications.

D. Custom Supply Enabler CSE_3

Custom Supply Enabler CSE_3 generates the EOO signal and has capacitor C_{OUT} at its input. The circuit is implemented by introducing in the basic CSE scheme a large resistor connected to the drain of M_1, as shown in Fig. 6(d). The voltage across this resistor becomes a logic signal that provides the trigger signal to the μC. The rest of the circuit is equivalent to CSE_2, but with a 2.9-V voltage detector, the Microchip® MCP112-290.

E. μC-Based Pulse Generator

The idea of driving $BOOST_2$ with a μC is justified by the fact that some data processing power is typically already present in the system, for example to perform some processing of the data to be transmitted; the effectiveness of the architecture can then be increased by exploiting this processing power during the energy accumulation phase as well. Furthermore, microcontrollers with a very low power consumption are available on the market; their power requirements can be further reduced by choosing the lowest possible clock frequency for the given application, as in the present case. Finally, the quality

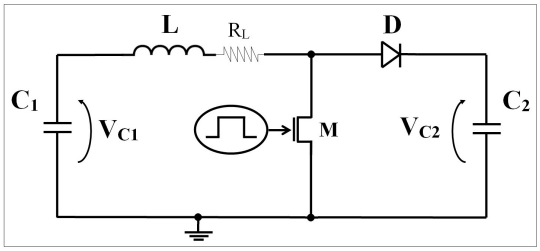


Fig. 8. Boost circuit with parasitic components

of the driving signals the μC can provide helps considerably the efficiency of $BOOST_2$, as mentioned before.

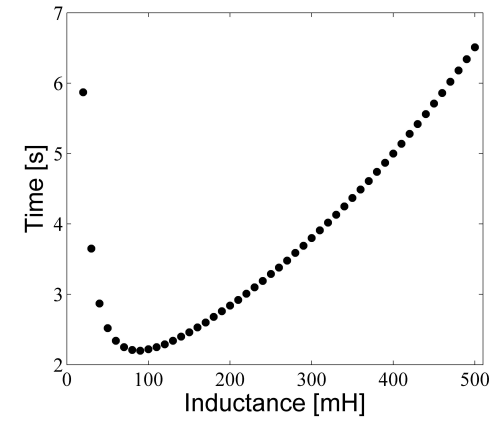
Fig. 7 shows the detail of how the μC is interfaced with the rest of the circuit: as soon as CSE_2 wakes the μC up, the latter starts driving $BOOST_2$ (through M_3); at the same time it inhibits the CPG through its STOP input (the μC acts on M_5 in Fig. 4) and drives $BOOST_1$ by means of M_2 which is connected to inductor L_1. When the charging up of C_{OUT} is completed, CSE_3 generates the EOO signal and the load can perform the useful function the system is designed for (for instance, data acquisition and transmission); being the μC involved in this process, the EOO signal in Fig. 7 goes directly to it. From this moment on the μC conceptually stops being part of the interface circuit and becomes the load together with the other load blocks (for example the RF subsystem). Since microcontrollers are intrinsically mono-tasking devices, as soon as the μC starts acquiring and processing data it quits driving $BOOST_1$ and $BOOST_2$; nevertheless the supply of the μC must be guaranteed and the energy stored in C_{2V} is not enough. For this reason the μC switches M_4 on, connecting C_{OUT} in parallel to C_{2V} through D_3.

IV. System Sizing

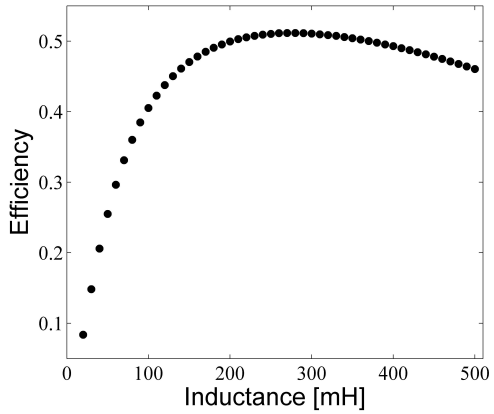
In Fig. 8 the schematic of a boost converter, as used in the presented system, is shown, where R_L represents the parasitic resistance of the inductor. The designer of such a system has a few degrees of freedom in designing it. As far as the capacitors values are concerned, the criterion for choosing them is pretty simple: given the voltages at which C_{IN} and C_{OUT} should be charged, 0.5 V and 3 V respectively, the value of C_{OUT} was chosen so as to leave a sufficient voltage across it after the load has completed its task; consequently, C_{IN} needs to store enough energy to recharge C_{OUT} considering the efficiency of the interface and, once again, with an acceptable voltage drop after the process of charging C_{OUT} ends. The purpose of C_{2V} is to supply the μC during its initial working phases: its capacitance value was chosen as lower as possible to perform this function, considering that it is charged to 2 V. The MOSFETs used as switches in the circuit were chosen basically because of their low threshold, a key requirement in such a low-voltage context, and their low drain to source resistance, to reduce losses. The most critical choice concerns the value of the inductors in the two boost converters: in fact, both conversion efficiency and conversion time depend on these inductors. Moreover availability of desired values and dimensions of the components should be considered as well. An analytical approach to the analysis of this circuit, with the aim of selecting the optimal inductor, is very complicated. For example, one may think of expressing the charging time as a function of the inductor value. However, since the voltage across C_2 increases during each switching cycle, the discharge time of the inductance decreases at each iteration and the charging time becomes a sum of varying intervals, a situation that does not give rise to a compact analytical formula. For this reason, the problem was approached by means of a series of parametric PSpice simulation with the inductor value as the parameter. Both $BOOST_1$ and $BOOST_2$ operate in discontinuous conduction mode (DCM), with the switch being driven by low-frequency switching signals with fixed duty cycle (as it will be detailed in the following, the CPG works at 100 Hz, the μC generates a 2 kHz output signal). Both converters use the same low threshold MOSFETs and diodes. In the PSpice simulations the MOSFET was modeled as an ideal switch with a fixed on resistance equal to the drain-source resistance of the actual MOSFET; C_1 and C_2 were modeled as ideal capacitors; the inductor L has its series parasitic resistor R_L; the diode D was of the BAT85 type. $BOOST_1$ has been designed to charge a capacitor of few μF to 2 V. In this circuit, because of the low voltage available to drive the switch and despite using a low threshold MOSFET, the switch is barely ON when V_{gs} is high and the corresponding drain-source resistance was evaluated to be around 500 Ω. The driving signal was modeled as an ideal, 500 mV pulse generator with a 2 % duty cycle. Finally, the inductor resistance was assumed to be proportional to the square root of its inductance. The results of 50 simulations of $BOOST_1$ as a function of the inductor value are shown in Fig. 9.

In particular, Fig. $9(a)$ shows the time needed to charge C_{2V} to 2 V while Fig. $9(b)$ shows the efficiency of the process, calculated as the ratio between the energy stored in C_2 when the charging process is over and the energy lost by C_1 in the same interval. Both graphs exhibit an extreme: one may choose the inductor value that gives the shorter charging time or the highest efficiency. Since the energy transferred to C_{2V} is very small with respect to the total energy stored in C_1, the efficiency is not so critical, because in any case, even when the efficiency is less than optimal, the voltage drop across C_1 will be negligible. For this reason we have preferred to select an inductance value (100 mH) that reduces the charging time even if efficiency is not maximized. This value is also convenient in terms of size and cost. On the contrary, $BOOST_2$ has to charge a much bigger capacitor up to 3 V and efficiency becomes of upmost importance. Furthermore, in this case the switch is more suitably driven by the μC and the value of the drain-source resistance of the MOSFET is reduced to 0.5 Ω; the duty cycle of the driving signal is 50 %. The results of 25 simulations as a function of the inductor value are shown in Fig. 10.

Fig. $10(a)$ represents the time needed to charge C_{OUT} to 3 V with respect to the value of inductance while $10(b)$ shows the efficiency, calculated as for the previous case. In this case, both curves are monotonic and a criterion for choosing the inductor value needs to be sought after. For $BOOST_2$ we decided to make the efficiency the highest priority. Looking

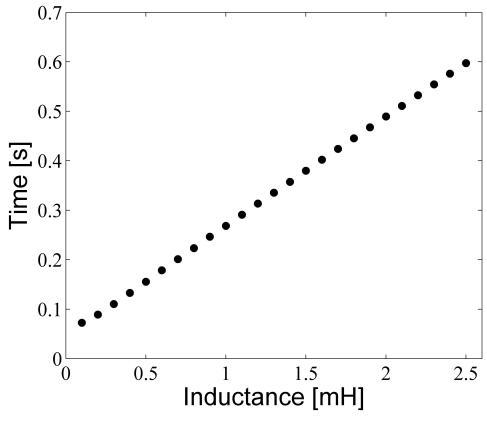


(a)

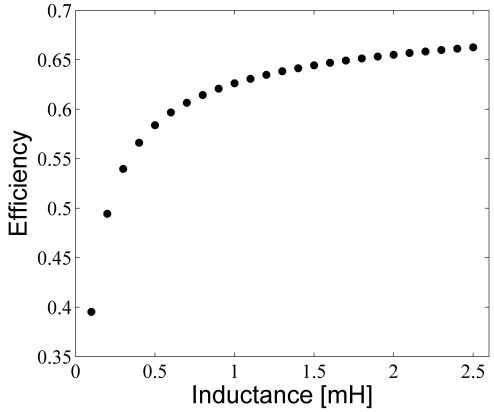


(b)

Fig. 9. (a) relationship between the time needed to C_{2V} to reach 2 V and the value of the inductance; (b) relationship between efficiency and the value of the inductance.



(a)



(b)

Fig. 10. (a) relationship between the time needed to C_{OUT} to reach 3 V and the value of the inductance; (b) relationship between efficiency and the value of the inductance.

at the curve in $10(b)$ it becomes apparent that increasing the inductance value above 1 mH gives only a modest increase in efficiency while the charging time increase consistently: as a consequence a 1 mH inductance has been selected, which represents a good trade-off between charging time and efficiency.

V. Photovoltaic Wireless Sensor Node

In order to test the proposed interface in realistic conditions, a complete harvesting system was built whose block diagram is shown in. Fig. 11. The interface circuit is powered by a photovoltaic cell, integrated in 0.35-μm BCD, SOI technology [17], whose dimensions are 385 μm $\times$ 245 μm. The load a temperature sensor station composed of an ultra-low-power μC (the Microchips® PIC18LF13K22), a 802.15.4-compliant wireless transmitter (Microchip® MRF24J40MA) and a low power temperature sensor (Analog Devices® TMP36). As previously outlined, the μC is shared between the interface circuit, driving the DC/DC converters, and the load, supervising its operation: the μC is programmed to perform data acquisition from the sensor and to transmit the information through the wireless module.

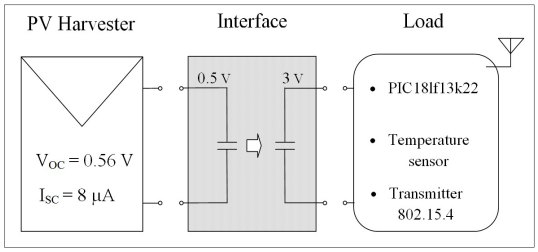


Fig. 11. Block diagram of the photovoltaic wireless sensor node

Given the energy required by the load for a working cycle — about 0.8 mJ — a 470 μF capacitor was chosen for C_{OUT}, giving a residual voltage of 2.4 V at the end of the transmission.

As far as C_{IN} is concerned, a maximum voltage drop of 50 mV after C_{OUT} gets charged to 3 V was chosen: assuming a global efficiency of 50% (which means a total drawn energy of 1.6 mJ), the required capacitance is about 50 mF. At the end, a 140 mF capacitor (CAP-XX® GW209F) was actually used because of low-leakage performance [18], availability and cost reasons.

Capacitor C_{2V} is application independent, since its choice

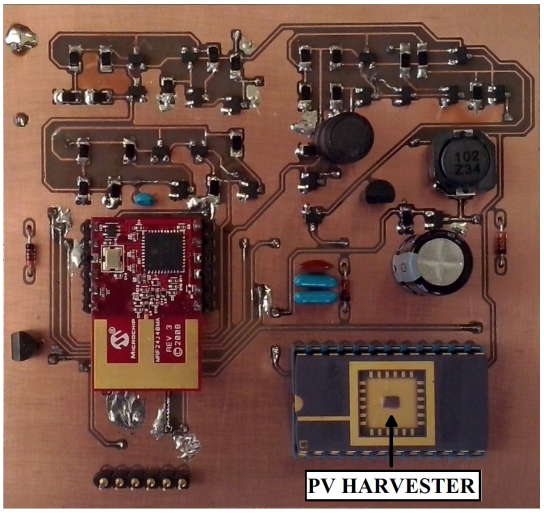


Fig. 12. Photograph of the system prototype (dimensions: 80×90 mm)

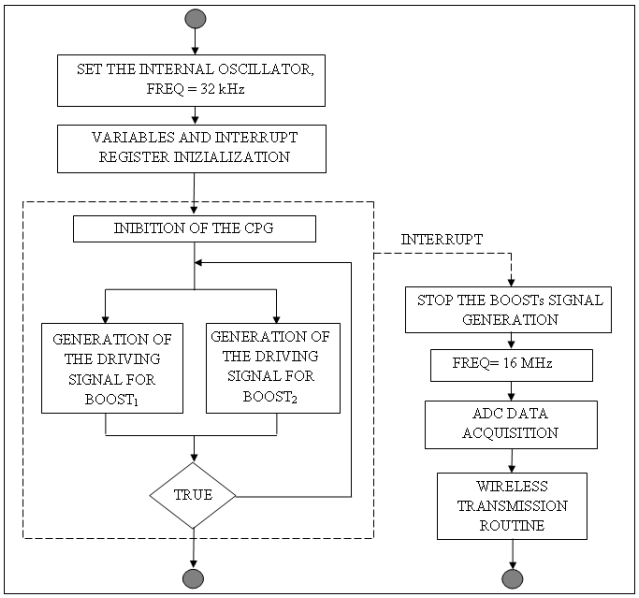


Fig. 13. Flowchart of the μC firmware

is driven by the μC electrical characteristics, which are uncorrelated to the characteristics of harvester and of load; a 2-μF ceramic capacitor showed to be suitable to sustain the μC supply during its initialization.

Fig. 12 shows the photograph of the realized prototype Printed Circuit Board (PCB), implementing the system. The board has been produced for testing and debugging purposes and is not representative of the miniaturized circuit that could be obtained by the use of more specific manufacturing technologies.

A. The μC firmware

Fig. 13 shows the flowchart of the μC firmware. The algorithm is designed to minimize the μC power consumption as much as possible. For this reason, the μC internal oscillator has been chosen and the lowest possible working frequency (32 kHz) has been selected. Furthermore, none of auxiliary blocks available in modern μCs have been used: in fact, activating them causes the current absorption to increase. For example, all the signals used to drive the switch in the Boost converters are generated through custom algorithms instead of using the PWM module and the supply of the μC is managed by CSE_2 instead of using the POR module. The firmware consists of a main routine — that is cyclically executed and which implements the interface functions — and of an interrupt subroutine — which develops the load related operations. At the beginning of the algorithm, after the device settings and initializations, the CPG is inhibited by raising of the output port connected to the CPG STOP input; after that, the μC starts driving both $BOOST_1$ and $BOOST_2$. The generation the these two signals is carried out by a custom algorithm designed to manage at the same time two different tasks.

The μC exits the infinite cycle only when CSE_3 generates the EOO signal that is sensed by the μC through an interrupt input port. When the EOO occurs, the algorithm jumps to the interrupt subroutine, the boosts driving signals are stopped and the load operation is carried out. The μC acquires data from the temperature sensor by means of the its embedded ADC module and transmits the achieved information through the external wireless module. When the transmission is over it returns to its inactive mode, waiting for a new cycle to begin.

VI. Experimental results

Initially, the system prototype has been tested under controlled conditions, with a light irradiance of 600 W/m^2 and a temperature of 30 °C, values that can anyway be found in a real outdoor scenario; in these conditions the current delivered by the harvester is about 8 μA [19].

Fig. 14 shows the measured voltages across capacitors C_{IN}, C_{2V} and C_{OUT}. In particular, Fig. 14(a) shows a complete start-up transient: at the very beginning all three capacitors are connected in parallel through L_1, D_1, L_2, and D_2 (Fig. 7) and are charged to about 0.5 V; as soon as the voltage across C_{IN} reaches 0.52 V, the cyclical operation of the load begins. Fig. 14(b) shows a detail of the first transmission: the time interval between A and C is the very short spike in Fig. 14(a). When C_{IN} has reached 0.52 V (A), C_{2V} is charged by $BOOST_1$, driven by the CPG, in about 2 seconds. As soon as C_{2V} reaches 1.9 V (B), it is suddenly discharged, because CSE_2 enables $BOOST_2$ and the μC, the latter being supplied by C_{2V} only. This fast discharge continues down to 1.4 V with a high slope; at that point, after an initialization delay, the μC takes control of $BOOST_1$, compensating the discharge of C_{2V}, and reducing the slope. After the same initialization delay, the μC also starts to drive $BOOST_2$ and to charge C_{OUT} to 3 V: this process lasts only about 300 ms, thanks to the value of the inductor of $BOOST_2$ and the higher operating frequency, as previously described. During the time interval from (B) to (C) the discharge of C_{IN} can be appreciated as well.

Finally, when C_{OUT} reaches 3 V, the operation of the load can begin (C): at that point the μC stops controlling $BOOST_1$ and C_{2V} is connected in parallel to C_{OUT} through M_4 and

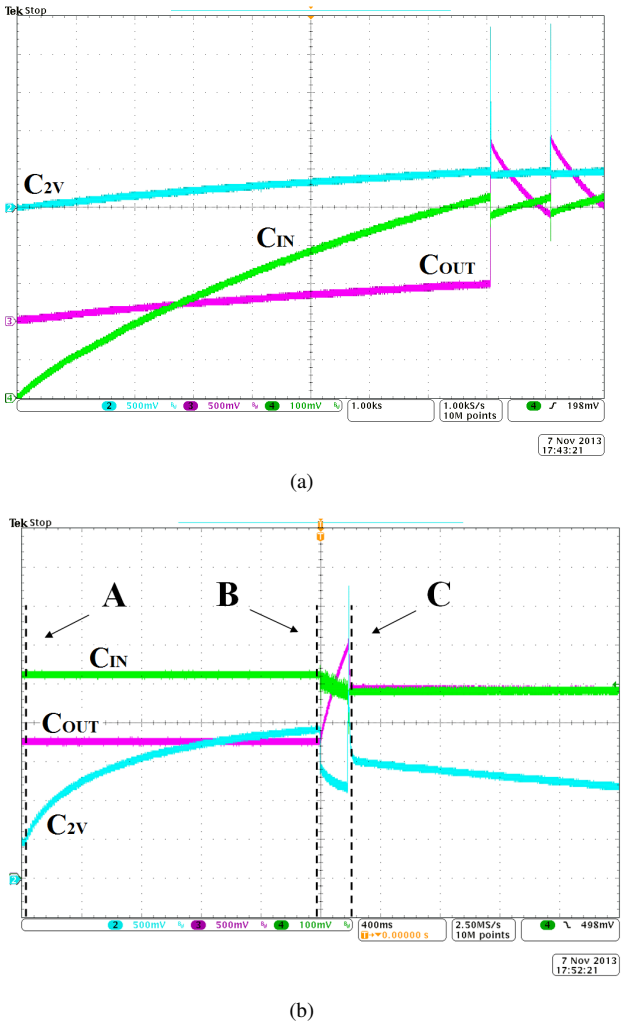


Fig. 14. Measured voltage across C_{IN} (green), C_{2V} (cyan), and C_{OUT} (magenta), under an artificial illumination of 600 W/m^2, at 30 °C: (a) full start-up transient, (b) detail of a load operation cycle.

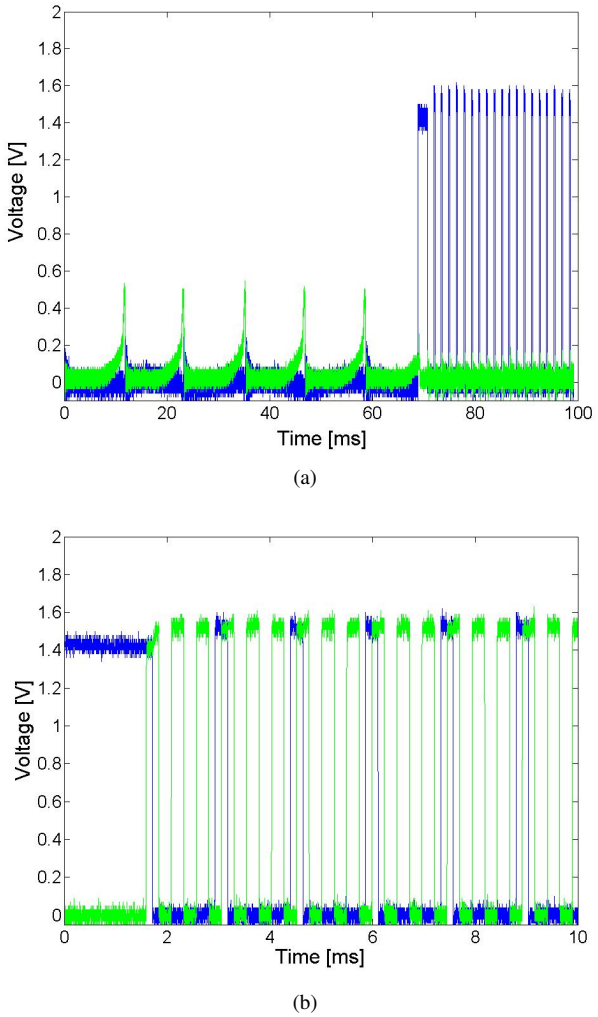


Fig. 15. Driving signals of the boost converters: (a) BOOST$_1$ before (green) and after (blue) the activation of the μC activation; (b) BOOST$_1$ (blue) and BOOST$_2$ (green) when driven by the μC.

D_3 (Fig. 7) in order to maintain a proper supply voltage for the μC, the temperature sensor, and the wireless module; this justifies the small, upward discontinuity of the voltage across C_{2V}: it is quickly charged at instant (C) to the same voltage as C_{OUT} minus the voltage drop across D_3. During this phase C_{OUT} is discharged by the energy consumption of the load and, as expected, reaches a minimum voltage of 2.4 V (the details of this are hard to see even in Fig. 14(b) because the working cycle of the load lasts a few milliseconds). When the active phase of the load is over, C_{2V} exhibits a further slow discharge while the μC is being switched off. At that point, M_4 switches off as too, coupling C_{2V} back to C_{IN} and starting a new cycle that will end as soon as C_{IN} reaches 0.52 V. The exponential discharge of C_{OUT} that can be appreciated in Fig. 14(a) between two transmissions is due to its self-discharge effect.

Fig. 15 shows the measured driving signals of the boost converters during the two phases of the interface circuit operation. In particular, Fig. 15(a) shows the driving signals of BOOST$_1$, before and after the activation of the μC: initially, a 100-Hz,-0.5-V driving signal with 2% duty-cycle is provided by the CPG; when the μC awakes, after the aforementioned initialization delay (during which the driving signal is maintained high), a 0.67 kHz, 1.5-V driving signal with a 20% duty-cycle is generated. By contrast, Fig. 15(b) shows the driving signals applied by the μC to BOOST$_1$ and BOOST$_2$ during the second phase: BOOST$_1$ is driven at the minimum possible frequency, just what is enough to sustain supply voltage of the μC; BOOST$_2$ is optimized to operate with a switching frequency of 2 kHz and 50% duty cycle.

The system was also tested in worst case conditions: the purpose was to identify the minimum required voltage and current of the harvester that allows a correct operation of the interface. By using a Keithley® 2000 digital multimeter these limits have been identified to be 2 μA and 0.5 V. These measurements also showed that the current consumption is dominated by the leakage current of capacitor C_{IN} and that the actual current consumption of the circuitry is about 1 μA when charging C_{IN}.

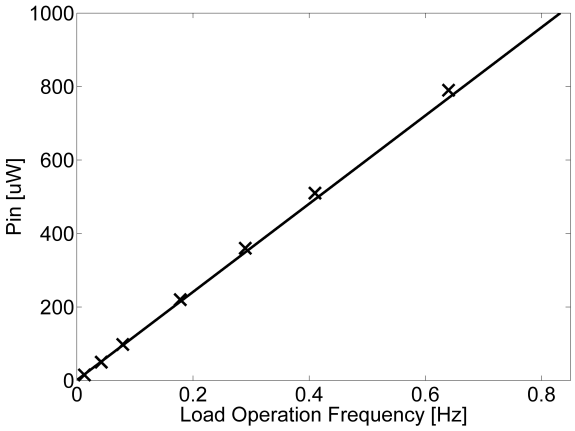


Fig. 16. Wireless transmissions frequency with W_{load} = 0.8 mJ

TABLE I
ENERGY HARVESTING SYSTEMS COMPARISON

	[20]	[21]	[14]	This work
Input voltage	$>$ 0.6 V	20 mV to 250 mV	0.5 V - 2 V	$>$ 0.5 V
Output voltage	0 - 3.3 V	1 V	0 V - 5 V	0 V - 5 V
Power throughput	10 μW 1 mW	1 μW 100 μW	5 μW 19 mW	1 μW 1 mW
Battery	2 V	1 V	3 V	Batteryless
End-to-end efficiency	70 %	N/A	70 %	65 %
Start-up voltage	$V_{IN} > 0.6$ V and $V_{BT} > 2$ V	$V_{BT} > 0.6$ V	$V_{IN} > 1$ V or $V_{BT} > 1$ V	$V_{IN} > 0.5$ V

It is also possible to evaluate the load operation frequency:

$$f = \frac{P_{IN} - P_C}{\frac{W_{load}}{\eta}}, \quad (1)$$

where P_{IN} is the power delivered by the harvester, P_C is the power consumption of the interface during the pre-charge phase, W_{load} is the energy for a single load operation and η is the global efficency of the interface. The latter has been calculated as the ratio between the energy gained by C_{OUT} and the energy delivered by C_{IN} in the time window from (B) to (C); its value is of about 65 %.

As the CSE_1 divider impedance is some Mohm, P_C is mostly influenced by the leakage current of C_{IN}: at 0.5 V, P_C is about 1 μW. In order to verify (1), a series of measurement with a controlled DC supply as a power source have been carried out: Fig. 16 shows the measured value of the wireless transmission frequency with different P_{IN} with together with the frequency calculated from (1).

To conclude, in Table I a comparison between the proposed interface and several recent energy harvesting systems based on DC/DC converters is presented.

VII. CONCLUSIONS

The power management techniques implemented in the proposed interface circuit allow proper operation of a energy harvesting system supplied by a transducer only capable of both low voltage and current. The correct operation of the system is guaranteed the harvester delivers at least 2 μA at 0.5 V, but it can of course work with higher values, thus allowing high flexibility in the choice of the energy source.

As a test case, a complete wireless sensor node, powered by an integrated BCD SOI photovoltaic harvester, has been successfully built and tested.

The volume of the interface circuit is dominated by the storage capacitors and inductors, which cannot be integrated: overall, it turns out to be smaller than 9 cm^3.

VIII. ACKNOWLEDGEMENT

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