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CMOS-Based Multifrequency Impedance Analyzer for Biomedical Applications

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***Abstract*—In this paper we present a monolithic microsystem, which can perform Bio-Impedance Analysis (BIA), and electro impedance tomography (EIT) measurements as well as record electrocardiogram (ECG) signals. In contrast to a full analog lock-in approach, a mixed analog/digital solution is adopted. The proposed solution has been designed, implemented and tested using a commercial 0.35-µm CMOS technology. The tuning range of the signal generator and the detector is from 10kHz to 10MHz in 1kHz steps. The circuit ensures a CMRR of 81dB@10kHz, which increases to 84dB@10MHz. The measured equivalent input noise power spectral density is en=2.57nV/√Hz at 10kHz in the worst case, close to the 1/f corner frequency. It decreases until en=1.8nV/√Hz at 1MHz and en=1.9nV/√Hz at 10MHz. Measurements of a reference RC network performed with the proposed monolithic solution and compared with a Keysight E4980A Precision LCR Meter shows a maximal relative error of 0.8% over the whole operating frequency range.**

***Index Terms*— Bioimpedance, Biomedical electronics, Biomedical monitoring, Biomedical telemetry, Demodulation, Digital modulation, Electrocardiography, Impedance measurement, System-on-chip**

I. Introduction

BIO-IMPEDANCE Spectroscopy, BIA, and EIT techniques have been widely investigated for measuring many different human pathologies. The characteristic of being a noninvasive, low cost solution, makes the bio-impedance measurement technique an optimal candidate for IoT devices and portable systems (i.e. arm band, fitness tracker devices, smartphone, health monitor devices). Bio-impedance spectroscopy has been used to monitor the hydration level of subjects suffering from renal disease [1], to evaluate the status of human tissue [2], or to quantify the body composition [3]. Moreover, it has been reported that BIA has been successfully employed to measure breathing rate [4], glucose level [5], and pulse wave velocity [6]. In addition, by using the EIT approach, the measurement principle of bio-impedance spectroscopy has been used to obtain time varying 2D images of the thorax for real-time lungs activities monitoring purposes [7].

Renal failure is the pathology where this organ loses its normal functional capacity. In advanced cases, when the renal function is severely impaired the dialysis therapy is the only available way to compensate for its malfunction. Dialysis therapies available today do not guarantee that at the end of a dialysis session the balancing of body fluid is adequately addressed. Recent findings have documented that fluid accumulation between dialysis sessions is a powerful predictor of death and cardiovascular complications [8]. Among all pathologies, hypervolemia is one of the most difficult to diagnose and one which may expose patients to an increased risk of death. Indeed, fluid accumulation will inevitably lead to hypertension. When the circulating volume is excessive, i.e. more than what the heart can effectively cope with, a congestive heart failure may arise. Hypervolemia usually manifests as pulmonary edema and peripheral edema.

With the BIA approach, the electrical impedance of the body is measured by injecting (through a couple of electrodes) a small alternating current into the body at controllable frequencies and by measuring the induced potential difference through others two electrodes [9]. Often the bioimpedance is measured in distributed manner over the body [10]. However the possibility to carry out a very precise and localized measurement allow to characterize the composition of the tissue. Applying the monitoring to the thorax region we have the possibility to learn in precise, accurate and not invasive way the amount water, which may accumulate in lungs, during the dialysis therapy. In the literature there are many studies that confirm the possibility to detect an edema state by measuring the thorax impedance. In particular, the study of Z.-Y Peng at al. [11] shows that changes of 2 - 6Ω of transthoracic impedance in animals (dogs) can be directly correlated to the presence of a pulmonary edema. In the last few years, many BIA systems have been developed [12-14], but the resolution is

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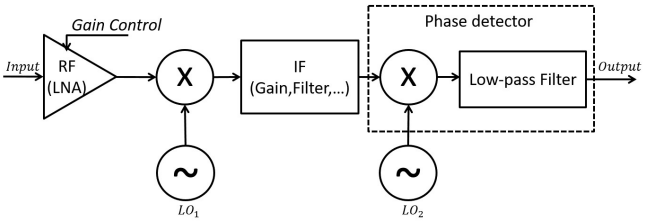

Fig. 1: General scheme of a heterodyne lock-in amplifier

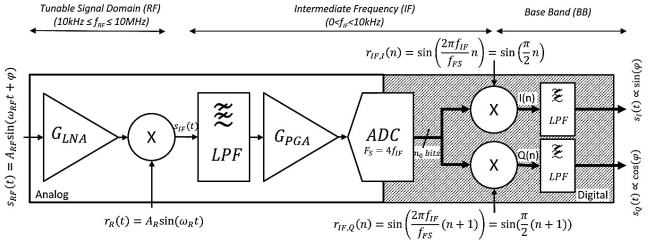

Fig. 2: Proposed improved heterodyne lock-in amplifier

often limited around 1Ω and the frequency response is not more than a few MHz. These current systems allow to make a qualitative assessment of the examined tissue, but they do not make it possible to obtain an image reconstruction of the liquid distribution in the lungs, which would allow to precisely identify the location of a possible edema.

On the other hand, Electrical Impedance Tomography (EIT) is a non-invasive, radiation-free technique of imaging, which can be used for the detection of pulmonary emboli, non-invasive monitoring of heart function and blood flow [15]. The principle of EIT is based on the back-image reconstruction of the voltage distribution obtained by stimulating a tissue with a current signal applied through electrodes distributed on the chest. A current application at the surface of a subject with homogenous bioelectric properties causes a reproducible distribution of potentials inside the subject. The regions in the chest with the same electrical potential, as a result of current application, are called isopotential lines. The distribution of isopotential lines contributes to a predictable voltage profile on the surface of the body. An increasing of impedance in a region results in a change in each of the voltage profiles which make up one frame. In the EIT case, image reconstruction requires voltage measurement with very high resolution of the order of nanovolts [16]. Thanks to the similarity between BIA and EIT measurements, it is possible to design and develop a system capable of providing both the characterization of impedances and the 2D image of a thorax's section. Moreover, it is also possible to monitor both ECG and respiration rate signals with the same system, which will allow having a complete monitoring of the patient's vital parameters during the dialysis therapy.

In this work, a monolithic mixed-signal (analog/digital) chip for a portable bio-impedance analyzer and EIT system is proposed. This device performs all of the tasks necessary to achieve bio-impedance/EIT measurements in the frequency range from 10kHz to 10MHz. Moreover, the proposed device allows measuring both bio-impedance and ECG signals. Furthermore, thanks to a programmable integrated routing network, which allows connecting in a flexible way the electrodes with the internal device building blocks, the same chip can be used to perform EIT.

The study and design of the proposed integrated system is the continuation of our previous work (see [1]) where we have developed a discrete device, which allowed us to study the correlation between the change in impedance and the hydration level. Based on [1] we have determined the levels of performance required to design the ASIC device in such a way to be able to cover all applications (BIA/EIT/ECG).

The paper is organized as follows: Section II describes the detection principle and the system architecture of the CMOS-Based Multifrequency Impedance Analyzer. Section III analyzes the key structures of the ASIC by providing more details on the working principle and by analyzing the ASIC form a theoretical point of view. Section III highlights the effectiveness of the proposed solution by means of computer simulation. Section V describes the circuit implementation. Section VI presents the measurements results and finally sections VII concludes the paper.

II. Detection Principle and System Architecture

In literature over the years many solutions which incorporate a lock-in amplifier into an integrated circuit have been proposed. One of the most interesting approach was proposed by Davide Bianchi et al. [17]. A high performance lock-in amplifier capable of working up to 150MHz has been implemented in CMOS 0.35µm technology. However, the design was optimized for current mode measurement and the reference signal need to be provided by an external source. Another design able to perform high frequency impedance measurement was proposed by A.Manickam et al. [18], but also in this case only the lock-in core was integrated, and the input was optimized for current mode operation.

The solution proposed in this paper combines the lock-In approach with the dual step superheterodyne demodulation scheme. Furthermore, in alternative to the full analog approach a mixed analog/digital solution is adopted. The device is able to measure both currents used for stimulation and voltages available on the sensing electrodes. Impedance evaluation and signal processing, is carried out half on chip and half off chip, by means of a microcontroller.

A. The proposed hybrid heterodyne lock-in amplifier

The working principle of the lock-in amplifier relies on the orthogonality of sinusoidal functions. In particular, the locking amplifier takes advantage form the property of the multiplication of two sinusoids. Namely, when a sinusoidal function $f_1(t)$ of frequency ω_1 is multiplied by another sinusoidal function $f_2(t)$ at frequency ω_2, different from ω_1, and integrated over a time much longer than the period of the two functions, then the result converges to zero. Instead, when the two frequencies ω_1 and ω_2 are in phase, the average value is equal to half the product of the amplitudes.

Heterodyning is a technique used to generate a new frequency by combining or mixing two frequencies. In telecommunications this principle is widely used in the radio

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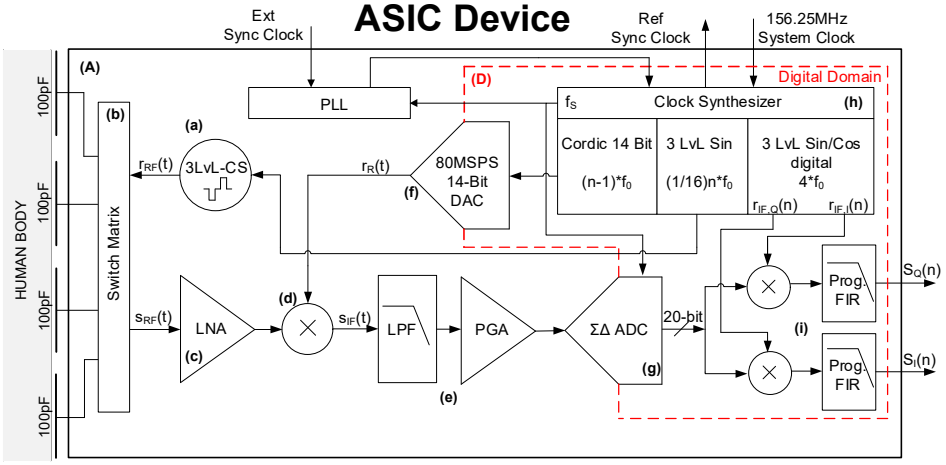

Fig. 3: System architecture [23]

receivers and transmitters.

The basic concept of the operation of the heterodyne structure can be described as follows (Fig. 1). The incoming signal, after being pre-amplified by a low noise amplifier in the radio frequency domain (RF), is mixed with a local oscillator (LO1) to produce sum and difference frequency components. The LO1 is selected to shift the RF signal to a fixed and known intermediate frequency (IF) (IF < RF) where all the signal conditioning and processing can be carried out. By following this approach, it is therefore possible to optimize the signal processing at a fixed known frequency, without the need to retune the whole processing chain depending on the incoming signal.

In conventional approach [18], the full acquisition chain of a heterodyne lock-in amplifier is implemented in the analog domain (LNA, low-pass filter, and phase detector) and the output of the phase detector generates DC signals which correspond to the In-phase (I)/Quadrature (Q) components of the signal to be sensed. With the proposed solution (Fig. 2) the LNA amplified signal is first frequency-shifted to the intermediate frequency (f_{IF}) domain, low-pass filtered (LPF) and then sampled by an analog-to-digital converter (ADC). At the end, the sampled signal is digitally demodulated and filtered to obtain the I/Q DC values. In this way, the phase detector is fully implemented in the digital domain. In general, when dealing with low noise and offsets, most of the analog circuits need to include chopping and active offset compensation techniques. On the other hand, by sampling the signal directly at intermediate frequency, these techniques turn out to be unnecessary. In fact, in the IF domain, the signal of interest is embedded in the AC component of the signal. This makes the detector immune to all DC signal components, which are added by the analog circuitry, or which were already present in the signal. Furthermore, by choosing the value of the intermediate frequency appropriately, it is possible to inherently limit the effects of noise (e.g. by placing f_{IF} > flicker noise corner frequency).

Digital demodulation normally requires complex digital circuits, which are capable of performing full precision multiplications. By choosing the sampling frequency equal to four times the intermediate frequency, the digital demodulation can be achieved by means of simple digital circuits. Moreover, by implementing a fully programmable digital low pass filter after the digital demodulator, the bandwidth of the phase detector can be digitally tuned according to the type of measurements required. In addition, the proposed system turns out to be also optimal for sharing circuits blocks. In particular, thanks to the low sampling frequency, this solution allows the use of time-multiplexing resource sharing, implementing a double demodulator and a double digital low-pass filter, with a single digital structure. The first digital demodulator decodes the in-phase signal (I demodulator), and the second digital demodulator decodes the quadrature signal (Q demodulator). This approach always ensures absolute consistency between the I and Q samples, and thus guarantees the highest possible accuracy in the detection of magnitude and phase.

B. System architecture

The system architecture is shown in Fig. 3. Compared to other solutions [18, 19], this new architecture combines the lock-in approach with the dual step super-heterodyne demodulation scheme. In contrast to the full analog approach, a mixed analog/digital solution is adopted. In particular, this solution performs a first frequency down-conversion in the analog domain (A) and shifts the I/Q demodulation in the digital domain (D). This has the big advantage of removing any sensible dual path from the analog domain (I and Q analog phase detectors) with important benefits in terms of circuit complexity, detector precision, and power consumption.

As shown in Fig. 3, the analog domain includes all the circuits required to generate the stimulation currents and to collect the induced voltage signals: (a) three level current source, (b) switch matrix, (c) low-noise amplifier, as well as the circuits necessary to perform the first step of the lock-in detection: (d) signal probing frequency (RF) to intermediate frequency (IF) demodulator mixer, (e) programmable gain amplifier and antialiasing filter, (f) digital to analog converter for generating a 86dB SNR sinusoidal demodulation signal,(LO) (g) sigma-delta modulator ADC. Fig. 3 also shows the digital domain blocks, including: (h) the synchronous signal generator, (i) the ADC decimator and the digital part of the lock-in detector, and

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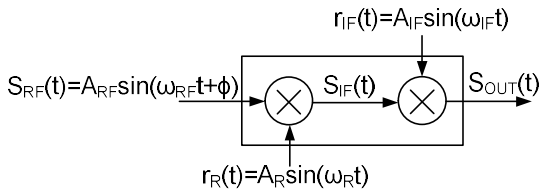

Fig. 4: Heterodyne demodulator

all control logic required to manage the chip and to communicate with an external microcontroller. Furthermore, the chip has a built-in PLL to provide the synchronization with other devices for a multichip operation (EIT operation mode).

III. System Analysis

A. Heterodyning and intermediate frequency IF

In order to appreciate the effectiveness of the proposed approach we evaluate the signal transfer function of the ideal heterodyne modulator shown in Fig. 4 (for simplicity a single path is considered – the I phase detector), where ϕ is the phase between the input signal (at ω_{RF}) and the two reference frequencies ω_R and ω_{IF}. By recalling the trigonometric product -to-sum identities and by noting that $\omega_{RF} = \omega_R + \omega_{IF}$, we can write the signal at the intermediate stage as:

$$S_{IF}(t) = \frac{A_{RF}A_R}{2}\left(cos(\omega_{IF}t + \phi) - cos\left((2\omega_R + \omega_{IF})t + \phi\right)\right) \quad (1)$$

from which it directly follows that:

$$S_{out}(t) = \frac{A_{RF}A_RA_{IF}}{4}(\sin(-\phi) + \sin(2\omega_{IF}t + \phi) - \sin(2(\omega_R + \omega_{IF})t + \phi) - \sin(-2\omega_R t - \phi)) \quad (2)$$

Eq. (1) shows that $S_{out}(t)$ is the combination of "image" signals with frequencies higher than the intermediate frequency f_{IF}, and a DC component, which depends only on the phase ϕ between the input signals. Furthermore from Eq. (1) if follows that if a DC signal k is superimposed to the incoming signal (i.e. an offset added by an input amplifier)

$$S_{RF_{dc}}(t) = S_{RF}(t) + k \quad (3)$$

at the IF stage the DC signal will be moved at frequency $f_R > f_{IF}$

$$S_{IF_{dc}}(t) = S_{IF}(t) + kA_{IF}\sin(\omega_R t) \quad (4)$$

which allows removing the unwanted effects of any DC components by implementing a LPF in the IF domain, before performing the second demodulation step.

In the same way a DC component added in the IF domain will be translated at frequency f_{IF} at the output of the second modulator stage. Therefore, all DC signals added by the circuitry in the RF and IF domain will not affect the accuracy of the measurement.

With the proposed hybrid approach, the second demodulator is implemented in the digital domain. Digital demodulation normally requires full precision multiplications. In general floating points units are implemented to minimize the effect of rounding and approximation. Instead, with the proposed solution, we are able to perform the demodulation step in a simple way.

By sampling the IF signal at four times the IF frequency, it results that the demodulation has to be performed with a reference sine wave sampled at four times its fundamental frequency (sampling frequency f_S=4f_{IF})

$$\left(r_{IF}(n)\right)_{@f_S} = \sin\left(\frac{2\pi f_{IF}}{f_S}n\right) = 0,1,0,-1,0,\ldots \quad (5)$$

By operating at four time the IF frequency, it means that the operation of demodulation is transformed into

$$s_{out}(t) = s_{IF}(t)\cdot r_{IF}(t) \quad (6)$$

$$(s_{out}(n))_{@f_S} = (s_{IF}(n))_{@f_S}\cdot(s_{IF}(n))_{@f_S} \quad (7)$$

$$(s_{out}(n))_{@f_S} = (s_{IF}(n))_{@f_S}\cdot\sin\left(\frac{2\pi f_{IF}}{f_S}n\right) \quad (8)$$

$$(s_{out}(n))_{@f_S} = (s_{IF}(n))_{@f_S}\cdot(\text{n \& 0x01})\cdot(-1)^{(n\ \mathbf{shr}\ 1)} \quad (9)$$

where n is a positive integer number and **shr** is the logical shift right digital operation on integer numbers.

When implemented with digital circuits, the demodulator is obtained with a simple inversion of sign combined with some logic gates. This mathematical approach has the valuable property to implement an ideal demodulation without adding any inaccuracies due to the digital quantization and due to the digital multiplication. In other words, this means that the accuracy of this phase detector is only determined by the resolution of the AD converter.

B. Operating frequencies

An essential condition to ensure proper operation of the whole system is the absolute synchronization among all of the signals, as well as respecting the following relationships among the signals:

$$f_{RF} > f_R > f_{IF},\ f_{RF} = f_R + f_{IF} \quad (10)$$

$$r_R(t) = A_R\sin(2\pi f_R t) \quad (11)$$

$$r_{IF,I}(n) = \sin\left(\frac{2\pi f_{IF}}{f_S}n\right) = sin\left(\frac{\pi}{2}n\right) \quad (12)$$

$$r_{IF,Q}(n) = \sin\left(\frac{2\pi f_{IF}}{f_S}(n+1)\right) = sin\left(\frac{\pi}{2}(n+1)\right) \quad (13)$$

$$f_S = 4\cdot f_{IF} \quad (14)$$

where f_{RF} is the frequency of the input signal s_{RF} resulting from the interaction of the current reference signal $r_{RF}(t)$ and the Device Under Test (DUT) attached to the terminals, f_R is the frequency of the reference signal $r_R(t)$ for the analog demodulator (d), f_{IF} is the intermediate frequency, f_S is the base sampling rate of the ADC, $r_{IF,I}(n)$ and $r_{IF,Q}(n)$ are the reference signals of the digital modulators.

By considering the requirements of our application, the intermediate frequency f_{IF} has been placed at a higher value than the bandwidth of the incoming signal ($f_{IF} > BW_{(s_{RF})} = 100Hz$). Moreover, the distance between the two spectral components $f_{lo} = f_{RF} - f_R$ and $f_{hi} = f_{RF} + f_R$ has been maximized to facilitate the design of the LPF (f_R as high as possible). In order to maximize the SNR the frequency f_{IF} has been selected higher than the flicker noise corner frequency of the PGA (1kHz) and set to $f_{IF} = 1.192$kHz.

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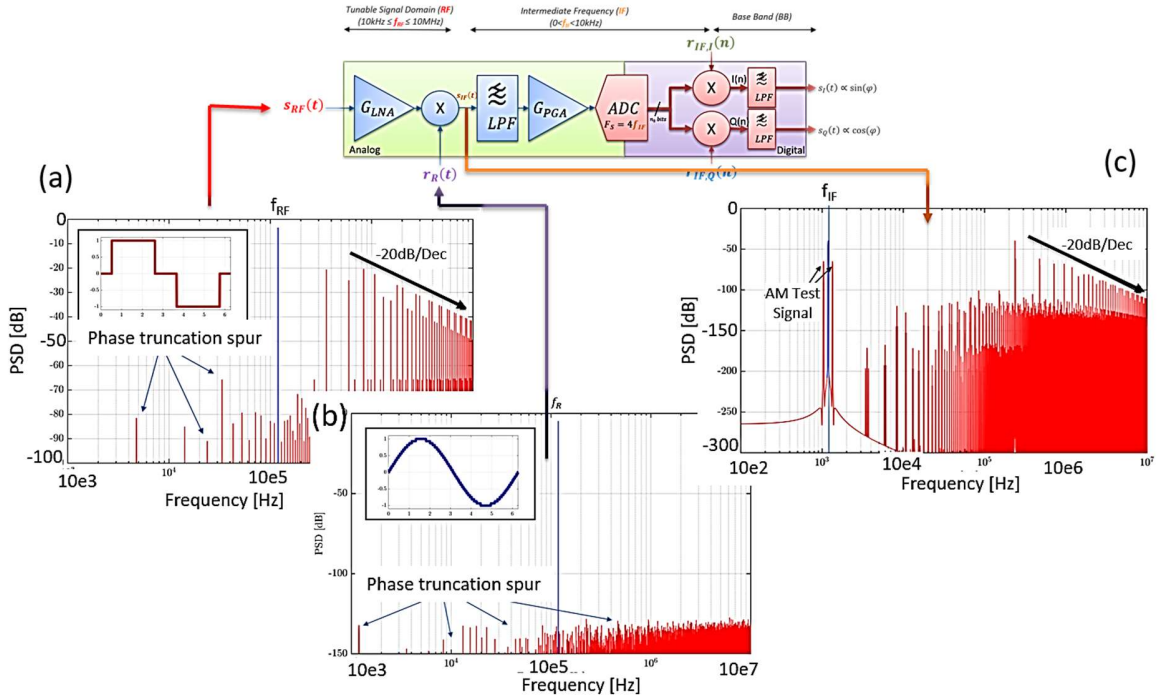

Fig. 5: PSD of the signals at different stages of the elaboration chain. (a) 3 level signal measured on the DUT, (b) PSD of the analog demodulator reference sinusoidal, (c) PSD of the demodulated signal

C. *Optimization of the excitation signal waveform*

Ideally, both signals $r_R(t)$ and $r_{RF}(t)$ should be ideal sine waves, however, two high quality synchronous sine waves generators would increase the complexity of the system. As a more effective solution we chose to replace the ideal sine wave of the $r_{RF}(t)$ signals with a sinusoid approximated by a three level signal $s_{RF}(t)$, (Fig. 5(a)) where $\pm\sin(\beta)$ are the switching thresholds between 0, 1 and 0,-1.

The development of the Fourier series of the $s_{RF}(t,\beta,\omega_0)$ function is:

$$s_{RF}(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}(a_n\cos(\omega_0 nt) + b_n\sin(\omega_0 nt)) \quad (15)$$

where $a_n = 0$ since $s_{RF}(t)$ is an odd function, and:

$$b_n = \frac{2\omega_0}{n\pi}(\cos(n\omega_0\beta) - \cos(n\pi - n\omega_0\beta) \quad (16)$$

The optimal value of β can be identified as $\beta = 1/(6f_S)$, which gives b_2=b_3=0, b_4=b_6=b_8=0 b_9=…=0 and b_5,b_7,b_{11},b_{13}≠0, proving that the first visible harmonic is the fifth. This corresponds to a significant reduction in the number of harmonics present in $r_{RF}(t)$.

IV. Model Simulation

In Fig.5(a) the Power Spectral Density (PSD) of $s_{RF}(t)$ is depicted. On the plot the 20dB/dec roll off of the signal harmonics (f_n>f_{RF}), which correlates to the 1/n term of the Fourier Series of the 3-level sinusoid, is clearly visible. At the same time, the effect of the phase truncation in the phase accumulator shows up with spurs located at frequencies below f_{RF}. On the same plot, it is possible to note the positive effect produced by the use of a β value close to 1/12 times the signal period. It is also possible to observe how the harmonics highlighted by the spectral analysis are in number and in amplitude lower than it would be with a classic square wave function.

In Fig.5(b) the PSD of the sinusoid generated by DDS is shown. The PSD is characterized by a strong signal centered at (n-1)f_{IF}. The quantization noise and the phase noise introduced by the phase accumulator are well below -86.6 dB.

In Fig.5(c) we can observe the folding effect of the demodulator on the $s_{RF}(t)$.

Fig.6(a) is the PSD of the 1-bit digital data stream of the sigma-delta modulator. Here the spurs caused by harmonics in the signal $s_{IF}(t)$ are easily recognizable and are concentrated in the noise shaping region of the modulator, and thus have no impact on the overall system performance (spurs in the noise shaping region will be suppressed together with noise in the digital decimation stage (Fig. 6(b)).

The last PSD depicted in Fig. 7(a) , highlights the frequency translation made by the digital I demodulator. Please note that the PSD of the signal at the output of the demodulator is not degraded but only mirrored around the Nyquist frequency. Low frequency noise is shifted to high frequency. With regards to the signal components at high frequencies, these are eliminated by the digital low pass filters (LP) located after the digital mixer, which makes the contribution of out of band signals negligible on the overall system accuracy.

V. Circuit Implementation

A. *Switch Matrix*

The switch matrix (SM) is an analog structure located between the chip PIN and the front-end circuits.

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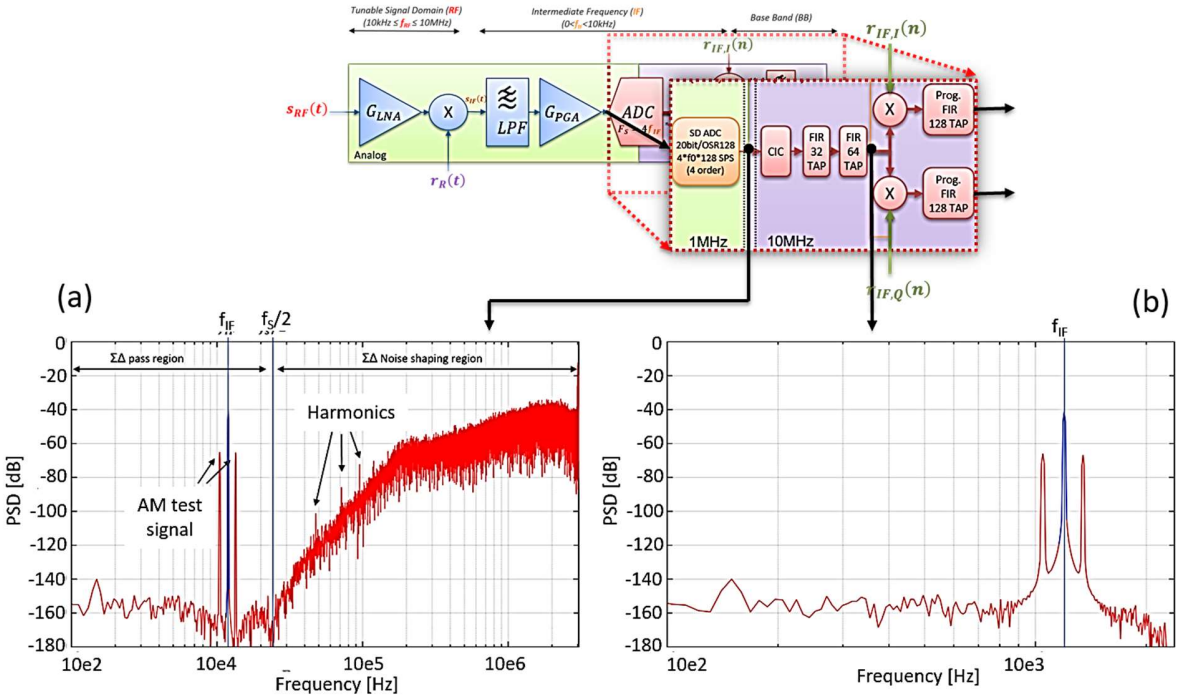

Fig. 6: ADC sampled signal (a) PSD of the 1-bit sigma delta modulator output, (b) PSD of the decimated and filtered digital signal at $4F_0$ sampling rate

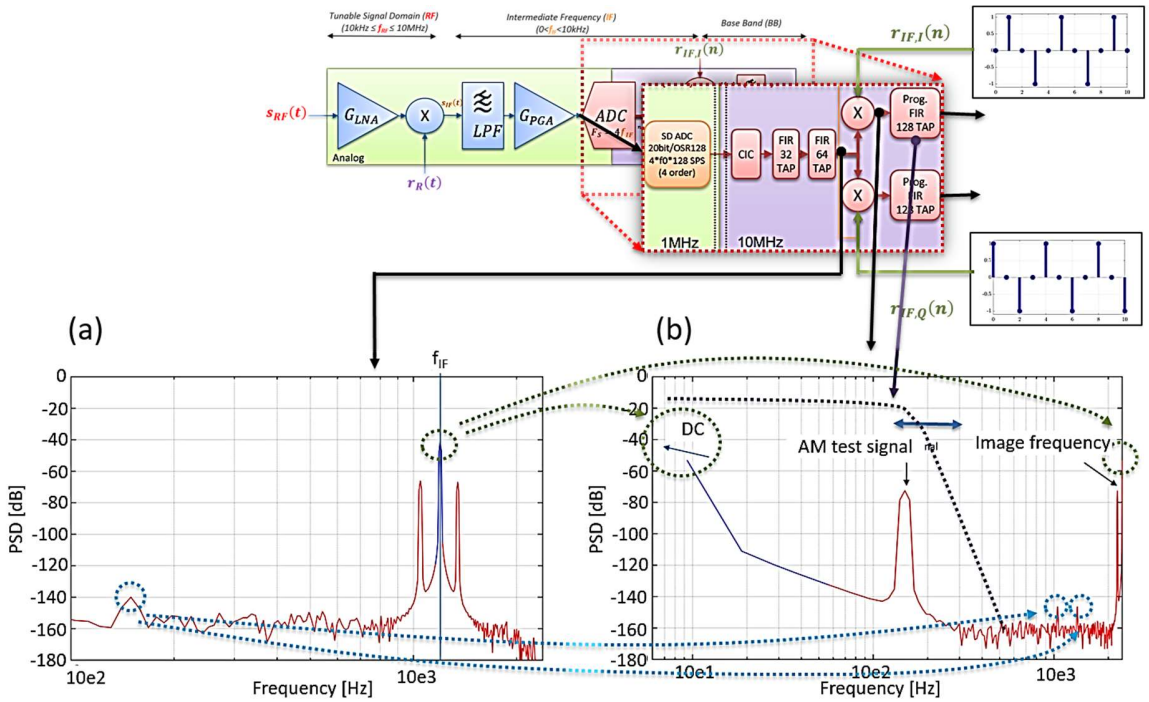

Fig. 7: Digital phase detector (a) PSD of the decimated and filtered digital signal (b) PSD of the digital demodulated signal

It allows to dynamically map the externally connected elements to the internal circuitry (current source and LNA). In particular, in order to perform correct measurements, the stimulation and the readout terminals are constantly exchanged. Furthermore, the SM is of fundamental importance for performing the auto calibration procedure of the entire measurement chain. The SM allows to connect eight possible input terminals (IO) with four function lines.

The configurability of the structure is guaranteed for each function line independently by a 4-bit binary code.

B. Low noise amplifier

Fig. 8 shows the main structure of the LNA consisting of a folded-cascode topology with two diode-connected transistors

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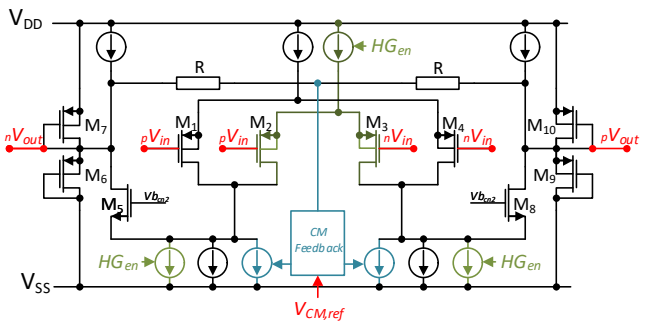

Fig. 8: Schematic of the LNA [23]

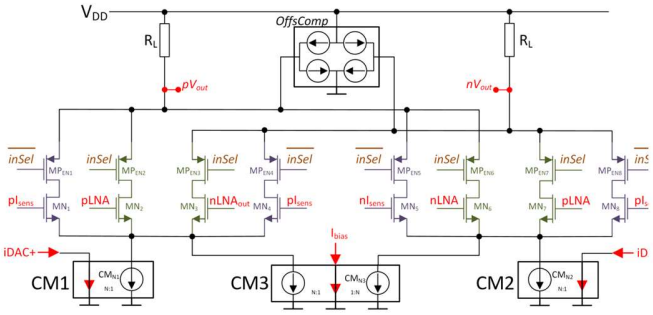

Fig. 9: Schematic of the mixer [23]

and a linearization resistor acting as a load. The differential input pair acts as a voltage controlled current source. It is implemented with P-MOS transistors (M1, M2, M3, and M4), in order to control the body voltage and to reduce both the body effect and the flicker noise contribution. The choice of a P-MOS transistor as active load is an important point for the design of an amplifier where the dependence of the gain on technology parameter changes has to be minimized. Another peculiarity of the circuit is the pair of low transconductance diode-connected transistors used as active loads (M6-M7 and M9-M10). Thanks to this configuration, the linearity of the amplifier is increased by reducing the dependence of the LNA gain on the input differential voltage. N-MOS transistors M5 and M8 allow folding the current from the input pair to the output node, thus reducing the voltage swing caused by the input signal and stabilizing the operating point of the output load.

In order to introduce an extra degree of freedom in controlling the linearity of the circuit, a resistor has been connected between the output nodes. A current controlled feedback loop has been added in order to control the output common mode voltage by directly adjusting the current in the input branch. In order to cover the 140dB of input dynamic range, the circuit has been made programmable (using the High Gain signal H_{Gen}) to reduce the gain from 40 dB to 28dB when the input signal exceeds 10mV. The input branches are, therefore, split in two parts: transistors M2 and M3 are activated in high-gain mode, while in low-gain mode M2 and M3 are deactivated, reducing the gain and increasing the noise contribution, which however allows keeping unchanged the dynamic performance, thus increasing the voltage input range up to 80mV. The circuit ensures a CMRR of 81dB at 10kHz, which increases to 84dB at 10MHz.

C. *Mixer*

The analog mixer stage (Fig. 9) has been implemented through a current steering Gilbert cell. The circuit is responsible for mixing both the LNA output signal and the signal Vsen from the 3-level current source (3LvL-CS). The choice of integrating a "double" mixer into a single structure is dictated by the need to avoid degradation of the LNA performance by placing a multiplexer in front of the mixing stage. The two signals LNAp-n and Vsenp-n are directly connected to the RF input transistors and the multiplexing function is realized through the selector inSel. The output current signal from the 14-bit-DAC is directly mirrored on the mixer through programmable current mirrors (CM1 and CM2), which allow setting the gain value. At the same time, to ensure proper operation of the structure, the bias current is adjusted (via CM3), ensuring a constant operating point. Furthermore, a programmable current source has been implemented as offset compensator (Offs Comp). This structure is directly connected to the two mixer outputs (Voutp and Voutn) to adjust the output common-mode level and to compensate for any offset arising from mismatches within the mixer structure.

D. *PGA*

The PGA and low-pass filter (LPF) blocks are realized with a chain of 3 stages. Two stages are optimized to generate an overall gain of 80dB (40dB + 40dB), while the third stage is optimized to realize the low-pass filter with cutoff frequency f_{-3dB} at 5.9kHz. Both the amplification stages and the filtering circuit are implemented with fully differential multiple feedback topology (MFB). The use of a MFB structure in each stage, although not essential, has the advantage of improving the circuit performance in terms of anti-aliasing filtering.

After the last stage gain stage, a differential unity gain buffer has been inserted. This buffer is required to drive the high input capacitive load of the ΣΔ-Modulator.

Given the large gain of the PGA, a programmable offset compensation circuit was introduced before the last amplification stage. This circuit is capable of compensating in a static manner (digitally programmable via a digital control word a possible DC offset, which could be present at the input of the last PGA gain stage. It should be noted that a possible DC component (offset) in the signal may represent a problem in terms of PGA saturation, but does not constitute a theoretical limitation to the accuracy of the measurement, which can be still carried out. Indeed, an offset in the $s_{IF}(t)$ signal would correspond to a signal at f_{IF} in demodulated digital signal. This unwanted signal is removed by the digital filters with no effect on the digital demodulated DC value.

E. *20-bit sigma-delta ADC*

The ADC is a 4th-order single-bit, single-loop, switched-capacitor ΣΔ-Modulator, with a topology incorporating both feedback and feedforward paths. To improve the stability and to ensure a flat-band around f_{IF} the transmission zeroes have been placed at DC, f_0=1.19kHz and $2 \cdot f_0$=2.38kHz. This is achieved by connecting the outputs of the first integrator and the output of second integrator to the input of the fourth

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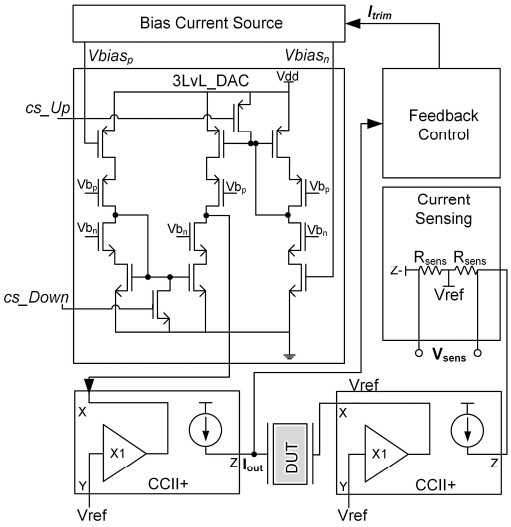

Fig. 10: Three-level current source

integrator through feed-forward paths. The feed-forward factors are both equal to 1/4. The local feedback around the first two and last two integrators form two local resonators, which allows placing a couple of complex zeroes at the desired frequency.

To ensure that the ADC noise is dominated only by the quantization noise, the integrating and sampling capacitor of the first integrator stage has been sized to C1=240pF and C2=120 pF; while the capacitors of the following integrators were kept small (few tens of picofarads), because their noise contribution is negligible on the total noise contribution. Indeed, only the noise contribution of the first integrator appears unaffected at the output of the modulator (the input noise undergoes the same transfer function as the input signal), while the noise due to other sources inside the feedback loop undergoes to the noise shaping transfer function, which makes the noise requirements for the second, third and fourth integrator less stringent than that of the first integrator.

The oversampling factor is 128, which sets the sampling frequency at $f_{s,ADC}=512 \cdot f_{IF}=610kHz$ and allows achieving the measured resolution of 96.8dB.

F. 14-bit 80MS/s DAC

The DAC, which is used to synthesize the LO signal, is a current steering DAC implemented by subdividing the bit coding in two structures: part of the bits is coded in the thermometric mode (the 12 most significant bits) and part in binary mode (the 2 least significant bits). Furthermore, in order to maintain a compact structure, the thermometric decoding section has been further divided in two sub-group of 6-bit (MSB and ISB) with the segmentation technique.

Linearity degradation has been reduced by means of a scrambler system, consisting of a butterfly randomizer which has been placed in front of the current sources. According to the analysis reported in [20] the randomization of elements transforms the mismatch error that produces tones in the output spectrum into a pseudo-noise, which improves the SFDR of the DAC.

All current sources are the parallel implementation of a single

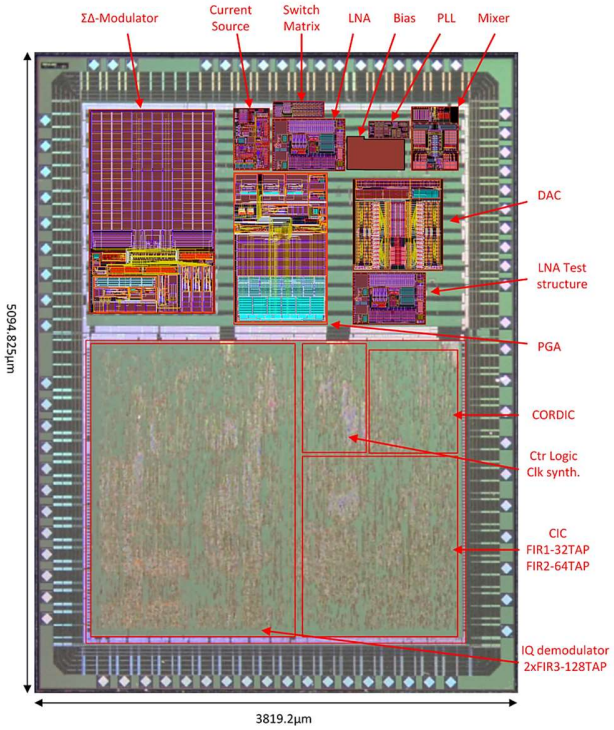

Fig. 11: Micrograph of the implemented ASIC [23]

current mirror cell composed by two cascoded P-MOS transistors, which allows increasing the output impedance. P-MOS transistors in the current cells allow achieving better shielding from substrate noise than N-MOS devices, thanks to their better isolation from the substrate. Furthermore, in order to reduce the charge-injection caused by the clock feed through, the P-MOS switches are followed by dummy switches with the scope of injecting an equal and opposite amount of charge into the channel.

The output current of the DAC is collected by a diode connected transistor, which acts as load (and is part of the current mirrors, which mirrors the DAC current into the mixer).

In order to allow changing the mixer gain, the DAC current has been made configurable through a 4-bit programmable resistor. The LSB can vary between 5.6nA and 103nA for a total current consumption between 115µA and 2.1mA.

G. Three level current source and current sensing

The 3-level current source (3LvL-CS) (Fig. 10) is the circuit responsible for the generation of the current required to stimulate the tissue (DUT). According to typical BIA and EIT specifications, the 3LvL-CS needs to be capable of generating a sine wave, approximated by a 3-levels signal, from DC up to a frequency of 10MHz.

The 3LvL-CS is composed by: a bias current source responsible for generating a symmetrical stimulus current on the DUT that is driven by the 3-level DAC through a CCII+ buffer; a second CCII+ buffer which act as current collector or virtual ground; a current sensing circuit for measuring the current through the DUT and finally a current control feedback circuit, which ensures the symmetry of the currents throughout the cycle of the signal.

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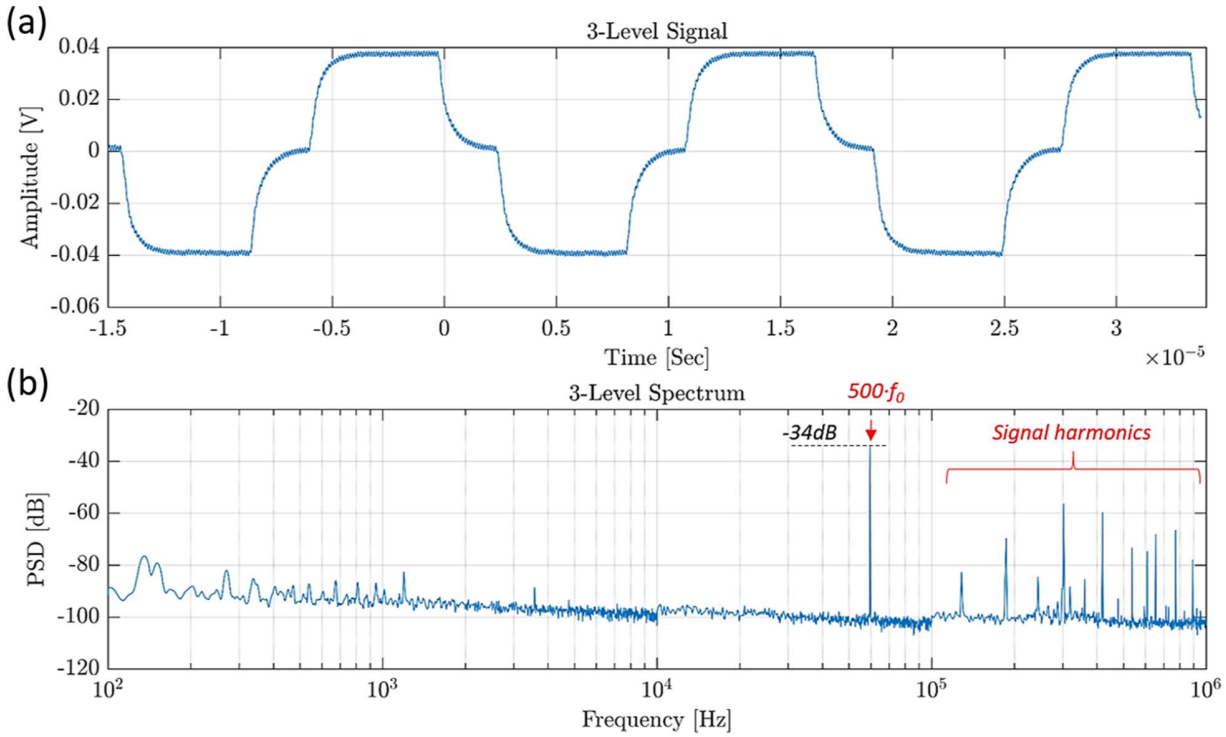

Fig. 12: LNA output (a) Time domain (b) Signal PSD

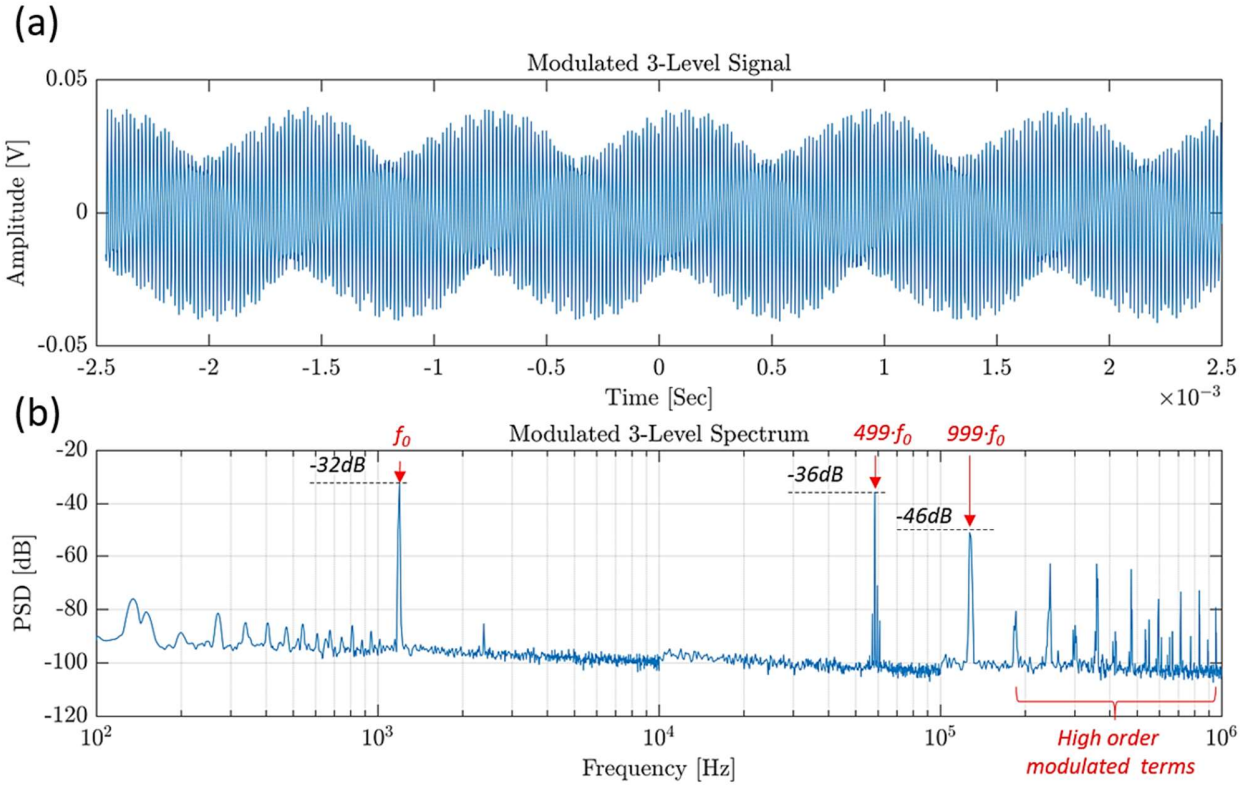

Fig. 13: Mixer Output for a 499f_0Hz demodulator reference signal (a) Time domain (b) Signal PSD

The current amplitude is programmable through the 4-bit register between two ranges: from 1µA to 15µA for the low current mode, and from 10µA to 150µA for the high current mode. The clock generator controls the timing of the 3LvL-CS through the cs-Up, cs-Down and cs-Reset signals. The cs-Up and cs-Down phases controls the I_{out} polarity alternatively

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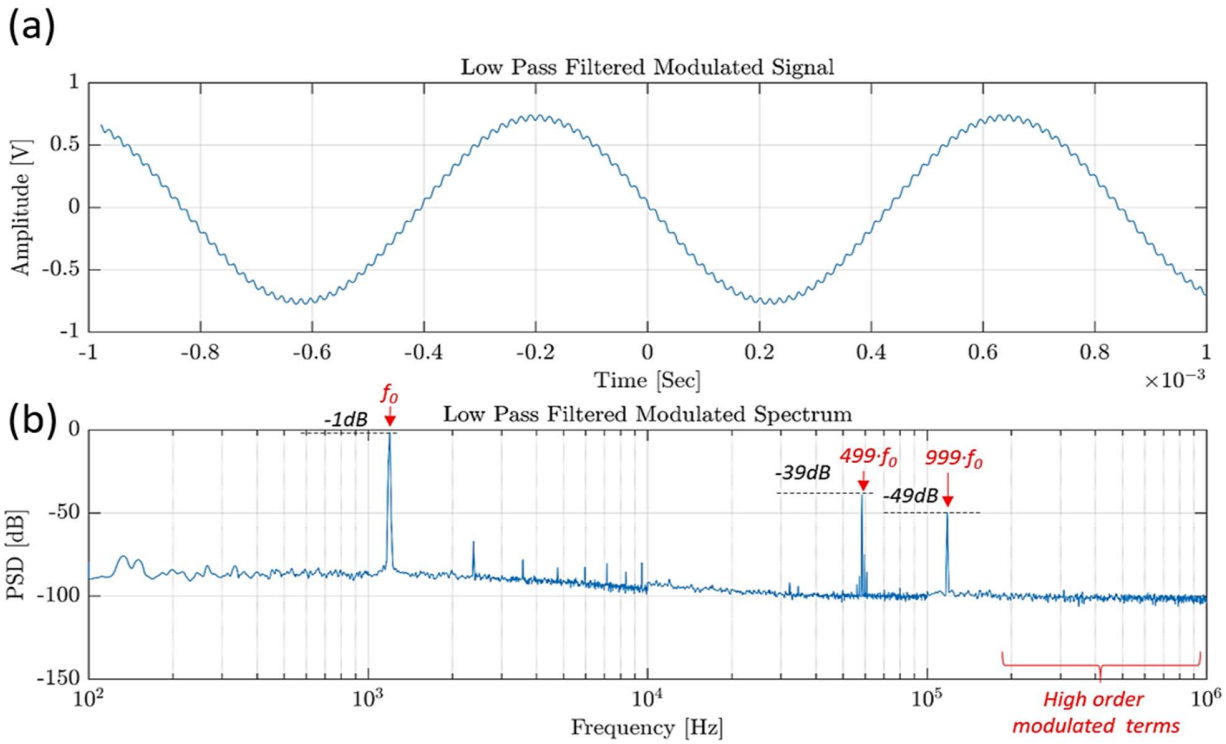

Fig. 14: PGA output (a) Time domain (b) PSD

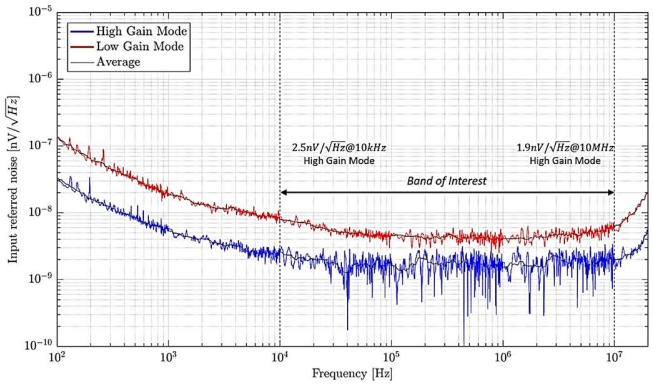

Fig. 15: LNA measured input referred noise

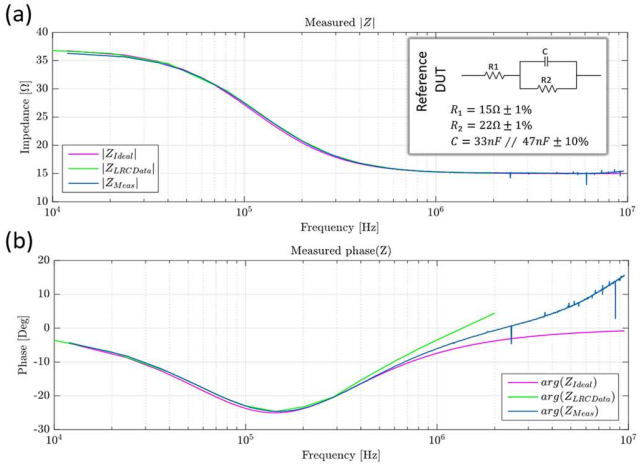

Fig.16: ASIC, LRC Meter electrical impedance measurement performance comparison (a) amplitude (b) phase [23]

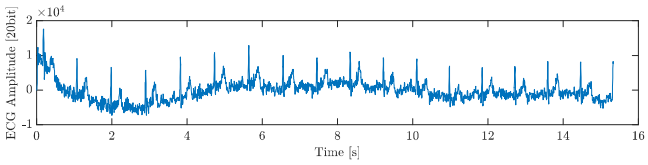

Fig. 17: ECG measurements [23]

enabling the P and N current mirrors.

Current mirrors are controlled by shorting the reference current to ground (or to V_{dd}). This approach in controlling the reference current has the advantage of minimizing (or even eliminating) any overshot in the transients.

To ensure an optimal and constant operating point for the current mirrors of the 3LvL-DAC, and, at the same time, to optimally isolate the current sources from the DUT, a current-conveyor (CCII+) structure has been implemented. The CCII+ behaves as a voltage follower between the Y terminal (current mirror output node) and the X terminal (voltage reference), and as a current follower between the X terminal and the Z terminal.

The current sense circuit has been implemented by means of a CCII+. The symmetry of the currents flowing into the DUT is ensured by the feedback control circuit, which, at the end of each cycle (0,+1,0,-1), ensures that the voltage measured at the 3LvL-DAC output node is equal to the reference voltage V_{ref}. In case of unbalancing between the currents, the feedback circuit generates a I_{trim} current compensating the unbalancing on the bias current source.

VI. Experimental Results

Fig. 11 shows a micrograph of the implemented ASIC. All circuit blocks have been fully experimentally characterized in

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terms of both functionality and performance.

Fig. 12 shows the graph of the LNA differential output signal (a) and its spectrum (b). In the upper image (a), the 3-levels (f_{RF}=500f_0) signal generated by the CS is plotted. The slow level transitions are the consequence of the limited signal bandwidth available on test PIN. PIN which, due to the parasitic capacitances and ESD protection resistances, form a low pass filter with a cutoff frequency of approximately 1MHz. In the frequency spectrum the fundamental frequency and its harmonics are easily distinguishable.

Fig. 13 shows the signal measured after the analog demodulation stage, and before the PGA amplification stage. For this measurement the DAC has been configured with a frequency of f_R=499 f_0. The spectral component (b) which can be identified at 499f_0 is the result of the product between the DC component found on the LNA signal and the DAC demodulation signal. At higher frequencies, some harmonics of the signal are visible. In particular, it has to be noted that, after the demodulation process, the harmonics around the signal at f_0 are minimal.

Fig. 14 refers to the signal measured after the PGA (PGA set at the nominal gain of 32dB). In this plot the effect of the anti-aliasing filter can be appreciated, which has greatly reduced the amplitude of the signal components located beyond the Nyquist frequency of the ΣΔ-Modulator.

Fig. 15 shows the LNA measured equivalent input noise power spectral density, which is en=2.57nV/√Hz at 10kHz in the worst case, close to the flicker noise corner frequency. It decreases to en=1.8nV/√Hz at 1MHz and en=1.9nV/√Hz at 10MHz.

In a first system validation experiment, the device has been employed to measure a reference RC network and the results have been compared with values obtained with a Keysight E4980A Precision LCR Meter (Fig. 16). The upper plot shows both the measured impedance and the expected value. The lower plot shows the corresponding phase behavior. The measured relative error between the ASIC and the LCR meter is lower than 0.8%. Measurements have been performed by stimulating the reference RC network with an excitation current of 25µA and by setting the phase detector bandwidth to 100Hz, which gives an effective impedance resolution of 1mΩ (note that with an excitation current of 150µA, it should be possible to reach the theoretical limit of 0.17mΩ).

Fig. 17 shows an example of ECG measurement, which has been carried out by setting $r_R(t)$=1, $r_{IF,Q}(t)$=1 and by using two measuring electrodes connected to the arms of a volunteer and one reference electrode connected to ground.

VII. Conclusions

We designed, implemented, and measured a new monolithic microsystem capable of (a) performing bio-impedance analysis, (b) record signals which can be used for electro impedance tomography, and (c) capture ECG traces. The device has been implemented in a commercial 0.35µm CMOS technology. Table 1 summarizes the measured performance of the proposed ASIC and compares it with the most relevant integrated circuits for impedance measurements [21, 22, 23], demonstrating that no other monolithic solution in literature allows performing BIA, EIT and ECG measurements by using the same circuit.

Specifications	H. Ko, et al. Ref [21]	S. Rodriguez, et al. Ref[22]	AD5933 Network Analyzer	This work
Measurements	BIA	BIA	Impedance	BIA, EIT, ECG
Impedance Range	0Ω … 800Ω	50Ω … 2kΩ	1kΩ … 10MΩ	1Ω … 1kΩ
Impedance Resolution	8.6 mΩ	1 Ω	244mΩ	1 mΩ
Voltage Resolution	N.A.	N.A.	N.A.	2.5 nV/√Hz
Frequency Range	250Hz…1.24MHz	2kHz…2MHz	1Hz…100kHz	10kHz …10MHz
Frequency Bandwidth	0.5Hz…100Hz	50Hz	500Hz	100 Hz (digitally configurable)
Relative error	0.26%	1%	0.5%	0.8%
Power Consumption	52 µW	298µW	125mW	100 mW
Power Supply	1.2V	1.8V	5.0V	3.3V
Silicon Area	13.8 mm^2	1.44 mm^2	N.A.	19.38 mm^2
Technology	0.13 µm CMOS	150 nm CMOS	N.A.	0.35 µm CMOS
ADC Signal Generation I/Q calculation (DSP)	12 Bits Off-Chip Off-Chip	Off-Chip Off-Chip Off-Chip	12 Bits On-Chip On-Chip	20 Bits On-Chip On-Chip

Table 1: Comparison table [23]

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