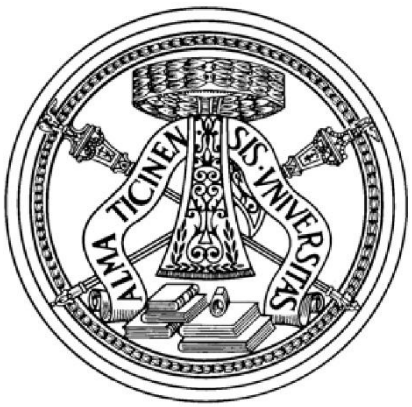

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Frequency Multipliers in SiGe BiCMOS for Local Oscillator Generation in D-band Wireless Transceivers

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Abstract

Communications at millimeter wave (mm-Wave) have drawn a lot of attention in recent years due to the wide available bandwidth which translates directly to higher data transmission capacity. Generation of the transceivers local oscillation (LO) is critical because many contrasting requirements, i.e. tuning range (TR), phase noise (PN), output power, and level of spurious tones, affect the system performance. Differently from what is commonly pursued at Radio Frequency, LO generation with a PLL embedding a VCO at the desired output frequency is not viable at mm-wave. A more promising approach consists of a PLL in the 10-20GHz range, where silicon VCOs feature the best figure of merit, followed by a frequency multiplier.

In this thesis a frequency multiplication chain is investigated to up-convert an LO signal from X-band to D-band by a multiplication factor of 12. The multiplication is done in steps of 3, 2, and 2. A sextupler chip comprises the tripler and the first doubler and the last doubler stage which upconverts the LO signal from E- to D-band is realized in a separate chip, all in a 55nm SiGe BiCMOS technology. The frequency tripler circuit is based on a novel circuit topology which yields a remarkable improvement on the suppression of the driving signal frequency at the output, compared to conventional designs exploiting transistors in class-C. The active core of the circuit approximates the transfer characteristic of a third-order polynomial that ideally produces only a third-harmonic of the input signal. Implemented in a separate break-out chip and consuming 23mW of DC power, the tripler demonstrates ~40dB suppression of the input signal and its 5th harmonic over 16% fractional bandwidth and robustness to power variation of the driving signal over a 15dB range. Including the E-band doubler, the sextupler chip achieves a peak output power of 1.7dBm at 74.4GHz and remains within 2dB variation from 70GHz to 82GHz, corresponding to 16% fractional BW. In this frequency range, the leakages of all harmonics are suppressed by more than 40dBc.

The design of the D-band doubler was aimed at delivering high output power with high efficiency and high conversion gain. Toward this end, the efficiency of a push-push pair was improved by a stacked Colpitts oscillator to boost the power conversion gain by 10dB. Moreover, the common-collector configuration keeps separate the oscillator tank from the load, allowing independent optimization of the harmonic conversion efficiency and the load impedance for maximum power delivery. The measured performance of the test chip demonstrated P_{out} up to 8dBm at 130GHz with 13dB conversion gain and 6.3% Power Added Efficiency.

Acknowledgments

I wish to thank my family before anything else because if it was not for them, I would be standing nowhere close to where I am now. I feel proud of Shiva, my wife, who stood beside me as a close friend despite all the ups and downs during our past years and I feel deeply indebted to my parents whose support for my education through all these long years was never-ending.

I can’t find the proper words to thank my supervisor professor Andrea Mazzanti for not only his deep knowledge and experience on the subject were always there to tap, but the level of his engagement in the research as a professor and his close collaboration with his students were not imaginable to me before joining the AIC Lab. Moreover, I am grateful to my colleagues for all their help, and above all, the warm and friendly atmosphere in our laboratory.

My Ph.D. research was defined within the framework of the European H2020 DREAM project. DREAM gave me an opportunity to be involved in a challenging project with a lot of room for innovations, as well as learning from the other designers of the team. The schedule of the project with the milestones planned ahead was a great help to me to keep my work organized. I am deeply grateful to the DREAM consortium for the opportunity and to the partners for the many fruitful discussions.

Infine, dopo aver trascorso più di tre anni in Italia, desidero esprimere la mia gratitudine per tutta l'ospitalità e lo spirito positivo che ho ricevuto qui. Il corso del mio dottorato nella bella Italia, rimarrà tra i miei migliori ricordi.

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List of abbreviations

LO……..…….Local Oscillation

TR…….……Tunning Range

LR……..……Locking Range

PN……Phase Noise

VCO……..……Voltage Controlled Oscillator

PLL……Phase Locked Loop

BW……Bandwidth

FBW...……Fractional Bandwidth

HRR……Harmonic Rejection Ratio

FoM……...……Figure of Merit

PPF…….……Poly Phase Filter

mm-Wave……..…….……Millimeter Wave

CS……Common Source

CD…….……Common Drain

IF……Intermediate Frequency

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Chapter 1 Introduction

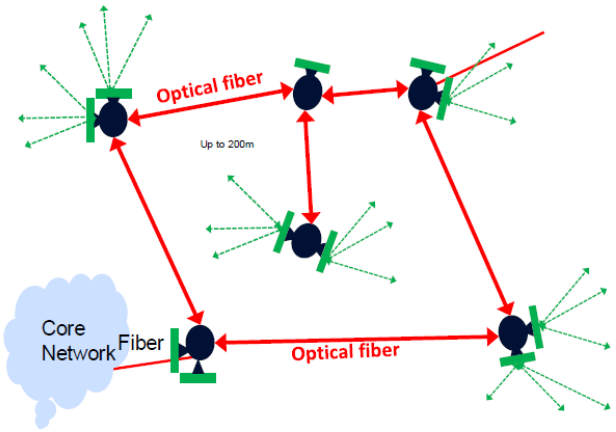
1.1 Motivation

The requirements of the envisioned 5G mobile communication necessitate pervasive access to information and data sharing at any time [1]. The increasing number of wireless devices simply implies more data traffic to be transferred by the network, in both up-links and down-links. In addition, the future mobile networks should be able to address new applications with different requirements such as machine-type communications, or the internet of things (IoT). Meanwhile, the growing share of video content in popular platforms such as YouTube and Netflix and also embedded video in social media networks increase data traffic and require higher data rates. For example, according to the 2017 Ericsson Mobility Report [2] mobile video traffic will experience an annual growth rate of 50% till 2023 and its share in the overall mobile data traffic will amount to 75%.

The mentioned growth in data traffic can only be addressed if innovative technologies enable future communication networks to handle bandwidths, data rates, and number of devices beyond the current limitations. In particular, for the mobile internet to be a reliable constitute for the wired technology, 5G networks should offer x10000 more traffic, x10-100 more devices, and higher than 10Gbps peak data rate [3].

Apart from the increased demand for higher data rate, the spatial distribution of users is another aspect of the future mobile communication networks. More than half of the world's population live in the cities. Dense urban populations are responsible for the majority of data consumption now, and will continue to play a more decisive role in the future. Therefore, increasing the capacity of the back and front hauls to meet the ever increasing demand for data traffic in densely populated urban areas is an inevitable challenge for 5G and beyond mobile networks. For this reason, mobile network operators have to meet expectations of their current users to survive in the market, and to hopefully gain new subscribers and grow their share of the market.

New network architectures have been studied to overcome the above challenges and small cells have been proposed as a promising solution. The mobile network cell size has been progressively shrinking from around 10,000ft for 2G to 1,000ft for 3G and 500ft for 4G/LTE standards. The smaller cell size allows more efficient use of the



(a)

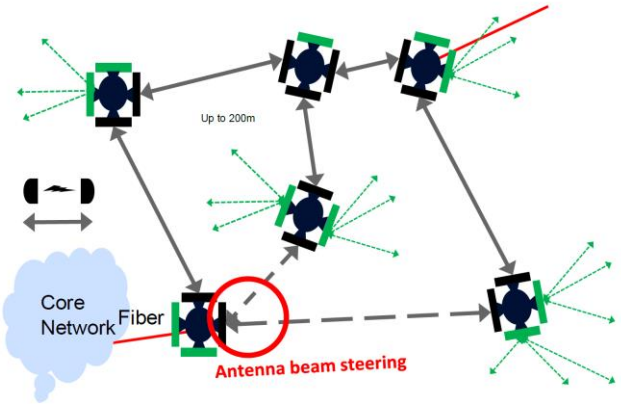


Figure 1.1. Small cell backhaul connections by (a) fibre optic, (b) seamless fibre performance wireless links [3]

available spectrum by reusing the same carrier frequency at different cells. Due to their dense deployment, however, small cells open the door to new challenges for the backhaul network such as cell edge intelligence and distributed cell control. Furthermore, the backhaul network plays a more decisive role in networks based on cloud architecture where signal processing and network management is centralized in the *core network*, since it's the backhaul network that transports data between the *access network* and the core. The backhaul network needs to meet more stringent criteria on latency and capacity as the amount of transported data grows with the amount of signal processing done in the cloud.

Heterogeneous networks (HetNets) is a solution adopted in modern communication networks where different types of cells with different access technologies are combined together. While macro cells are used to provide coverage in HetNets, micro and pico cells are used to offload the traffic to areas with high user density. Small cell

backhauling links can be implemented in a manner similar to Figure 1.1a using fiber optic wiring deployment. However, despite the many advantages of the fiber optic, its installation cost is high, and in some cases not environmentally friendly. Therefore, wireless solutions with sufficiently high data rates are required to realize a HetNet similar to the one shown in Figure 1.1b. In order to achieve a seamless operation, the performance of these wireless links should rival that of the fiber, obviously with substantially lower cost.

1.2 The DREAM[1] project

The European horizon 2020 project DREAM was defined to "research **a wireless link solution supporting data rates up to 100 Gbps covering distances of up to 300m at ultra-high carriers in the D-band frequency range**" [3]. The three companies, three research institutions, and one university that formed the DREAM consortium are VTT (Finland), STMicroelectronics (Italy and France), Nokia (Italy), CEIT and ERZIA (both from Spain), III-V Lab (France), and the University of Pavia (Italy). VTT is responsible for project management and also the design of the D-band Antenna set. System analysis and architecture was responsibility of Nokia, and ERZIA was in charge of PCB design and assembly of the final demonstrator. The design of the radio chipset was the joint responsibility of III-V Lab, CEIT, and the University of Pavia. Figure 1.2 shows the system-level architecture of the envisioned transceiver in which the role of each partner is marked. This thesis was defined within the framework of the DREAM project where the primary role of the University of Pavia was to provide **a solution for generation of a D-band local oscillation (LO) signal for the full radio.** As the transceiver will be realized with direct conversion architecture, quality of the LO signal plays a key role in the overall performance of the radio. The choice of the short millimeter wave frequencies (100-300GHz) was mainly motivated by the wide available spectrum, and also the relatively lower atmospheric and rain attenuation. Moreover, STMicroelectronics 55nm SiGe BiCMOS technology with a simulated maximum oscillation frequency (f_{max}) of 330GHz was chosen to design and fabricate all the integrated circuits. The reasons for the choice of technology were manifold. A BiCMOS process that offers f_{max} equal to a competing CMOS node, is normally based

[1] **D-Band Radio solution Enabling up to 100 Gbps reconfigurable Approach for Meshed beyond 5G networks**

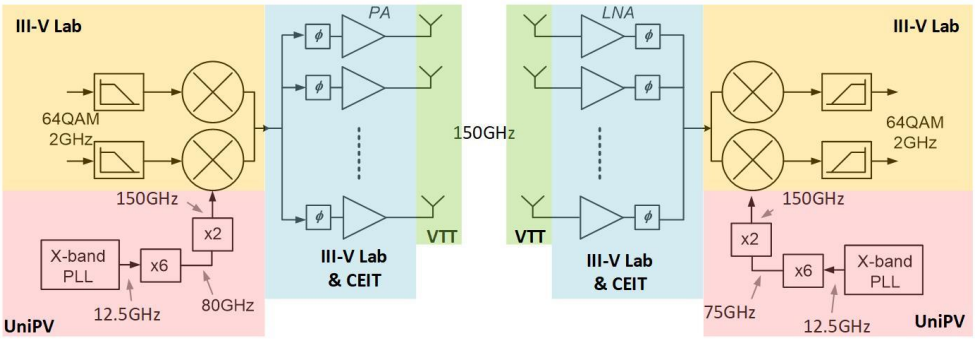


Figure 1.2. System-level architecture of the DREAM's transceiver with the role of each partner marked.

on a CMOS node at least two generations before. Therefore, with lower cost, the BiCMOS process offers better passive devices and improved metallization which directly translates to better RF/mm-Wave performance. Figure 1.3 shows the metal stack of the STMicroelectronics' BiCMOS technology featuring 8 metal layers and 1 aluminum capping layer. The 3μm thick copper layer M8, with a typical sheet resistance of 5.8 mΩ/sq and minimum allowed width of 0.6μm is normally used for signal paths and high quality inductors due to its superior conductivity and lower capacitance toward the substrate. The top aluminum capping layer is thinner (0.6μm) , has inferior properties with respect to M8, and the minimum allowed width is 3μm which makes it unsuitable for interconnections and is mainly used for distribution of the supply and ground. M6 and M7 both are 0.7μm thick with a sheet resistance of around 21mΩ/sq, and are also used to realize inductors if the quality factor is not critical. At mm-wave frequencies, inductors from a few tens of pH to a few nH have been reported with maximum quality factors between 10 to 30 [4]. Also, integrated transmission lines realized using M8 for the signal and M1 or M4 for the ground were

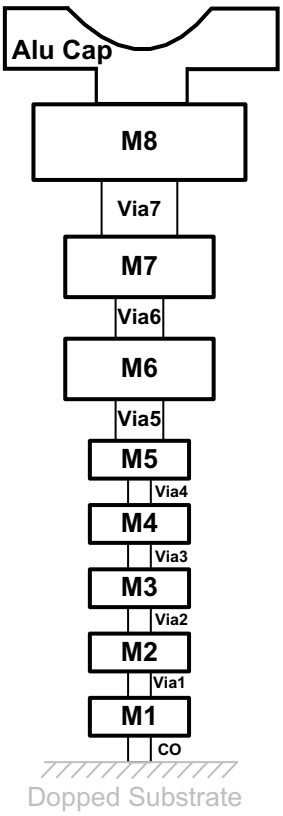


Figure 1.3. Cross section of the metal stack of the 55nm BiCMOS technology.

reported to have a measured characteristic impedance ranging between 28Ω to 87Ω if the width of M8 is 0.54μm and 16.7μm, respectively [4]. In simulations, the characteristic impedance was equal to 50Ω for a width of 8.57μm and at D-band frequencies the quality factor was in the range 25-30Ω.

M2-M5 are 0.3μm thick with a sheet resistance of 100-130mΩ/sq (depending on the width) and the sheet resistance of M1 is around 183 mΩ/sq with a thickness of 0.1μm. M1-M5 are mainly used for interconnections of active devices as the minimum allowed width is 0.1μm for M2-M5 and 0.09μm for M1.

Bipolar transistors are known for their higher transconductance, lower Flicker noise, and higher breakdown voltage compared to CMOS transistors. The latter advantage allows the use of higher supply voltages, hence higher output voltage swing and consequently higher output power without compromising reliability or exposing the transistors to parameter deterioration, as is the case of MOS transistors. Last but not the least, the provider of the BiCMOS technology, STMicroelectronics, is one of the top suppliers of analog integrated circuits in Europe, as well as the world, and its contribution to the DRAEM consortium facilitates and secures the development of mm-Wave integrated circuits in the future.

In the next section performance parameters and challenges of mm-Wave LO generation, as well as the different methods reported in the literature will be reviewed. The proposed architecture for LO generation pursued in this work will be presented in section 1.4. It will be elaborated how and why the LO chain is composed of two different chips. The first chip, a frequency sextupler will be covered in Chapter 2. The chapter begins with a review on the building blocks and architecture of the chip, then each sub-block is discussed in detail and the experimental measurement results of the whole test chip are presented in section 2.5. Chapter 3 follows almost the same flow for the second chip, i.e. begins with the design description and concludes with measurement results. Finally, Chapter 4 summarizes and concludes the thesis while an overview for the future works is presented. Appendices and references are available at the end of the text.

1.3 LO generation at mm-Wave frequencies

Generation of the transceivers local oscillation is critical because many contrasting

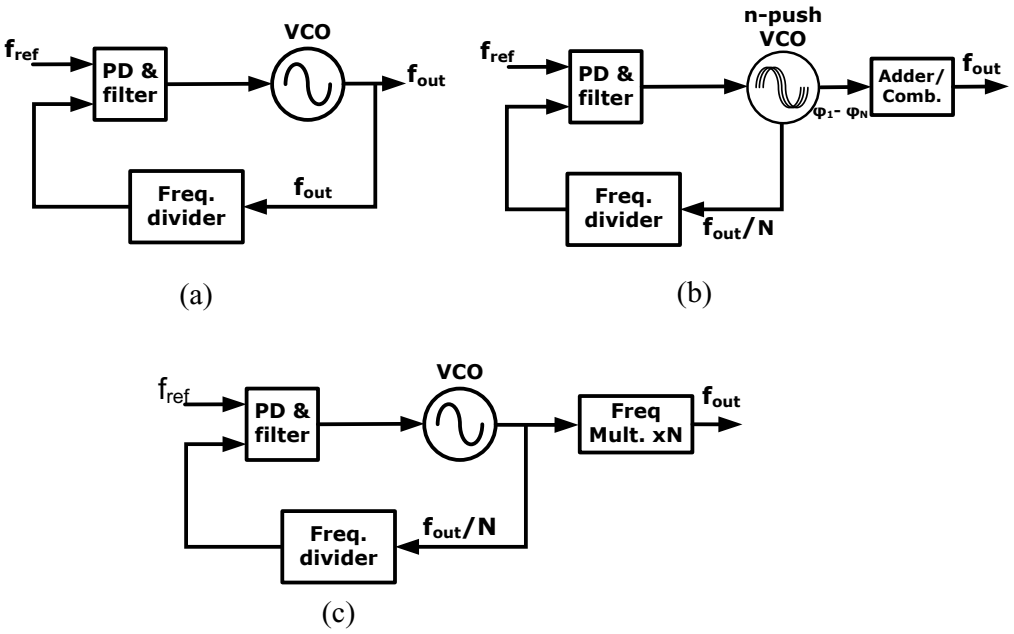


Figure 1.4. LO generation at mm-wave frequency using (a) direct synthesis, (b) n-push technique, (c) frequency multiplication

requirements, i.e. tuning range, phase noise, output power, and level of spurious tones, affect the system performance. Moreover, the power consumption of the LO generation and distribution circuits is another critical aspect, as it can make a dominant contribution to the transceiver's overall power consumption [5, 6].

Figure 1.4 shows three main solutions for LO generation at mm-Wave frequencies. Direct synthesis, as in Figure 1.4a, uses a PLL embedding a VCO at the desired output frequency. Commonly pursued at radio frequency, this solution is not suitable for mm-Wave applications because the severe impact of device parasitics in silicon technologies, and the low quality factor of passive components (mostly variable capacitors) impair the achievable Phase Noise (PN) and Tuning Range (TR). Moreover, traditional frequency dividers in the PLL need excessive power consumption. A more promising approach consists of a PLL in the 10-20GHz range, where silicon VCOs feature the best figure of merit. Figure 1.4b shows principles of the N-push technique where N synchronized oscillators work at a frequency N times lower than the output frequency, f_{out}. Designing the VCO at a lower frequency gives the advantage of higher Q of passive components resulting in a lower PN, and smaller contribution of fixed capacitors to the effective tank capacitance which results in larger tuning range. Moreover, the frequency divider running at lower speeds dissipates less power. In [7],

N-push technique is used to multiply by five, where a ring oscillator at 7.8GHz is used to generate 5 sets of equally phase-spaced differential signals. Although the multiplication factor can be increased arbitrarily in theory, the most practical challenge would be the generation of the phase shifted signals with high accuracy over a reasonably wide BW. The high output power and high spur rejection in this work were achieved at the cost of a very small BW (1.4%) and high power consumption of the ring oscillator. A similar approach called edge combining technique was used in [8] to realize a tripler. This technique could also, in theory, be extended to realize high multiplication factors. However, the need for high number of phase shifted signals still remains a big challenge. Note that in both of these works the phase-shifted signals are generated by ring oscillators, thus the number of stages need to increase with the number of required phase-shifted signals. In addition to the normally low oscillation frequency of ring oscillators which also decreases with increasing the number of stages, their implementation in BiCMOS technology results in a more power hungry circuit than in CMOS due to the absence of complementary devices.

An alternative approach is using a VCO at low frequency followed by a frequency multiplier, as show in Figure 1.4c. The main challenges in designing frequency multipliers are their DC to RF power conversion efficiency, achieving wide bandwidth, and spectral purity of the output tone. Regarding the latter, frequency multipliers normally benefit from nonlinear characteristic of components to generate higher harmonics of the driving signal, hence the output tone may be polluted with the driving tone and other undesired harmonics. Good suppression of the undesired harmonics is mandatory not to impair the transceiver performance, particularly with high-order modulations [9].

In order to achieve mm-Wave frequency using a signal source at Ku-band, a high multiplication factor is required. Injection locking technique [10] was used in [11] to achieve high multiplication factors (13-15). A frequency tracking loop was used in this work to tune the digitally controlled oscillator's free running frequency very close to the target frequency as the injection signals were very weak and the locking range was very small. Although the achieved BW of 12% around 30GHz was reasonable, the high complexity can be a challenge when targeting higher operation frequencies and impair the solution's robustness.

A more robust approach is cascading several multiplication stages of factors between 2 to 5. Three push-push doubler stages were cascaded in [12] to realize an octupler in SiGe technology. A fractional BW of 40% around 70GHz and 40dBc harmonic suppression was achieved using five stages of filtering and consuming 410mW of DC power. In [13] two frequency triplers were cascaded to implement a frequency multiplier by 9, where both stages were composed of common source (CS) transistors biased in class-C. Featuring 12% fractional BW around 94GHz and 31dBc suppression of spurious tones, the frequency multiplier requires 14dBm input power and consumes 438mW of DC power. Sextuplers have also been realized by cascading multiplication stages. High output power and 21.5% fractional BW around 93GHz were achieved in [14] by cascading a tripler, based on CS transistors biased in class-C, and a doubler in push-push topology. Consuming 470mW power and three filtering stages with orders of 5, 5 and 6, and a large area of 4.5mm^2, spurious tones were suppressed by 18dBc. The sextupler in [15] uses similar topologies for harmonic generators with smaller area, lower power consumption, and higher harmonic suppression of 39dBc, but at the cost of less than 2% fractional BW around 77.4GHz.

Comparison of the different methods to design frequency multipliers with high multiplication factors reveals that cascading multiplication stages results in lower complexity, hence more robustness compared to other methods and is more suited to high frequency operation. However, there are several trade-offs between BW, power consumption, and chip area on the one side, and harmonic suppression on the other side. Meanwhile, sensitivities to bias voltage or input power level appear as challenges to these otherwise robust circuits.

In this work, a frequency multiplication chain of 12, up-converting the LO signal from 12.5GHz to 150GHz, was designed and implemented. All designs were done using STMicroelectronics' 55nm SiGe BiCMOS technology in three tape-out runs. Experimental tests were carried out on the test chips and their performances were characterized, and compared to simulation results. Innovative ideas have been used in the design of each building block, resulting in superior performance of the test chips compared to other works reported in the literature or available on the market. The overall architecture of the multiplier chain is discussed in the next section, and details of the design will be covered in the following chapters.

1.4 Proposed LO generation architecture

The overall architecture of the LO chain is shown in Figure 1.5. The proposed architecture allows to generate a precise and accurately tunable oscillation at X-band using conventional frequency synthesis methods such as PLLs, and then to up-convert it to D-band. The alternative method, which is designing a PLL directly at D-band, would be too cumbersome for several reasons such as low quality factor (Q factor) of passive elements at high frequency, excess contribution of PN from the low frequency reference, and excessive power consumption of the frequency division block in PLLs. Therefore, the idea of generating the LO at X-band and then up-converting to D-band is implemented.

Output of the X-band LO, single ended, is fed to the designed frequency multiplier by 6 (FMX6) which constitutes a single chip. Output of the second chip, at E-band, has a center frequency of 75GHz. This output is in turn fed to a third chip whose first block is the D-band frequency doubler which in turn rises the local oscillation frequency to 150GHz. This doubler is followed by a phase shifter, mixer etc. which are out of the scope of this thesis.

The frequency synthesis architecture, split in two different chips, is conceived to meet system level specifications while minimizing risks or the DREAM project's success, and to increase testing and debug flexibility. Propagation of signals off-chip at D-band is extremely critical. Therefore, the last doubler of the LO-chain will be finally implemented on the same chip hosting the D-band up-/dn-converters. The FMX6 multiplier, with output in E-band (75GHz center frequency) is implemented as a separate chip allowing to simplify test of the D-band up-/dn- converters by using an E-band laboratory signal source. Finally, the X-band PLL chip can be easily replaced by an instrument, not compromising all the tests of the DREAM project's demonstrator in case of PLL issues, and allowing to test the radio link performance with an ultra-clean

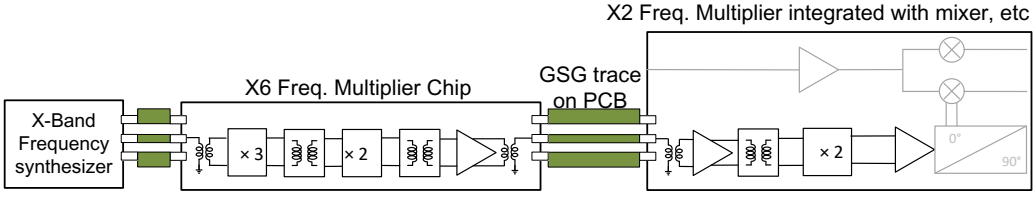


Figure 1.5. The proposed LO chain to upconvert an X-band source to D-band

(low phase noise and spurs) instrument-like synthesized signal.

In Figure 1.5 the connection between FMX6 and the next chip is done single ended for three main reasons: First, if realized differentially, then the input of the next chip had to be differential too. Consequently, it would be necessary to provide a differential input source at E-band to test the next chip, which is not available. Second, differential probes are limited to 60GHz, so differential testing is not feasible. Third, the connection between the two chips is realized with PCB traces, and implementing the transition in single ended is easier and safer. Otherwise, matching of the two routes of a differential E-band signal on PCB traces could be an issue.

Table 1.1 gives some of the most important expected performance parameters of the LO chain at D, E, an X bands. Note that the noise performance at X-band is derived from D-band using the theoretical 20log(N) formula, where N is the frequency multiplication factor [16].

Looking at specifications for the X-band PLL characteristics, an analysis of commercial products available in silicon technology reveals that there is already on the market a suitable device. The StuW81300 [17], produced by STMicroelectronics, is a good candidate to be used for frequency synthesis at X-band. Adoption of this component reduces design risk. Some of the most important performance characteristics of this product are summarized in Table 1.2.

It is worth to mention that at the time this project started, no similar devices in silicon technology were available on the market. The device that most closely matches the specifications is the HMC1101, produced by Analog Devices. But it is realized in very expensive compound semiconductor technology and the performance does not fully

Table 1.1. Expected performance of the proposed LO chain at D, E, and X bands

	Expected @ D-band	**Expected @ E-band**	**Expected @ X-band**
Frequency Range	140-160GHz	70-80GHz	11.66-13.33GHz
Power	0dBm	0dBm	0dBm
Integer Spur level	<-30 dBc *	-36dBc*	--
PN @ 1MHz offset **Noise Floor**	-96 (dBc/Hz) -140 dBc/Hz	-102 (dBc/Hz) -146dBc/Hz	-117.6 (dBc/Hz) -161.6 dBc/Hz

*Since it is difficult to define a minimum level of spur rejection required at D-band, a definitive number has not been set.

Table 1.2. Characteristics of StuW81300 commercial PLL

	StuW81300	DREAM spec. @ X band
Output power	+4dBm single ended	> 0dBm
Reference Spur	>20dB	--
PN @ 1MHz offset	-125 (dBc/Hz)	-117.6 dBc/Hz
Frequency Range	7.7-16GHz	11.66 -13.33GHz
Supply voltage	3-5.4V	--

meet DREAM targets in terms of covered frequency and spurs level.

1.4.1 X-band phase locked loop

The StuW81300 is considered as the X-band synthesizer in the LO generation chain. It is a commercial frequency synthesizer from ST Microelectronics, realized in silicon BiCMOS technology. The simplified block diagram is shown in Figure 1.6. The output of this PLL has a frequency range of 1.925-16GHz and uses two RF outputs to cover this range. The lower RF_{out} in Figure 1.6 generates oscillation between 1.925GHz and 8GHz. If desired by the user, the on-chip frequency doubler connected to the upper

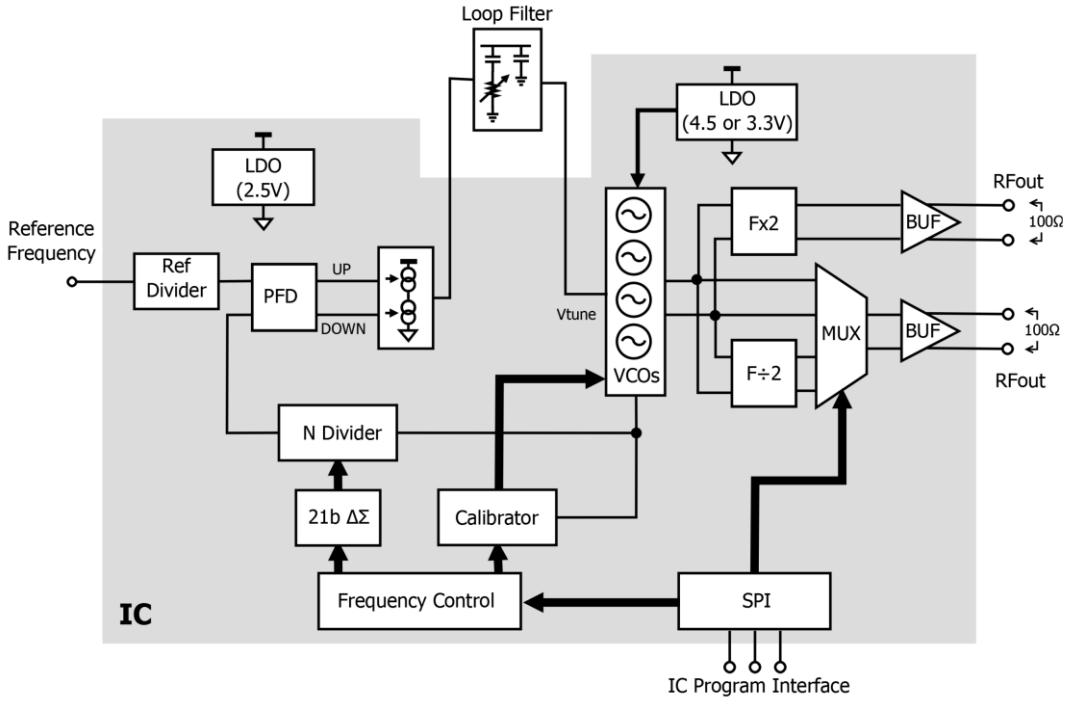


Figure 1.6. simplified block diagram of StuW81300 frequency synthesizer

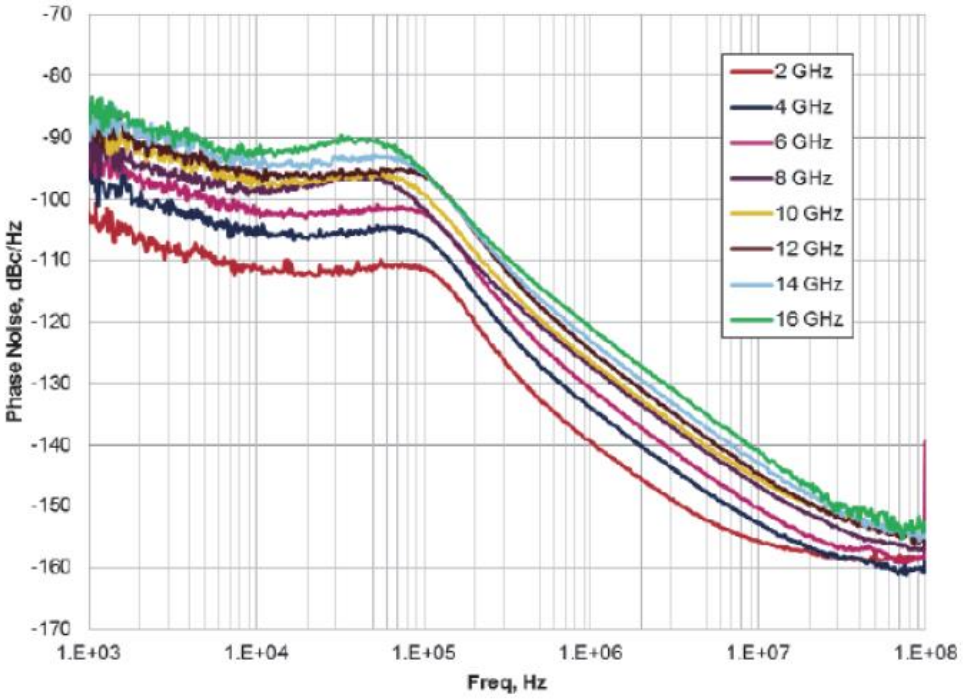


Figure 1.7. Phase noise performance of StuW81300 frequency synthesizer

RF_{out} can be used to up-convert this frequency and cover up to 16GHz. For this RF output, both differential and single ended operation is supported which suits our needs.

According to Figure 1.7, at 12GHz (the closest one to the DREAM center frequency reported to X-band, 12.5GHz), the PLL features a PN of -125dBc/Hz at an offset of 1MHz. Considering the multiplication factor of 12 to reach D-band, and assuming sufficiently low PN introduced by the frequency multiplication chain, the phase noise should be -103dBc/Hz at 1MHz offset from the D-band carrier. According to Table 1.1, the required phase noise is more relaxed, i.e. -96dBc/Hz. The noise floor merits a special discussion. The far-out phase noise target of DREAM is -140dBc/Hz at D-band. This spec is derived as a reasonable number, but not key to reach the target data-rate and link coverage. The phase noise floor reported at X-band for the StuW81300 is -161.6dBc/Hz. From simulations, standard oscillator topologies in silicon can meet this requirement. But measuring this very low noise level is difficult, requiring a suitable spectrum analyzer or phase noise meter with very wide dynamic range. From measurements reported on the StuW81300 datasheet the noise floor at 12GHz is -156dBc/Hz, 5.6 dB higher than the target. On the other hand, this measurement is very likely limited by the noise floor set by the measurement equipment. Moreover, it should be noted that the DREAM frequency synthesis chain in Figure 1.5 allows bypass or

easy replacement of the X-band synthesizer in case the StuW81300 misses some critical specification.

Chapter 2 E-band Frequency multiplier by 6

Figure 2.1 shows the architecture of the proposed frequency multiplier by 6 which is composed of a frequency tripler, a doubler, and an output buffer. In section 2.1 the most basic circuit techniques for frequency multiplication is explained followed by a review of the previous works. Based on the practical specifications of the frequency multiplier circuits, an analysis is presented in section 2.2 on the most optimum order for the multiplication stages in the chain to achieve the lowest levels of spurs at the output. Section 2.3 begins with a detailed description of the operation principles of the proposed tripler circuit. Then the details of the actual implementation are presented. The tripler circuit was fabricated as a separate break-out chip and its performance was experimentally characterized. Measurement results of this break-out conclude section 2.3. Design of the next stages, the frequency doubler and the buffer are covered in section 2.4, and the measurement results of the full sextupler chip in section 2.5 conclude this chapter.

2.1 Circuit techniques for frequency multiplication

The most common method to generate higher harmonics of a driving signal is by using a transistor biased in class-B/C, as shown in Figure 2.2a. For frequency multiplication by N, the LC load is tuned to a center frequency of Nf_0 (being f_0 the input signal frequency). The -3dB bandwidth is inversely proportional to the filter quality factor: $BW_{-3dB}=1/Q$. The harmonic content of the transistor current, I_{out}, is set by the conduction angle, θ, determined by the bias voltage V_{bias}. To gain insight, the top plot in Figure 2.2d reports the simulated fundamental, 2nd, and 3rd order currents (I_{f0}, I_{2f0}, and I_{3f0} respectively), normalized to transistor area, as a function of estimated θ. The total harmonic rejection ratio (HRR) is dominated by I_{f0}, i.e. the leakage of the driving signal, which is always larger than $I_{2f0,3f0}$, as evident also from the bottom plot showing the ratio I_{f0}/I_{2f0} and I_{f0}/I_{3f0}. The optimum conduction angle for the desired

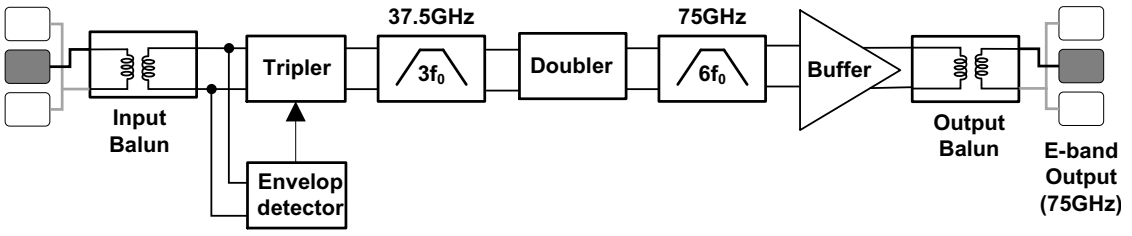


Figure 2.1. Block diagram of the frequency multiplier by 6 chain

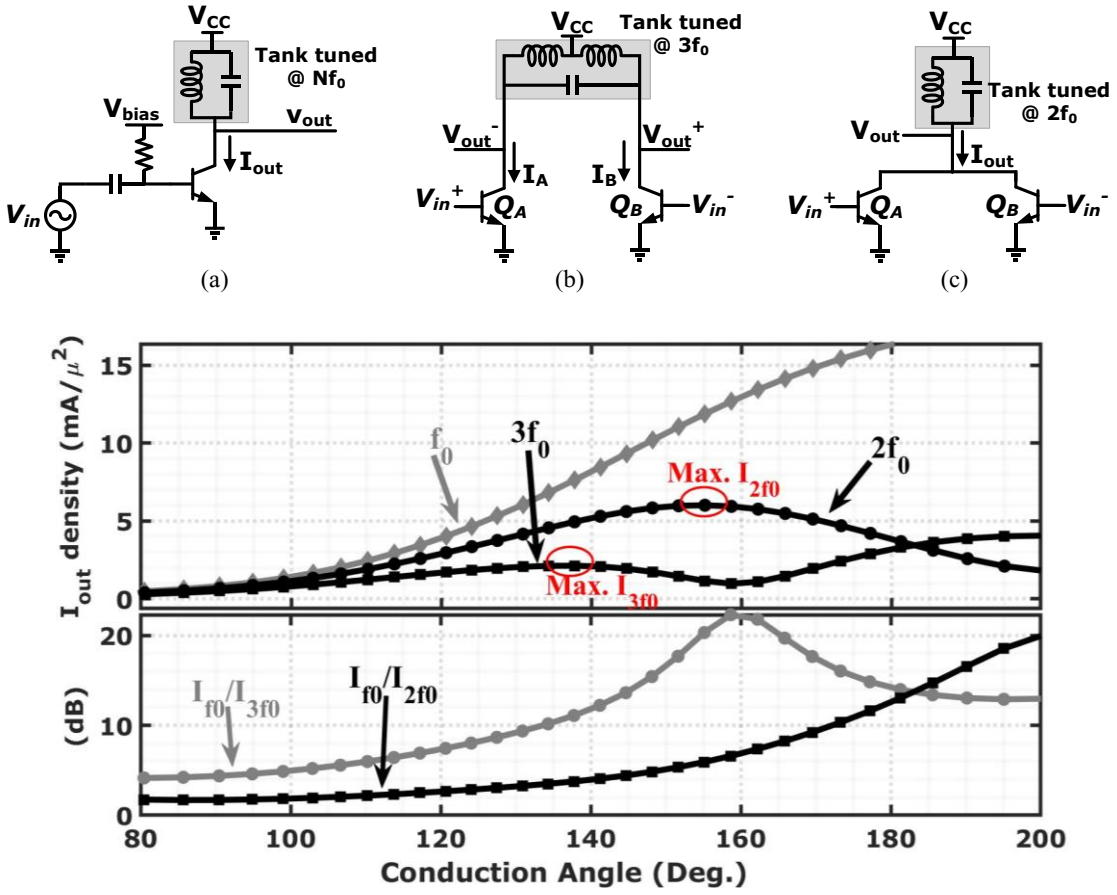


Figure 2.2. (a) Single BJT biased in class-B/C as a harmonic generator, (b) Differential version for odd-order multipliers, (c) Differential version for even-order multipliers (push-push), (d) Harmonics of I_{out}

harmonic can be selected based on the required harmonic rejection and the desired harmonic power. For example, in case of a tripler, θ≈140° maximizes I_{3f0} and hence the tripler output amplitude but I_{f0} is 10dB larger than I_{3f0} (bottom plot). Targeting a bandwidth of 15% (Q=6.7) the rejection of I_{f0} from the LC load is 20log(3)+20log(Q)=26dB, leading to HRR=26-10=16dB only on the tripler output voltage (V_{out}). Looking again at the plots in Figure 2.2d, I_{f0}/I_{3f0} is minimized (from 10dB to 4dB) at lower θ. This improves HRR by 6dB, from 16dB to 22dB. However, I_{3fo} at θ≈80° is roughly 7 times lower than at θ≈140°. Therefore, the mild improvement of HRR comes at the price of 17dB output amplitude reduction. A similar conclusion can be drawn for the case of a doubler. That is, HRR can be mildly improved at the price of significant reduction of the desired tone's amplitude. In summary, despite its simplicity, the class-B/C multiplier suffers from very poor suppression of the driving signal. This can be improved, in principle, by using a more complex filter topology or by cascading multiple filtering stages, but at the cost of design complexity, bandwidth limitation and power

penalty.

As shown in Figure 2.2b and c, the conventional class-B/C harmonic generators can be improved to realize balanced topologies. The odd harmonics of the input signal in I_A and I_B are out of phase, following $V_{in}^{\pm}$, whereas the even harmonics are in phase. Therefore, the even harmonics of $I_{A,B}$ in Figure 2.2b appear as common mode to the differential load and do not appear in the differential output. In the push-push topology of Figure 2.2c however, the odd harmonics cancel each other out before loading the tank while the even harmonics add constructively.

A frequency doubler is presented in [18] where an optimally biased and spaced array of transistors are used in common-source (CS) configuration. Use of transmission lines for matching and spacing the transistors has resulted in 12.3% fractional BW in W-band and 23dBc suppression of the driving signal. A good example of the push-push topology is presented in [19] where 58% fractional BW from 22-40GHz is achieved and the driving signal is suppressed by 30dBc. Note that, ideally, there should be no fundamental component introduced by a balanced doubler. However, the fundamental tone is always present due to device/balun mismatch and capacitive coupling, and this is normally the dominant spurious tone [19, 20]. Therefore, f_0 is usually present and around 20-30dB lower than the main tone at the doubler's output, and we shall see its significance in section 2.2.

Alternative techniques to implement even-order frequency multipliers are mixing and waveform shaping. Gilbert cell was used in [21-23] to mix a signal with itself to generate an output at the double frequency. In [22] it is demonstrated that the output power of the Gilbert cell can be maximized if the correct amount of phase shift is introduced between the two copies of the input signal. While delivering excellent results in Ka-band, application of this method at E-and D-band seems challenging as the passive components used in the phase shift network grow too small and the parasitic capacitances of the transistors play a more important role. Transistor multiport waveform shaping was used in [24] to design an efficient and highly wide BW doubler with intrinsic suppression of the 4^{th} harmonic, although a high input power of 11dBm is required.

Frequency triplers based on topologies depicted in Figure 2.2a and b are widely reported in the literature while many of them use injection locking technique to improve harmonic rejection and signal power. However, in any case the total harmonic rejection ratio (HRR) is typically around 20dB [25, 26], dominated by leakage of the driving signal, with some

exceptions reaching 30dB [27-29]. The suppression of the driving signal could be improved by rising the filter selectivity, but at the cost of larger power consumption or bandwidth limitation [30].

Mixing is another alternative approach to realize odd-order frequency multipliers. In [31] a push-push pair generates a current at twice the input frequency, which is used as the tail current of a differential pair switched by the driving signal. The two sets of differential signals applied to the push-push pair and the differential pair are in quadrature and provided by a poly phase filter (PPF). The tripler achieves a wide BW of 44% but rejection of the driving signal is limited to 20dBc due to the phase error in the PPF. A different and more promising approach to realize a frequency tripler (or potentially multipliers with higher factors) is waveform shaping. In [32] two oscillators are quadrature coupled in a ring structure. They are injected by class-C CS devices driven by four 90° spaced signals at f_0, generated by a PPF. Similar to the previous work, the harmonic rejection and BW of this structure was limited mainly due to the phase error of the PPF.

2.2 Order of frequency multiplication stages

The proposed frequency sextupler is shown in Figure 2.1. When frequency multipliers are cascaded, intermodulation of each stage folds the harmonics from the previous stage and creates new harmonic tones at the output. For example, in a case where a tripler precedes a doubler, the component at f_0 leaked into the tripler's output can get mixed with the main component at $3f_0$ and generate a tone at $4f_0$. This issue is critical as these tones can be very close to the desired tone and difficult to be filtered out. Therefore, an important consideration to be taken into account is to arrange the order of the multiplication stages such that the spurious tones from the intermodulation stay as far as possible from the main tone. In case of a frequency sextupler, there are two possibilities: *Tripler first* and *Doubler first*. Before discussing the two cases, we need to characterize both multipliers in terms of their harmonic rejection. Assuming the input to be of the form $x = \cos(\omega_0 t)$ and that the doubler is balanced and memoryless, i.e. it does not generate odd-order harmonics and the operation frequency is low enough, its output can be approximated by the following polynomial:

$$y = \frac{1}{2\rho}\, x + x^2 \qquad (2.1)$$

Where ρ is the doubler's suppression of the tone at f_0 with respect to $2f_0$. Note that the first term of the polynomial is included despite the assumption of a balanced topology for the reason

discussed in section 2.1. Similarly, assuming the same input and that the tripler is balanced, the tripler's output can be approximated by the following polynomial:

$$w = \frac{1-3\gamma}{4\gamma}\, x + x^3 \qquad (2.2)$$

Where γ is the tripler's suppression of the tone at f_0 with respect to $3f_0$.

A. Doubler First:

When the doubler is the first block in the chain, its input is a single tone at ω_0. Therefore, using (2.1) and omitting the DC component, its output can be approximated by:

$$y \cong \frac{1}{\rho}\,\mathrm{Cos}(\omega_0 t) + \mathrm{Cos}(2\omega_0 t) \qquad (2.3)$$

The doubler's output is then fed to a tripler. In this case, the tripler's output can be obtained by substituting (2.3) in (2.2). Keeping only the tones closest to the desired tone $(6\omega_0 t)$, the output will be:

$$w \cong \frac{3}{\rho^2}\,\mathrm{Cos}(4\omega_0 t) + \frac{3}{\rho}\,\mathrm{Cos}(5\omega_0 t) + \mathrm{Cos}(6\omega_0 t) \qquad (2.4)$$

As the 5th harmonic is the closest tone to 6th harmonic, thus is the most important one, we focus our attention to it. Assuming $\rho = 30$, which is aligned with practical values reported in the literature, results in around 20dBc suppression of the 5th harmonic.

B. Tripler first:

Following the same approach as in the previous case, the normalized output of a balanced tripler excited by a single tone at ω_0 can be approximated by using (2.2):

$$y = \frac{1}{\gamma}\,\mathrm{Cos}(\omega_0 t) + \mathrm{Cos}(3\omega_0 t) \qquad (2.5)$$

The tripler's output is then fed to a doubler. In this case, the doubler's output can be obtained by substituting (2.5) in (2.1). Keeping only the tones closest to the desired tone $(6\omega_0 t)$, the output will be:

$$w \cong \frac{\gamma}{2}\,\mathrm{Cos}(4\omega_0 t) + 0 \times \mathrm{Cos}(5\omega_0 t) + \mathrm{Cos}(6\omega_0 t) \qquad (2.6)$$

Comparing (2.6) and (2.3) leads us to an important result: in the *tripler first* case the 5th harmonic disappears. This is an important difference because due to the small spectral distance

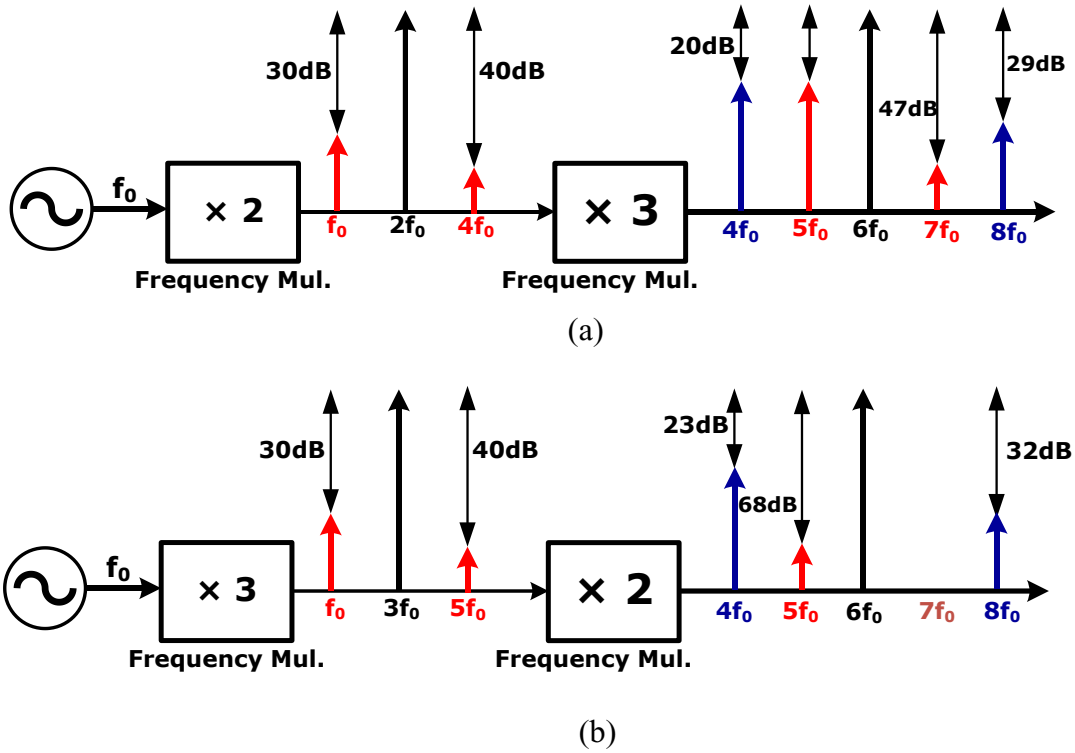


Figure 2.3. Conceptual diagram to show effect of multipliers' order on output spurs. (a) Doubler first, (b) Tripler first.

to the desired tone, it's very difficult to filter the 5th harmonic in the output.

The above analyses were based on approximating the two multipliers with (2.1) and (2.2), in both of which only two nonlinearity terms were included. A more reliable analysis can be done by using more terms in the polynomials. Therefore, a similar analysis as above was done including the 4th and the 5th harmonics for the doubler and tripler, respectively. Also a realistic scenario was considered by assuming that the 4th and 5th harmonics were 10dB lower than the fundamental in (2.1) and (2.2), respectively. Figure 2.3 shows a graphical representation of the outcome and the analysis is provided in Appendix I for reference. Note that the 4th and 8th harmonics are almost equally suppressed in both cases. However, in the *tripler first* case (Figure 2.3b) there is 48dB more suppression of the 5th harmonic and the 7th harmonic disappears completely.

Another important observation that can be made from the above analysis is the effect of harmonic rejection levels of the first and second blocks on the overall harmonic rejection of the multiplier chain. By assigning different values to γ and ρ in either of the two cases, it is observed that the first block has always a more dominant role. For example in the *tripler first*

case, $\gamma = 20$ and $\rho = 40$ results in 19.6 and 25.5dBc suppression of the 4th and 6th harmonics, respectively, whereas $\gamma = 40$ and $\rho = 20$ results in 25.5 and 34.5dBc suppressions. Therefore, it can be concluded that harmonic rejection of the first block plays a more critical role on the overall harmonic rejection of the multiplier chain: as in [12, 33] the multiplier stages with higher harmonic rejections are placed early in the multiplication chain and those with inferior harmonic rejection performances are used as the last stages.

2.3 Proposed frequency tripler with 37.5GHz output frequency

2.3.1 Principle of operation

Assuming a sinusoidal driving voltage, $V_{in}(t)=Asin(2\pi f_0 t)$, the active core of an ideal tripler generates current only at the 3rd harmonic if the trans-characteristic follows the 3rd order polynomial:

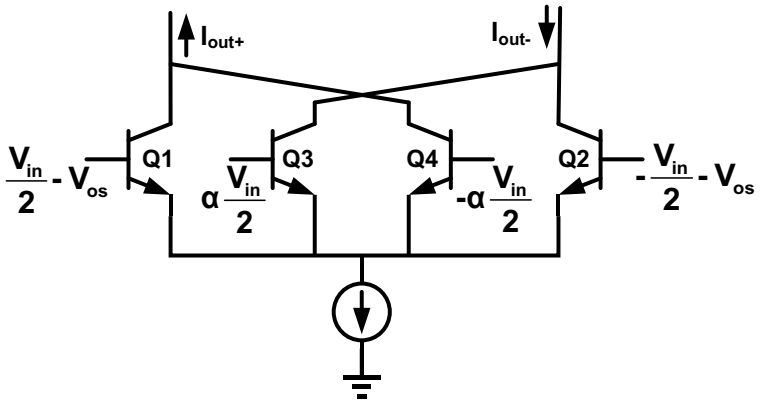
$$I_{out} = \left(\frac{3}{A} v_{in} - \frac{4}{A^3} v_{in}^3\right) g_m \qquad (2.7)$$

Figure 2.4a shows the proposed circuit schematic to approximate (2.7) while the ideal and transistors trans-characteristics are plotted in Figure 2.4b. $Q_{3,4}$ are driven by the input signal attenuated by α. $Q_{1,2}$ are directly driven by the input signal but with a negative DC level shift ($-V_{os}$) with respect to the base of $Q_{3,4}$. The circuit operation is as follows: at small V_{in}, the lower bias voltage keeps $Q_{1,2}$ off and the circuit approximates equation (2.7) near the origin with a simple differential pair formed by $Q_{3,4}$. But when V_{in} rises, $Q_{1,2}$ turn on, subtract current from the outputs and reverse the slope of the trans-characteristic. The zero crossings of the current offsetted from the origin (in Figure 2.4b), occur when the voltage at the base of $Q_{3,4}$ equals the voltage at the base of $Q_{1,2}$ i.e. $½\alpha V_{in}=½V_{in}-V_{os}$. This condition is satisfied for $v_{in} = \pm 2\,V_{os}/(1-\alpha)$. The zero crossings of (2.7) are at $v_{in} = \pm\sqrt{3}A/2$. Therefore V_{os} and α must be selected to satisfy:

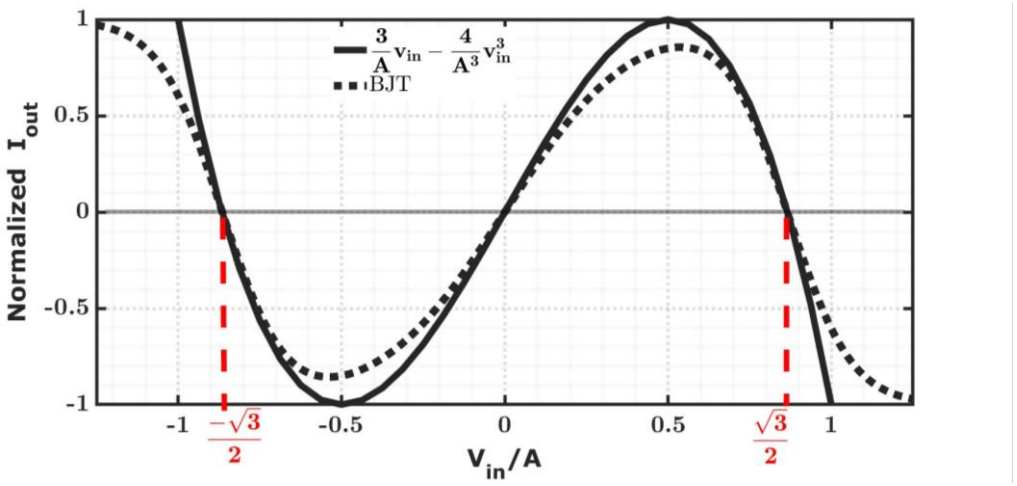
$$\frac{2V_{os}}{(1-\alpha)} = \frac{\sqrt{3}}{2} A \qquad (2.8)$$

Further circuit analysis proves that setting α=0.2 allows to fit the slope of (2.7) near the three zero crossings. With α fixed, equation (2.8) shows that to maintain the correct zero crossings at different input powers, V_{os} must be varied linearly with the input signal amplitude (A). Therefore, V_{os} is generated by an envelope detector, shown in the block diagram of Figure

2.1.



(a)



(b)

Figure 2.4. (a) Simplified schematics of the proposed tripler (b) comparison of the DC transfer characteristic with Eq. (2.7)

Looking at the plot in Figure 2.4b, the transistor implementation approximates well equation (2.7). Simulations at low frequency confirm that the circuit suppresses almost completely the component at f_0 in the output current. With a driving signal in Ku-band, device parasitic capacitors distort the dynamic shape of the trans-characteristic and reduce the f_0 suppression, but the issue can be solved by resonating out the equivalent shunt capacitance at the common-emitter node at frequency $2f_0$. The achievable f_0 rejection is ultimately limited by the accuracy to which V_{os} is set.

2.3.2 Circuit design

The complete tripler circuit is shown in Figure 2.5. The differential signal provided by the transformer balun (T_1) drives directly the base of $Q_{1,2}$ while it is attenuated by α through a capacitive voltage divider (C_1, C_2) to feed the base of $Q_{3,4}$. The four transistors have the same

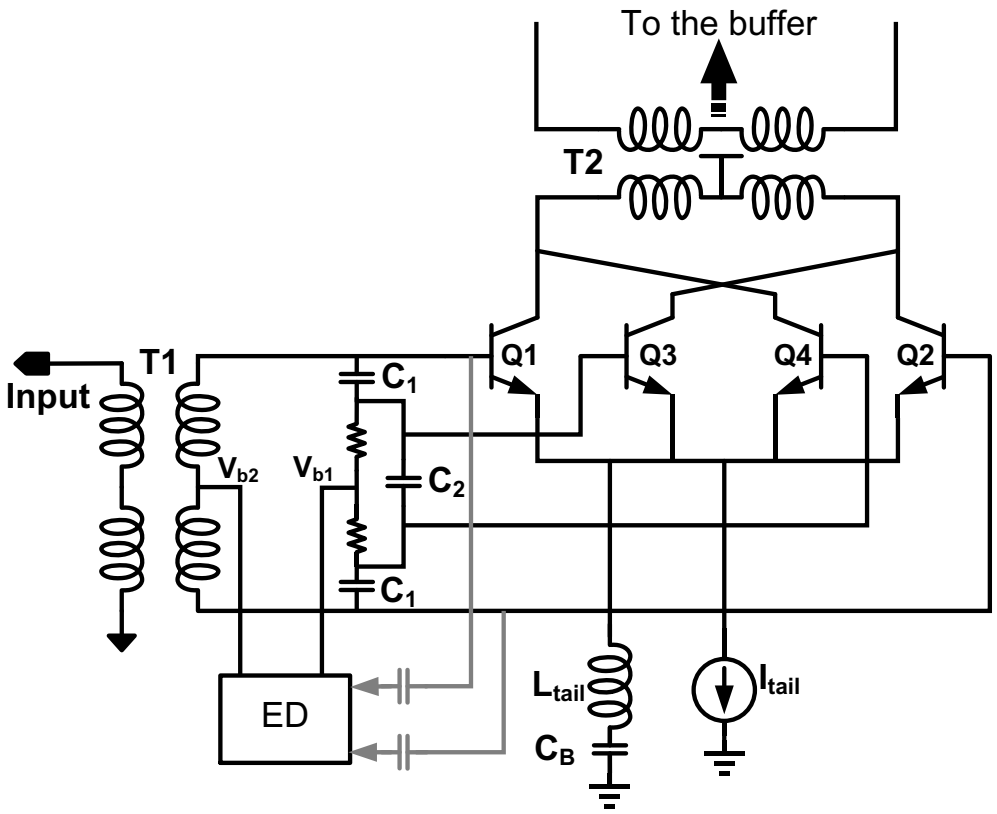


Figure 2.5. Detailed schematics of the proposed Tripler

emitter area (A_e=17.5x0.2 um^2) and are biased by I_{tail}=12.8mA. The inductor L_{tail} resonates with the equivalent shunt capacitance at the common-emitter node and C_B is sized sufficiently large to act as an AC short. The quality factor of L_{tail} is not critical, because the impedance at resonance is limited by the low equivalent resistance at emitters of $Q_{1\text{-}4}$. The transformer T_2

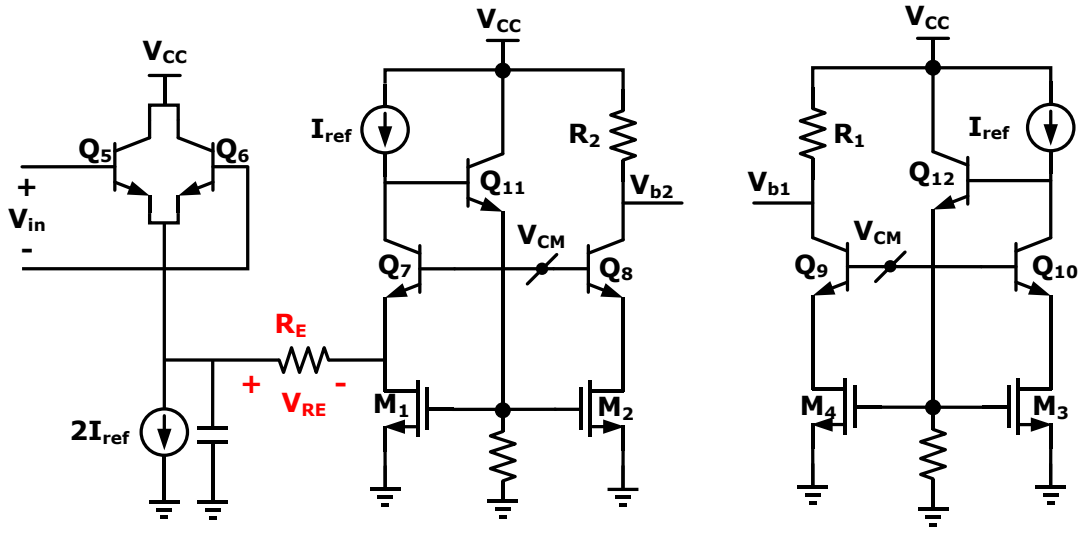


Figure 2.6. The Envelope detector Circuit

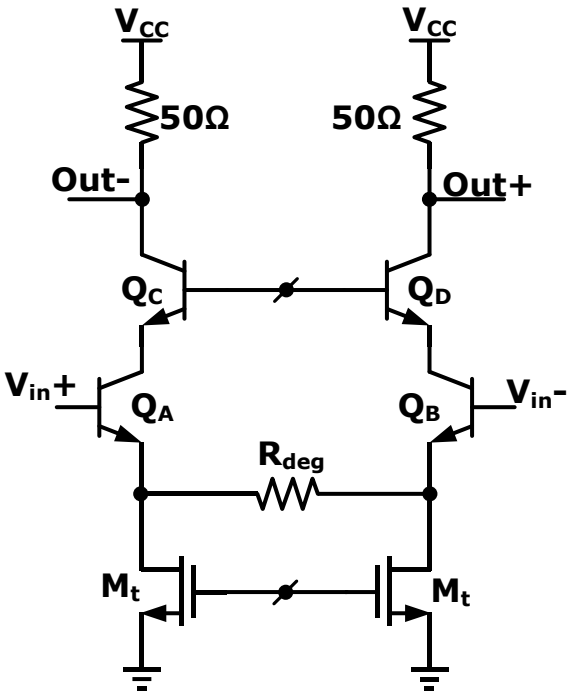


Figure 2.7. Test buffer following the tripler

provides the supply voltage (V_{cc}=1.7V) and couples the tripler to the cascaded circuits (test buffer in the tripler breakout, or doubler in the sextupler chip, shown in Figure 2.1). The transformer is designed to achieve a fractional bandwidth of 16%, centered at 37.5GHz.

V_{b2} and V_{b1} are the bias voltages for $Q_{1,2}$ and $Q_{3,4}$ respectively. They are generated by the envelope detector (ED) block such that V_{b1}-V_{b2} (corresponding to V_{os} in Figure 2.4) tracks the amplitude of the driving signal. The ED circuit schematic is shown in Figure 2.6. $Q_{5\text{-}10}$ share the same bias voltage, V_{CM}. In this way, $Q_{5,6}$ (driven by $V_{in}(t)$) and Q_7, set V_{RE} equal to the average value of $|V_{in}(t)|$. If $V_{in}(t)=A\sin(2\pi f_0 t)$, $V_{RE}=A/\pi$ and $I_{RE}=(A/\pi)/R_E$. $M_{1,2}$ mirror $I_{ref}+I_{RE}$ into R_2 while $M_{3,4}$ mirror I_{ref} into R_1 leading to $V_{b2}=V_{cc}-(I_{ref}+I_{RE})R_2$, $V_{b1}=V_{cc}-I_{ref}R_1$. Assuming $R_1=R_2$ results in $V_{os}=V_{b1}-V_{b2}=R_2 I_{RE}=(A/\pi)(R_2/R_E)$. The ratio R_2/R_E is selected such that V_{os} satisfies equation (2.8), thus allowing to maintain good suppression of the fundamental frequency component independently from the amplitude of the input signal.

In the tripler breakout chip a linear buffer follows the tripler and it is designed with the purpose of performing accurate experimental characterization of the tripler circuit. As shown in Figure 2.7, it is realized with a resistively degenerated cascode differential pair with resistive loads. From simulations, it introduces 9.6dB flat attenuation with 70GHz bandwidth, allowing measurements up to the 5th harmonic of the input. The output power at 1dB gain compression point is 1dBm.

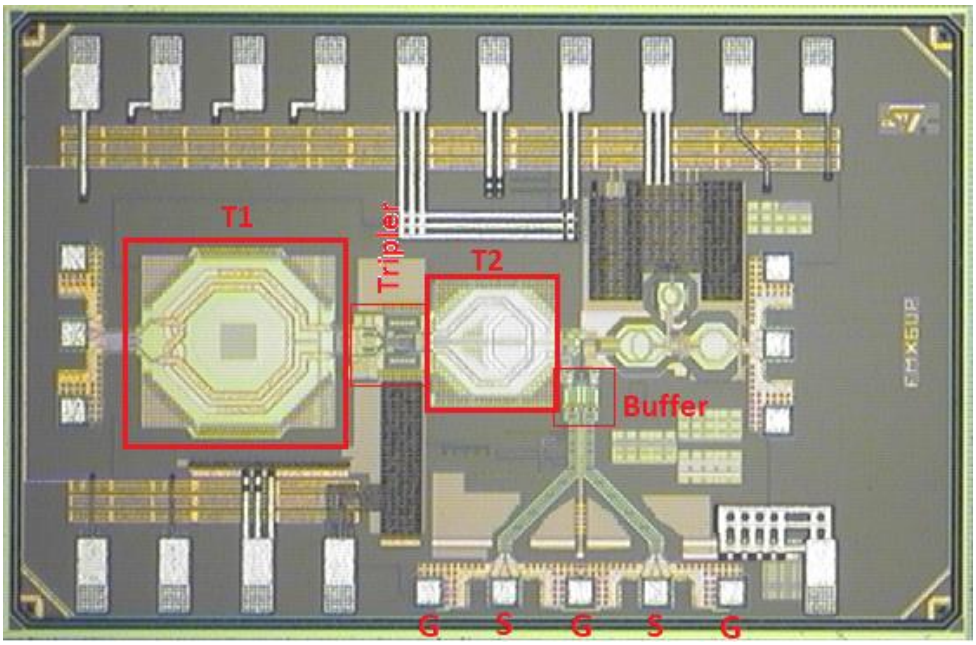


Figure 2.8. Chip photograph of the tripler breakout

2.3.3 Measurement results of the tripler breakout

The frequency tripler is designed and fabricated in STMicroelectronics 55nm SiGe-BiCMOS technology. All the simulations were done using the Spectre engine and the inductors were modeled using EMX which is a 2.5D electromagnetic simulator. The chip photograph is shown in Figure 2.8. The input signal is provided by a continues wave (CW) source and the output is measured using a spectrum analyzer. The on-chip buffer provides a differential output (GSGSG pad in Figure 2.8) but measurements are performed single-ended by probing each of the two outputs separately. Figure 2.9 compares the measured and simulated power delivered to a 50Ω load at $3f_0$ and the leakage of f_0 and $5f_0$ versus frequency when the tripler is driven by a 0dBm input signal. The single-ended peak output power is 0dBm at 37.8GHz and remains above -3dB variation from 35 to 41GHz, corresponding to 15.8% fractional bandwidth. Maximum and minimum rejection of f_0, $5f_0$ in this frequency range are 43.8dB and 37.5dB respectively. The tripler and ED draw 13.6mA from a 1.7V supply while the output buffer, not optimized for power efficiency but for wide bandwidth and high linearity, draws 32mA from a 3V supply. From simulations, the differential voltage swing at the buffer's input is around 930mV zero-peak.

Figure 2.10 shows the measured output power at $3f_0$ when the input power is swept at 12.5GHz. The same plot reports the HRR considering signal leakage at f_0 and $5f_0$. In the range –5 to 10dBm the single-ended output power at 3_{f0} rises from -8 to +4dBm. The HRR is better

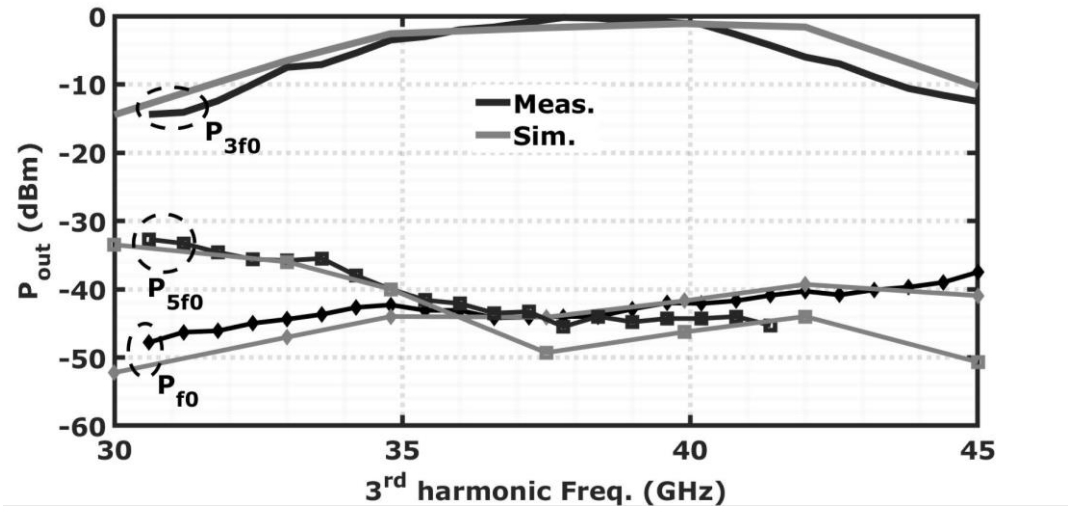


Figure 2.9. Measured and simulated output power of the tripler breakout chip showing the 3rd harmonic, f0, and f5 leakage

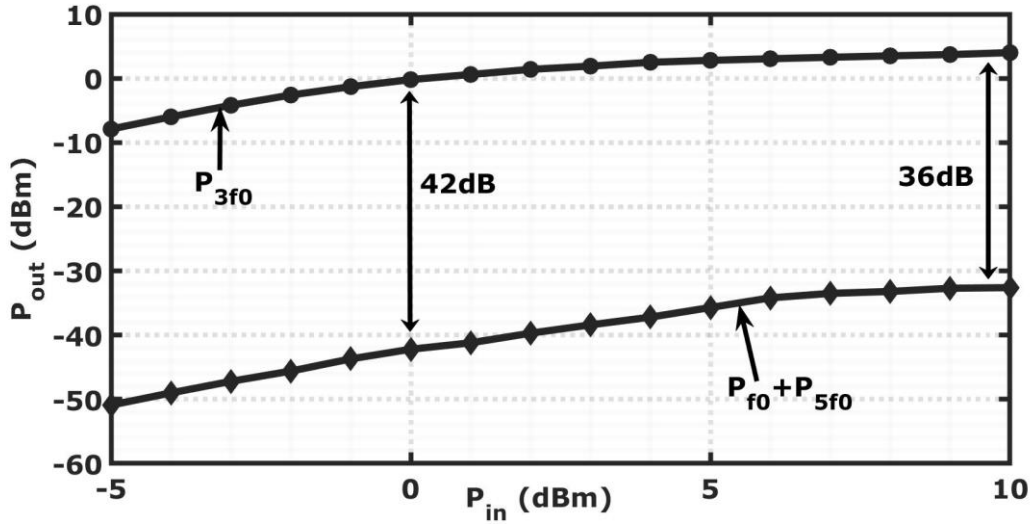


Figure 2.10. Measured output power of the tripler breakout chip showing 3rd harmonic and HRR versus input power at f_0=12.5GHz

than 40dB until 4dBm input power and rises to 36.6dB for 10dBm input.

Figure 2.11 shows input and output PN at 12.5GHz and 37.5GHz, respectively. The difference between the two plots is 9.5dB, as expected by the frequency multiplication by 3, thus proving negligible phase noise deterioration from the tripler.

Finally, measurement results are summarized in Table 2.1 and compared against previously reported frequency triplers. All the designs are based on transistors in class-C for harmonic generation. On average, the rejection of unwanted tones is near 20dB. [28] reached 33dB by leveraging injection locking filtering, but at the cost of narrow bandwidth, limited by the

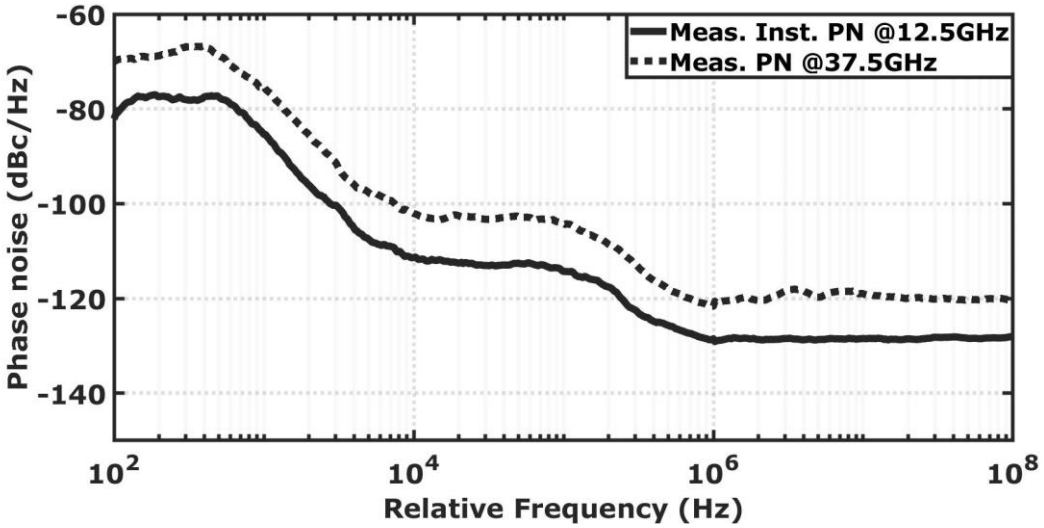


Figure 2.11. Phase noise performance of the tripler

locking range. The tripler in [30] reaches 28dB rejection and maintains wide bandwidth by inserting a notch filter tuned to f_0, but the core power dissipation is nearly 3 times larger than in this work. The proposed solution demonstrates > 10dB improvement of undesired harmonic tones rejection with operation bandwidth and core power dissipation aligned with state of the art.

Table 2.1. Measurement summary and comparison for the tripler breakout chip

Ref	*Tech*	*f_{out} (GHz)*	*Supp. of Largest tone (dBc)*	*P_{in}/P_{out} (dBm)*	*P_{DC} (mW) Core + Buffer*
[26]	0.18um SiGe BiCMOS	80-100 (20%)	20	0/-10.5	5+70
[28]	65nm CMOS	85-95.2 (3.5%)[a]	32.9	4/-3.8[b]	5.2+ 14.6
[34]	0.13um CMOS	57-61 (6.6%)	22-31.3	0.5/-9.5	9.96+16.1
[35]	0.15um PHEMT	58.5-65 (10.5%)	19-21	-1/-2.6	56
[30]	0.13um SiGe	48-58 (19%)	28-38	-2.5/9.5	62+158
[36]	0.13um CMOS	36-48 (28%)	10-40	0/-11.4	12.6+11.9
[37]	0.15um PHEMT	35-38.5 (9.5%)	10-22	9/-0.4	18.9
This work	55nm SiGe BiCMOS	35-41 (15.8%)	37.5-43	0/0 (Single ended)	23+96

2.4 Proposed frequency doubler with 75GHz output frequency

As discussed earlier, push-push frequency doublers are the most popular due to their simplicity and inherent suppression of the driving signal. However, their single-ended output poses a challenge to differential operation of the following stages. Figure 2.12 shows the proposed differential frequency doubler which is based on the conventional push-push design. The differential input signal is applied to the base terminal of transistors $Q_{13,14}$. The two inductors L_1 and the capacitor C_4 are big enough to work as open and short at the frequency of operation, respectively. Therefore, the current signal at double frequency that flows **into** the common emitters of $Q_{13,14}$, passes through C_4 and then buffered by Q_{15}, and finally flows **out of** its collector terminal, hence delivering a differential current to T3. In order for Q_{15} to work as a current buffer in common-base configuration, its base voltage should be at AC ground with respect to the differential signal applied to $Q_{13,14}$. This is accomplished by means of the capacitors C_3 whose equivalent capacitance for a common mode signal at $V_{in}^{\pm}$ is four times larger than it is for a differential signal. Therefore, the network made of C_3 works as a low-impedance path to keep the common mode voltage of Q_{15} equal to $Q_{13,14}$, whereas differentially, it provides a 4 times smaller capacitive load to T2. Note that the resistors R_3 only provide the DC bias for $Q_{13,14}$, which is almost equal to that of Q_{15}. At the frequency of operation, the admittance introduced by C_3 is dominant and over R_3.

The secondary of the transformer T3 drives the output buffer shown in Figure 2.13. The input transistors $Q_{16,17}$ and the cascode transistors $Q_{18,19}$ work as a cascode differential

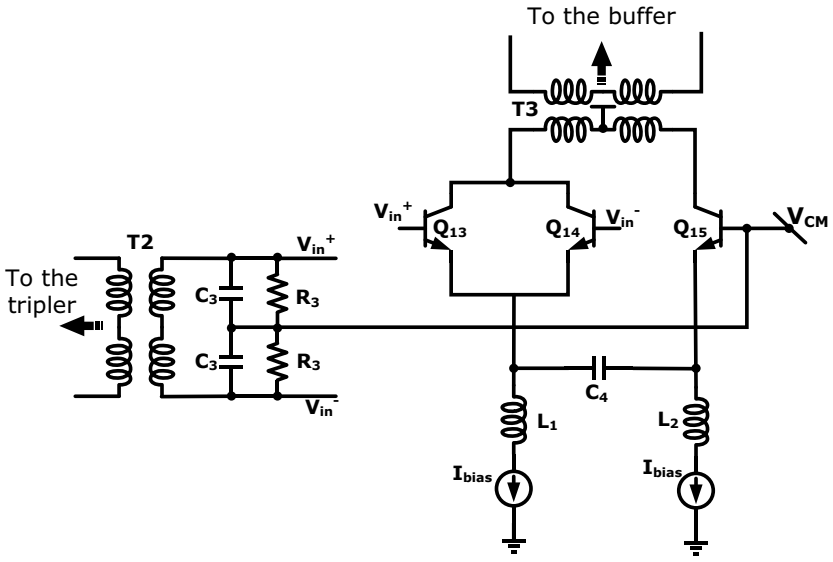


Figure 2.12. Proposed E-band frequency doubler with differential operation

amplifier. The transistors $Q_{20,21}$ are cross-coupled by the pair of capacitors C_X and form a cross-coupled differential oscillator. The capacitors C_X are sized large enough to drive the bases of $Q_{20,21}$ with a large voltage swing and steer I_{XC} to one branch at each half cycle. Therefore, the combination of the cascode amplifier and the oscillator form an injection-locked buffer amplifier. Due to the low quality factor of the oscillation tank ((composed of T4, the parasitic capacitances and the off chip equivalent 50Ω resistance), the locking range of the injection buffer is high enough to cover the frequency range of interest. Moreover, the amount of current injected into the tank by the cascode buffer can be programmed by changing I_{buff}, while the amount of oscillation current can be programmed by changing I_{XC} in Figure 2.13. Therefore, *locked* operation can be ensured over the frequency range of interest by setting the $\frac{I_{inj}}{I_{osc}}$ ratio sufficiently large [10] through programming the two bias currents, I_{buff} and I_{XC}. The reason behind using the oscillator in parallel with the cascode buffer is twofold; *first*, the oscillator working in the injection locked regime suppresses the undesired tones, thus improves spectral purity of the output tone. *Second*, it allows using smaller input devices in the buffer ($Q_{16,17}$). This is because the current delivered to the load is directly proportional to the sum of the bias currents, $I_{buffer}+I_{XC}$. The smaller is the contribution of I_{buff} to this sum, the smaller the size of input transistors. The smaller size of $Q_{16,17}$ is desirable because it means less parasitic capacitance at the input of the buffer, which facilitates matching of the buffer to the previous stage, the doubler. T4 both serves as the inductor of the oscillation tank and the output balun to deliver a single ended output. A matching network between T4 and the GSG pad provides

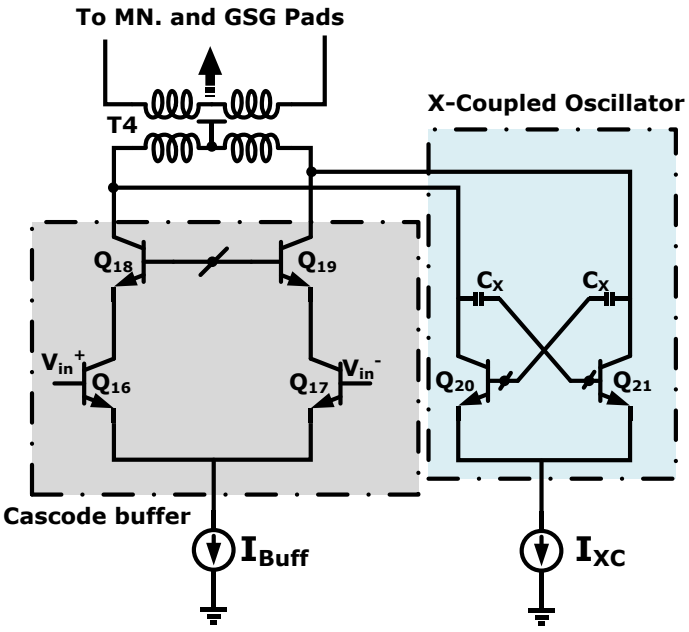


Figure 2.13. Output injection buffer

50Ω matching to the load.

2.5 Measurement results of the sextupler chip

The chip photograph and the measurement setup is shown in Figure 2.14 and Figure 2.15, respectively. The sextupler chip is designed in the same technology as the tripler breakout and measures 0.81x1.7mm^2. All the simulations were done using the Spectre engine and the inductors and transmission lines were modeled using EMX which is a 2.5D electromagnetic simulator. The input signal is provided by a CW source and applied through microprobes. The

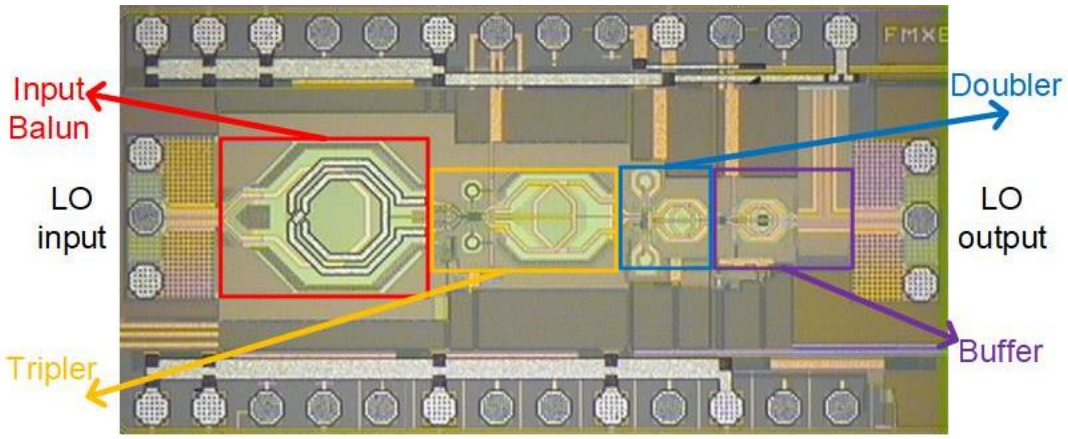


Figure 2.14. Microphotograph of the sextupler chip

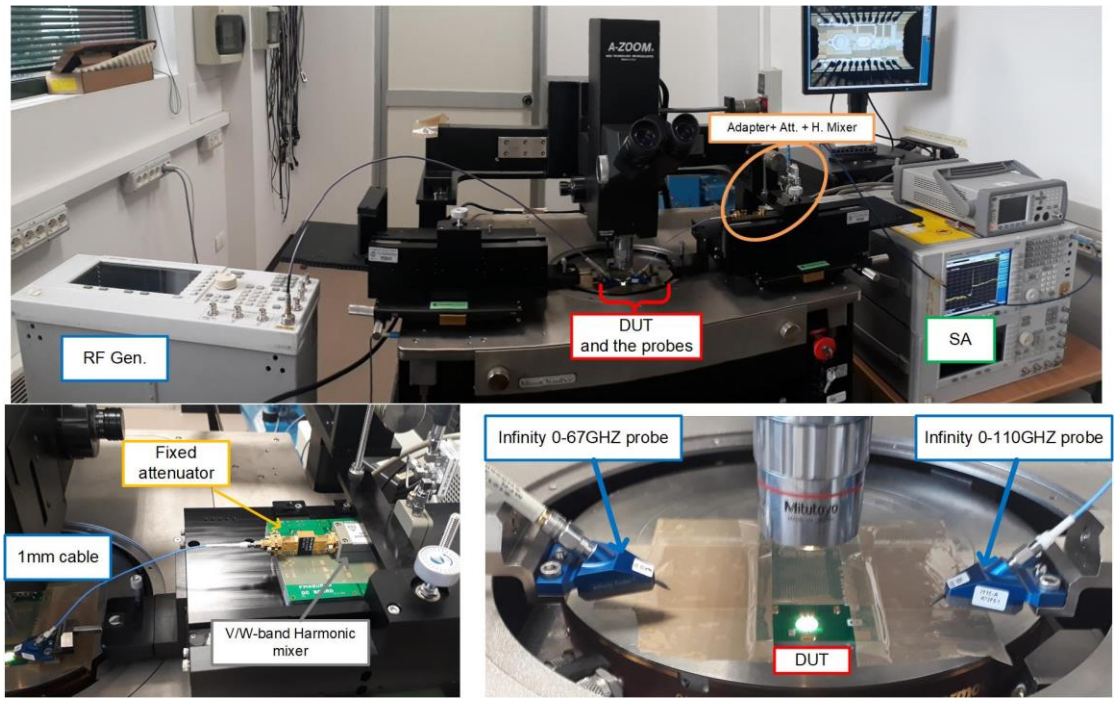


Figure 2.15. Measurement setup for the sextupler test chip

output is measured using a spectrum analyzer whose operation frequency was extended to V and W-band using harmonic mixers. The harmonic mixers saturate at very low input power. Therefore, a fixed waveguide attenuator was used before the mixers. Moreover, the overall loss of the path from the probe tips to the spectrum analyzer, including the probe loss, cable and adapter losses, the fixed attenuation, and the loss of the harmonic mixers (typically around 35-40dB) were measured using calibration kits and de-embedded from the measurement results.

Figure 2.16 shows the measured power delivered to a 50Ω load at $6f_0$ and leakage of other harmonics of f_0 versus frequency when the sextupler is driven by a 0dBm input signal. The

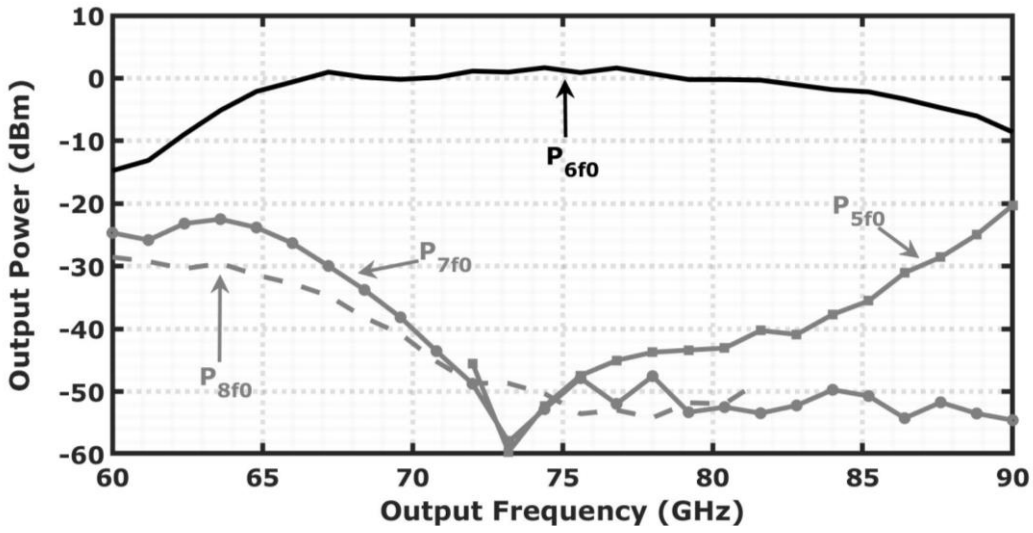


Figure 2.16. Measured output power of the 6th harmonic and the largest spurious tones versus frequency for 0dBm input signal

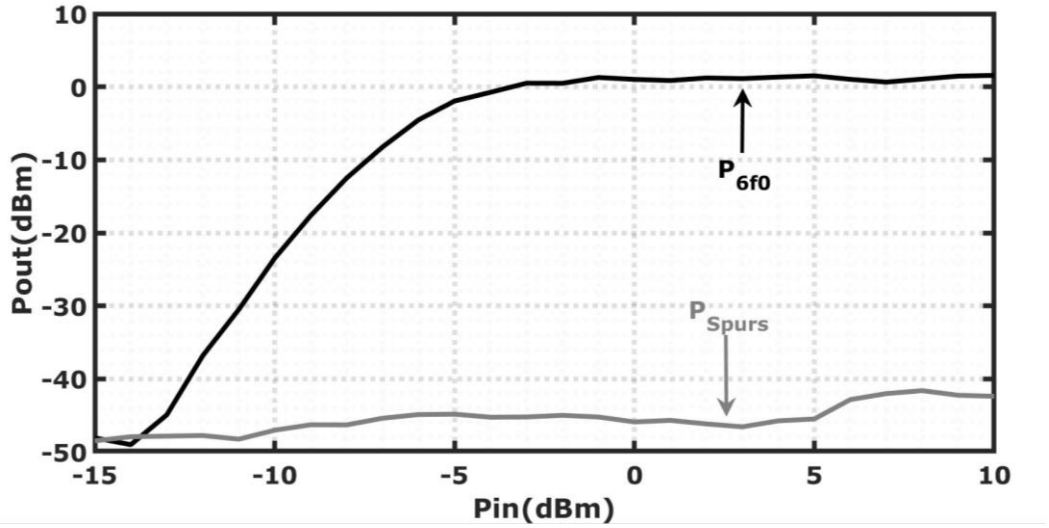


Figure 2.17. Measured output power of the 3rd harmonic and HRR versus input power at f_0=12.5GHz. P_{Spurs} shows sum of powers of all spurious tones.

peak output power is 1.7dBm at 74.4GHz and remains within 3dB variation from 65.5GHz to 83.5GHz, corresponding to 24% fractional BW. In this frequency range, the leakages of all harmonics are below -30dBc and at the center frequency are as low as -50dBc. Moreover, in the BW required for the DREAM project (70-80GHz), all harmonics are suppressed by more than 40dBc. From Figure 2.16 it can be seen that at the lower and higher extremes of the frequency range, the leakage of the undesired harmonics is dominated by the 7^{th} and 5^{th} harmonics of the input signal. As discussed in section 2.2, the 7^{th} harmonic should not be present at the output, or generated in the first place. This was under the assumption that due to the symmetry, all even-order harmonics of the driving signal are suppressed in the tripler's output, and it only generates the fundamental and 5^{th} harmonic. However, if there is an asymmetry in the differential signals driving the tripler, even harmonics are also generated. As the 4^{th} harmonic is the most spectrally close tone to the third harmonic, it experiences little suppression by the transformer T2 (Figure 2.5) and appears at the input of the doubler. Then, it is intuitive to expect the 3^{rd} and 4^{th} harmonics to be mixed in the doubler and generate a tone at the 7^{th} harmonic (also from equation (2.1)). This asymmetry is most likely introduced by the input balun due to modeling errors. In a similar manner, the 2^{nd} harmonic at the doubler's input can be mixed with the main tone at $3f_0$ and generate the 5^{th} harmonic at the output. It's important to note that the mechanism described above is a minor nonideality that occurs at extremes of the frequency band. In the bandwidth of interest, however, all spurious tones were heavily suppressed.

Figure 2.17 shows the measured output power at $6f_0$ when the input power is swept at 12.5GHz. The same plot reports the HRR considering signal leakage at $5f_0$,$7f_0$ and $6f_0$. The output saturates when the input power reaches -3dBm, and from -3dBm to 10 dBm, variation of the output power is limited to 1dB. Also, the HRR is better than 40dBc for input power larger than -4dBm and does not deteriorate with increased input power. The full chip draws 43.9mA from a 1.7V supply and the individual contributions of the tripler, doubler, and the output buffer are 10, 10, and 23.9mA respectively.

Finally, measurement results for the sextupler chain are summarized in Table 2.2 and compared against previously reported frequency multipliers that incorporate an odd order stage. The tripler stages in most of the works are based on class-C non-linearity generators similar to Figure 2.2a or b. The main advantage of the presented work is high suppression of the undesired harmonics while the bandwidth and efficiency are aligned with the state of the art. The multiplier by 9 in [13] is a cascade of two triplers with one amplification stage in

between the two and a power amplifier to drive the load. Excluding the input balun, there are 6 pairs of coupled transformers through the chain to reject the undesired harmonics by 31dBc. In comparison, the proposed design offers 10dB more harmonic rejection if the same fractional BW is considered, with using only half of those coupled transformers, higher conversion gain and overall efficiency. Also in [14] three filtering stages with orders of 5, 5, and 6 are employed to reach a HRR lower than the proposed work, while the efficiency is almost half. Another work that merits attention is the design presented in [15] in which there is a cross-coupled oscillator in parallel to both multiplying stages, thus harmonics have been rejected close to 40dBc while the efficiency is highest compared to all other works. However, due to the cascaded injection-locked oscillators the fractional BW is extremely small (1.5%) and not usable for applications of high data rate transmission. In comparison, the HRR of the presented work is more than 40dBc at center frequency if an equal fractional BW is considered.

Table 2.2. Measurement summary and comparison for the sextupler test chip

Ref	***Tech***	***× N***	***f_{out} (GHz)***	***Supp. of Largest tone (dBc)***	***P_{out} (dBm)***	***CG (dB)***	***P_{DC} (mW)***	***η*****
[13]	65nm CMOS	9	88-99.5 (12.2%)	31	8.5	-5.7	438	1.5
[38]	65nm CMOS	9	88.9-95.5 (7.2%)	16	-1.8	1.4	120	0.55
[39]	90nm CMOS	6	96.1-98.4 (2.3%)	NA	-17.2	-17.2	55.4	0.034
[40]	100nm mHEMT	6	155-195 (22.8%)	20	0	-6.5	92.5	1
[41]	65nm CMOS	6	74.7-80.5 (7.4%)	NA	4	4	51	4.8
[15]	65nm CMOS	6	76.81-77.95 (1.47%)	39	8.9	NA	116.7	<6.6
[14]	100nm mHEMT	6	78-104 (28.6%)	25	7	5	470	1
This work	55nm SiGe BiCMOS	6	65.5-83.5 (24%)	30*	1.7	1.7	74.63	1.95

*40dBc suppression considering 16% BW from 70 to 82GHz.

**$\eta = \frac{P_{out}}{P_{DC}+P_{in}}$

Chapter 3 D-band frequency doubler

As discussed in section 2.1, the easiest way to implement a frequency doubler is by leveraging transistors biased at a low conduction angle to generate a strong second harmonic of the input. By using a pair of transistors driven by a balanced signal (also known as push-push configuration) the fundamental component and odd-order harmonics are well suppressed without requiring highly selective filters. Nevertheless, when the operating frequency gets closer to the technology limit, f_{max}, designing power efficient frequency doublers is challenging because of the limited output power and the low available gain of transistors. As a matter of fact, the majority of frequency doublers with the output signal near or above 100GHz require high input power (P_{in}), typically greater than the output power (P_{out}) [21, 42-45]. The resulting negative Power Added Efficiency, PAE=(P_{out}-P_{in})/P_{DC} (being P_{DC} the power consumption) sets challenging demands and high power consumption also to the driving circuits.

To the author's knowledge, the best performance above 100GHz is demonstrated by the push-push doubler in [46]. Realized in a SiGe BiCMOS technology with 500GHz f_{max}, it shows a record conversion gain of 4dB, P_{out}=5.6dBm and PAE=5.9% at maximum output power. A similar circuit topology, implemented in a 350GHz f_{max} SiGe technology [47], still delivers a high P_{out} of 6.5dBm, but with conversion gain and PAE reduced to 1.5dB and 3.3%, respectively.

In this part of the work, a common-collector Colpitts oscillator which works as a common-base injection-locked amplifier is investigated to boost the current conversion efficiency of mm-Wave push-push doublers, enhancing the conversion gain, output power, and PAE. A D-band frequency doubler test chip was design in the same SiGe BiCMOS technology as the previous chip, with 330GHz f_{max}, and delivers P_{out} up to 8dBm at 130GHz with 13dB conversion gain and 6.3% PAE.

3.1 Circuit description

The circuit schematic of the presented frequency doubler is drawn in Figure 3.1. The second harmonic of the input signal is generated by transistors $Q_{1\text{-}2}$, in push-push configuration. The input signal, at frequency ω_0, is made differential by the transformer T1. Because well balanced voltages at the base of $Q_{1\text{-}2}$ are key to ensure good suppression of the fundamental frequency component, the residual common mode signal due to imbalances in transformer T1

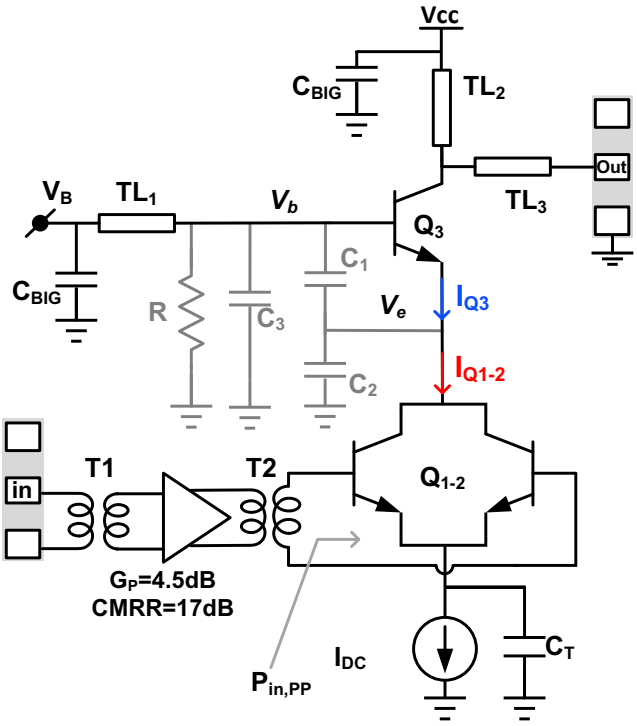
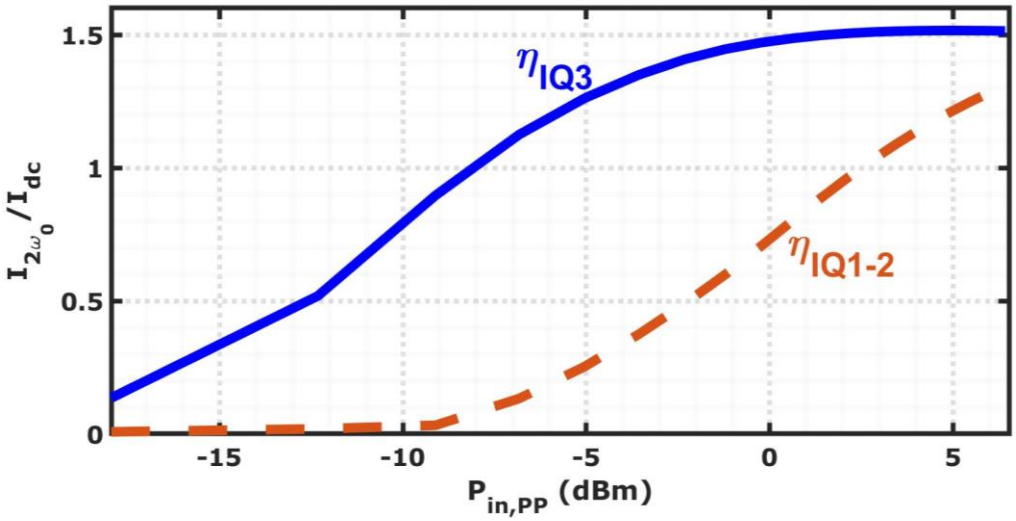


Figure 3.1. Schematic of the proposed Colpitts frequency doubler

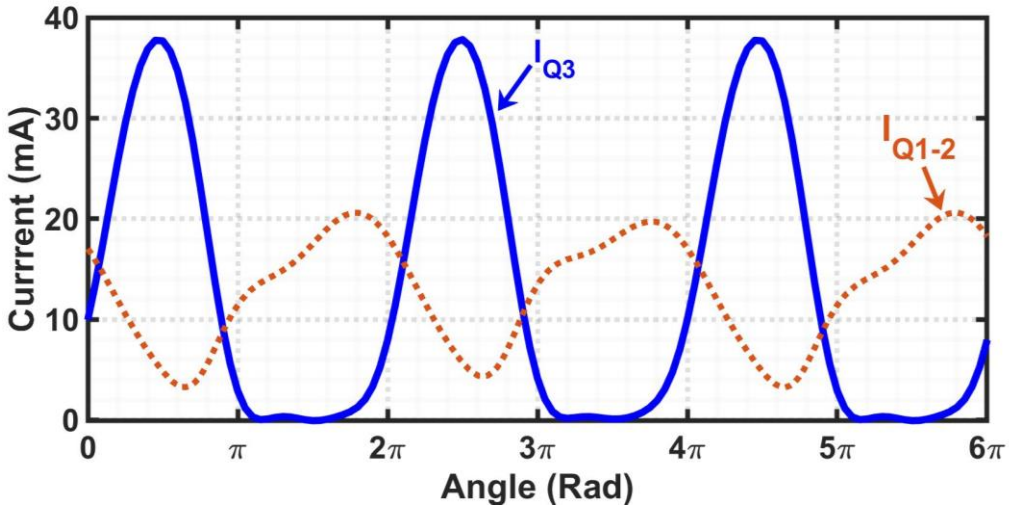
is attenuated by a differential-pair buffer stage, coupled to $Q_{1\text{-}2}$ with the transformer T2. The buffer draws around 7mA and introduces a simulated power gain G_P ~ 4.5dB with simulated common-mode rejection ratio of 17dB at 65GHz. $Q_{1\text{-}2}$ are biased at constant current, I_{DC}, and the large capacitor C_T sets the emitters to AC ground such that the transistors can operate in class-C, delivering a harmonic-rich output current [48].

Ideally, the collector current of $Q_{1\text{-}2}$, $I_{Q1\text{-}2}$ in Figure 3.1, should look like a train of tall and narrow pulses. At low frequency, with such a configuration, the current conversion efficiency, i.e. the ratio between the harmonic component at $2\omega_0$ and I_{DC}, $\eta_{I_{Q1-2}} = (I_{2\omega_0}/I_{DC})$, is close to 2 [48]. However, at high frequency the transistors' parasitics (the extrinsic base resistance and the base-emitter capacitance in particular) reduce significantly the conversion efficiency and the available output power from the push-push pair. Above 100GHz, with a reasonable driving power at the base of $Q_{1\text{-}2}$, $\eta_{I_{Q1-2}} < 1$.

Looking at the schematic in Figure 3.1, the current $I_{Q1\text{-}2}$, comprising I_{DC} and the second harmonic component is injected into Q_3. Together with the resonator comprising stray capacitances (C_1,C_2,C_3) and the transmission line stub TL_1 (AC shorted at one end by C_{BIG}), Q_3 forms a common-collector Colpitts oscillator. But for the input signal, at the emitter, Q_3



(a)



(b)

Figure 3.2. (a) Harmonic conversion efficiency on the current of Q_{1-2} and Q_3 versus the power driving Q_{1-2} (b) Time-domain current waveforms for $P_{in,PP}$= -1.2dBm

works as an injection-locked common-base amplifier which enhances significantly the current conversion efficiency and delivers higher power at $2\omega_0$ from the collector to the output through a matching network realized with TL_2 and TL_3.

The plot in Figure 3.2a shows the simulated conversion efficiency of the current at the output of Q_{1-2} ($\eta_{I_{Q1-2}}$) and at the collector of Q_3 ($\eta_{I_{Q3}}$) versus the power driving the push-push pair, $P_{in,PP}$. Comparing the two curves, the addition of the Colpitts stage to the push-push pair requires ~10dB less input power to reach the same harmonic generation efficiency. For given input power, e.g. $P_{in,PP}$=-5dBm, $\eta_{I_{Q1-2}}$= 0.25 while $\eta_{I_{Q3}}$ is raised by 5 times to 1.26.

It is worth noticing that the higher harmonic generation is achieved without raising the current consumption, because the same DC current, set by the current source I_{DC}, flows in both $Q_{1\text{-}2}$ and Q_3. To gain further insight, Figure 3.2b plots the current waveforms $I_{Q1\text{-}2}$ and I_{Q3} over time with $P_{in,PP}$=-1.2dBm. The mean value is the same in the two curves. The higher component at $2\omega_0$ in I_{Q3} is the result of Q_3 working in class-C with a small conduction angle, leading to the pulsed current shape. Here, the resonant tank formed by C_1,C_2,C_3, and TL_1 plays a key role since it absorbs $I_{Q1\text{-}2}$ when Q_3 is off, and it delivers the sharp I_{Q3} pulses when Q_3 turns on.

For circuit design and optimization, the Colpitts oscillator can be analyzed by partially using the results in [49]. Assuming a sinusoidal voltage across the Colpitts resonator (C_1-C_3 in parallel with TL_1) and an exponential I_C-V_{BE} characteristic for Q_3, the conversion efficiency $\eta_{I_{Q3}}$ is given by:

$$\eta_{I(Q3)} = \frac{I_{2\omega_0}}{I_{DC}} = 2\frac{B_1(a_e)}{B_0(a_e)} \tag{3.1}$$

where B_0, B_1 are the modified Bessel functions of the first kind of orders zero and one, respectively, and $a_e = v_{be}/(nV_T)$ (being v_{be} the 0-peak base-emitter voltage of Q_3, n the transistor ideality factor, and V_T the thermal voltage). $\eta_{I_{Q3}}$ is a monotonic function of a_e, growing from 0 to 2 when $a_e \gg 1$, i.e. $v_{be} \gg nV_T$. From a design perspective, to have the highest current component at $2\omega_0$, for fixed I_{DC}, the v_{be} of Q_3 has to be maximized.

Looking at the circuit schematic in Figure 3.1, C_1 and C_3 represent the capacitance from base to emitter of Q_3 and the capacitance from the base of Q_3 to ground while C_2 is the capacitance from the collector of $Q_{1\text{-}2}$ to ground. The resonance frequency of the Colpitts tank is $\omega_r = 1/\sqrt{LC_{eq}}$ (where L is the inductance of the TL_1 stub and $C_{eq} = C_3 + (C_1\ C_2)/(C_1 + C_2)$. R represents the equivalent resistance of the tank at resonance. The signal current at $2\omega_0$ which enters into the node shared by C_1 and C_2 is $I=(I_{Q3}\text{-}I_{Q1\text{-}2})$. By defining $m = C_2/(C_1 + C_2)$, the voltage at the base of Q_3 is $v_b = I\ R\ (1 - m)$. Assuming the tank's quality factor, Q, is sufficiently high, the base-emitter voltage can be approximated as[2]:

$$v_{be} \approx IR\ m\ (1 - m) \tag{3.2}$$

At ω_r, R can be written as $R = \omega_r LQ$. Substituting for R and rewriting (3.2) in terms of ω_r

[2] With moderately low Q, which is the case at high operation frequency, the approximated analysis still provide qualitatively correct results, as confirmed by the simulations in Figure 3.3.

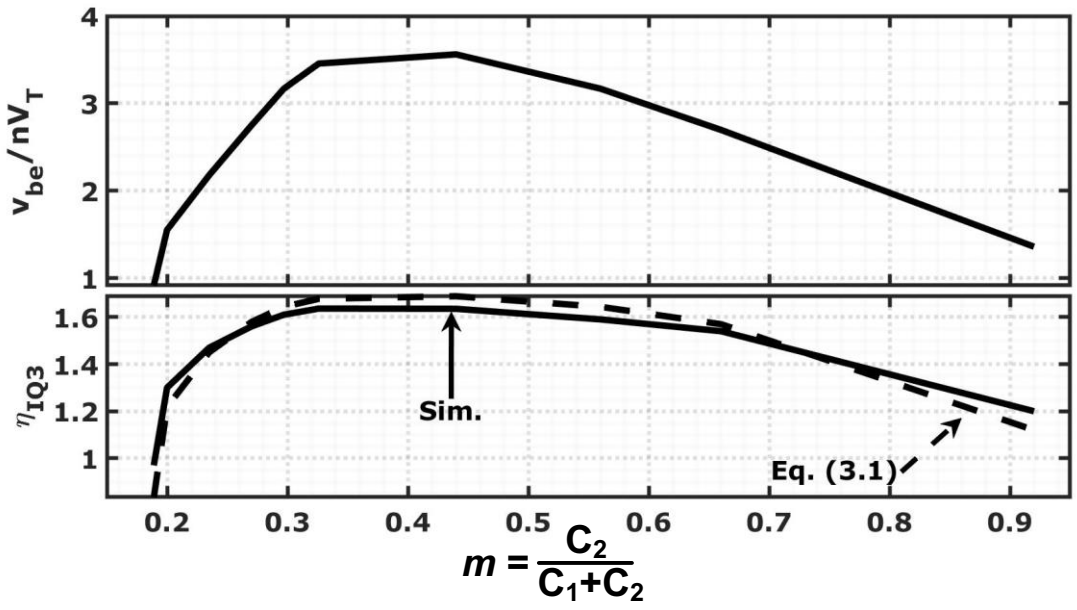


Figure 3.3. Simulated $\frac{v_{be}}{nV_T}$ of Q_3 (top plot), and $\eta_{I_{Q3}}$ (bottom plot) from simulation and equation (3.1).

and C_{eq} yields:

$$v_{be} \approx I \frac{Q}{C_1 \omega_r} \frac{(1-m)m}{m + \frac{C_3}{C_1}} \tag{3.3}$$

Equation (3.3) suggests that assuming a fixed quality factor for the tank and a desired ω_r, v_{be} and hence $\eta_{I_{Q3}}$ are maximized if the right-most fraction is set to its maximum value. C_1 is implemented by the parasitic base-emitter capacitance of Q_3, which in turn is sized for a desired P_{out}. In this design, the emitter area for Q_3 is set to 25x0.2μm^2. C_3 comprises the capacitance to ground of TL_1 and the base-collector capacitance of Q_3. The optimal m to maximize equation (3.3) is determined by C_2, which must absorb the parasitic capacitance at the collector of $Q_{1\text{-}2}$.

The top plot in Figure 3.3 shows the simulated v_{be}/nV_T versus m with the selected size for Q_3. $Q_{1\text{-}2}$ are replaced by an ideal current source with I_{DC}=10mA and $I_{2\omega o}$=6mA, emulating the case with $P_{in,pp}$~-1.2dBm from Figure 3.2(a). In the simulation, C_2 is implemented with an explicit capacitor and changed to sweep m. The top plot in Figure 3.3 shows that v_{be} peaks between m=0.35-0.45, in agreement with what expected from equation (3.3). The bottom plot shows $\eta_{I_{Q3}}$ both from simulations and calculated by equation ((3.1) with the simulated v_{be}/nV_T in the top plot.

In the final design, $Q_{1\text{-}2}$ were sized with 9.4x0.2μm^2 showing a parasitic collector capacitance ~50fF, which implements C_2 with the optimal $m \approx 0.4$. However, it is worth noticing from Figure 3.3 that the sensitivity of $\eta_{I_{Q3}}$ to m around the optimal value is low, ensuring a robust performance against uncertainty in the precise value of the capacitors.

A merit of the common-collector Colpitts oscillator as an injection-locked amplifier is that it keeps separated the load, at the collector, from the resonator, connected to the base and emitter terminals. In this way, the current-conversion efficiency and load impedance can be optimized almost independently, to maximize the output power. To deliver power to the off-chip 50Ω load impedance, a matching network, comprising TL_2-TL_3 is added between the GSG output pad and the collector of Q_3. The optimal load impedance is found with load-pull simulations. Figure 3.4 draws the constant power circles on the Smith chart with 1dB steps at 130GHz when the circuit draws I_{DC}=11mA from V_{CC}=2V. The maximum output power, P_{out}, is 5dBm. However, the sensitivity of P_{out} to the load is low. Modeling the load seen by the collector of Q_3 as a parallel resistance and inductance, P_{out} stays greater than 4dBm for a resistance between 30Ω to 90Ω and the inductance between 15pH to 24.5pH.

When driven by the input signal, the Colpitts oscillator is injection-locked by the by the current delivered by the push-push pair. The frequency locking range is set by the quality factor of the tank and the ratio between the component at $2\omega_0$ of injected current ($I_{Q1\text{-}2}$) and the oscillator core current (I_{Q3}) [10]. The low tank quality factor (Q<3), limited by the large loss in the device parasitic capacitors in the tank, ensures the oscillator maintains lock over very

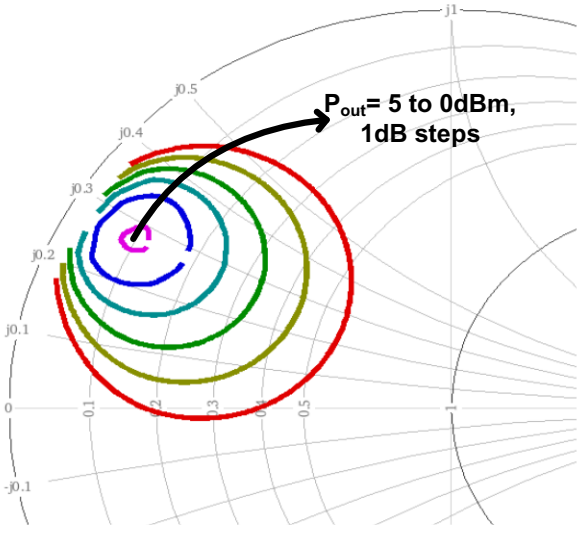


Figure 3.4. Constant-power circles from load-pull simulation

wide frequency range. In this situation, the doubler operation bandwidth is mostly limited by the frequency response of the output matching network.

3.2 Measurement results

The measurement of this chip requires a more complicated setup because there were no spectrum analyzer available at D-band (nor any extension module), nor any signal source above 70GHz. To generate the input signal above 70GHz, an E-band VNA[3] extension module[4] was used which allows up-converting frequency of the input signal by a factor of 6. To monitor the output spectrum, a D-band VNA extension module[5] was used to down-convert the test signal to a low IF suitable for the spectrum analyzer. The input-output characteristics of both of the extension modules are nonlinear, frequency dependent, and time varying. Therefore, a characterization procedure is required before measurements can be done.

Figure 3.5 shows the internal schematics of the D-band VNA extension module along with the instruments' configuration in transmit (up-converting) and receive (down-converting) modes. The characterization procedure is described only for the D-band module, but is similar for the E-band module, hence the latter is not covered here. In transmit mode, as shown in Figure 3.5a, an input signal is applied to the *RF input* port whose frequency is up-converted by a factor of 12 and appears at the *waveguide test* port. The output power is proportional to the applied power to the *RF input* port, but the ratio is non-linear, frequency dependent, and varies with time. A built-in functionality of the module allows down-converting a small fraction of the transmitted power to a *Reference IF* port. The LO required for the down conversion should be provided by another signal source to the *LO input* port which also incorporates a built-in frequency multiplier by 12. If the power applied to the *LO input* port is set to the maximum allowed level, the ratio between the power going out of the *waveguide test* port and the power that appears at the *Reference IF* port is linear but frequency dependent. The characterization was done by sweeping the frequency applied to the *RF input* and measuring the power at the *waveguide test* port and at the *Reference IF* port using a D-band and a low frequency power meter, respectively. At each frequency, the difference between the two power meters (in dB) was kept as the offset associated to that frequency, so the module was characterized over the full D-band range. The IF frequency was kept constant by keeping a fixed offset between RF

[3] Vector Network Analyzer
[4] Agilent N5260-6004
[5] VDI VNAX, WR6.5

and LO frequencies.

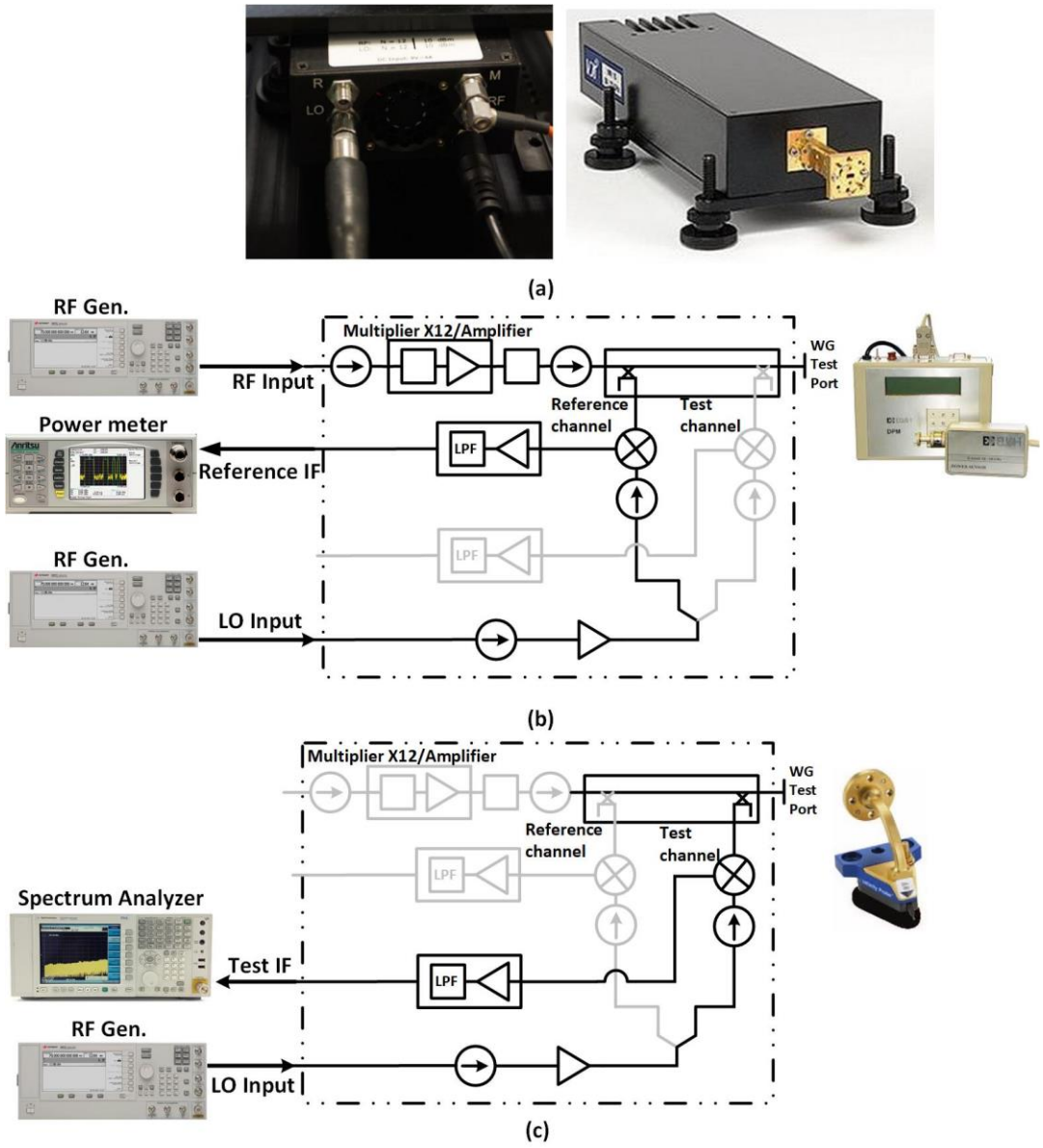


Figure 3.5. (a) D-band VNA extension module from VDI, (b) internal schematics and instrument configuration in transmit mode, (c) internal schematics and instrument configuration in receive mode

In receive mode, as shown in Figure 3.5b, a small fraction of the signal that enters the *waveguide test* port is down-converted and amplified to a dedicated port, the *Test IF* port, using the signal provided to the *LO input* port. The relationship between the power entering the *waveguide test* port and the power that appears in the *test IF* path was characterized as a function of frequency by connecting a pair of the modules back-to-back, one working in transmit and the other in receiver mode. Using the numbers previously obtained for the transmitter, the offset of the *test IF* path with respect to the entering power was measured for

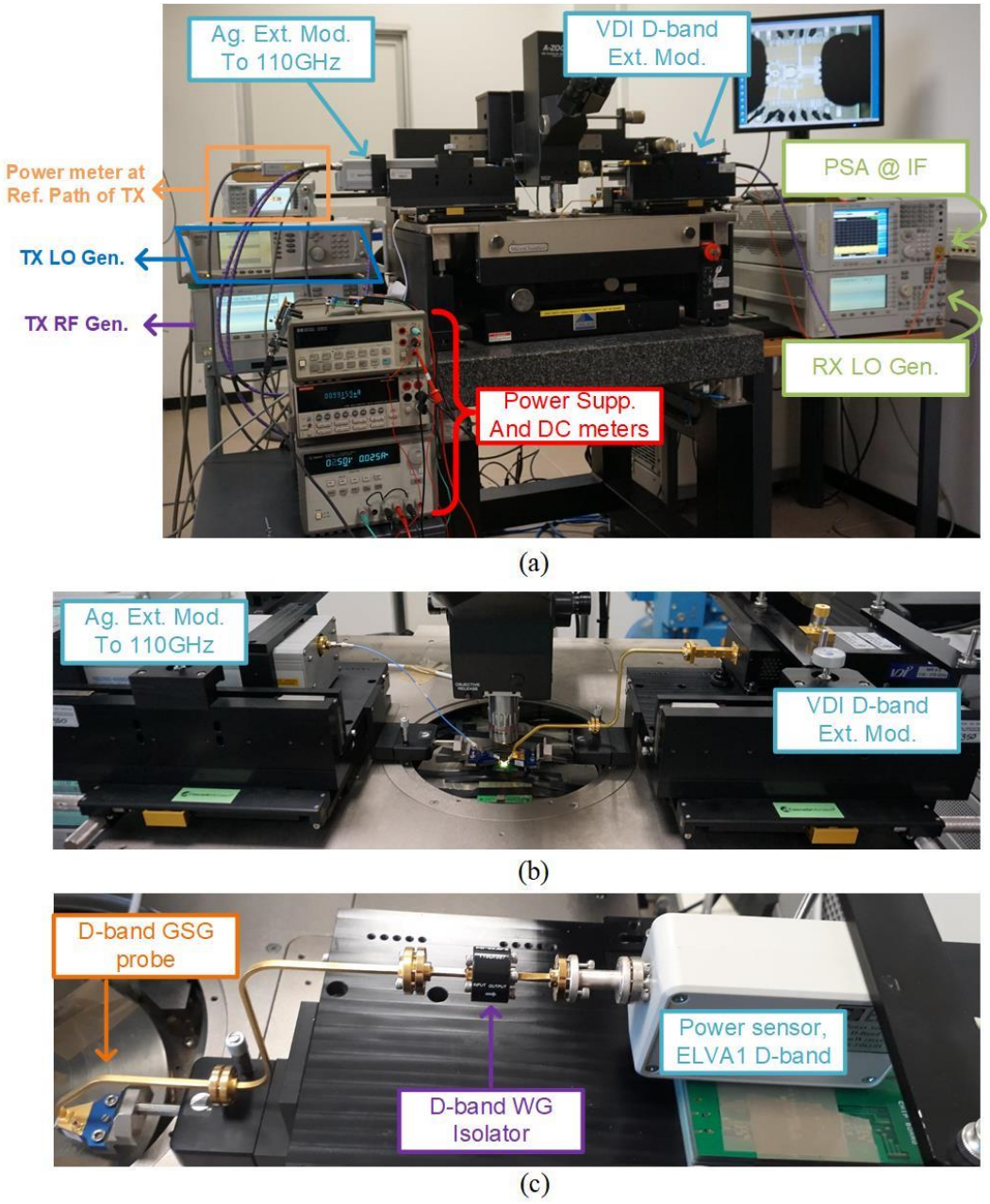


Figure 3.6. (a) Measurement setup for the D-band doubler, (b) Down converting the D-band output spectrum and measuring with PSA, (c) measuring directly using power meter.

each frequency.

Having this frequency dependent offset in hand, a D-band signal can be down-converted to an IF band and monitored by a spectrum analyser. Figure 3.6 shows a complete setup in which the E-band signal is generated using an E-band VNA extension module and the D-band signal is down-converted and monitored by a spectrum analyser. Note that in both IF paths, there are amplifiers with low-pass characteristics, which means the usable bandwidth of these paths is limited and much smaller than the D-band spectrum. Therefore, the D-band Spectrum was

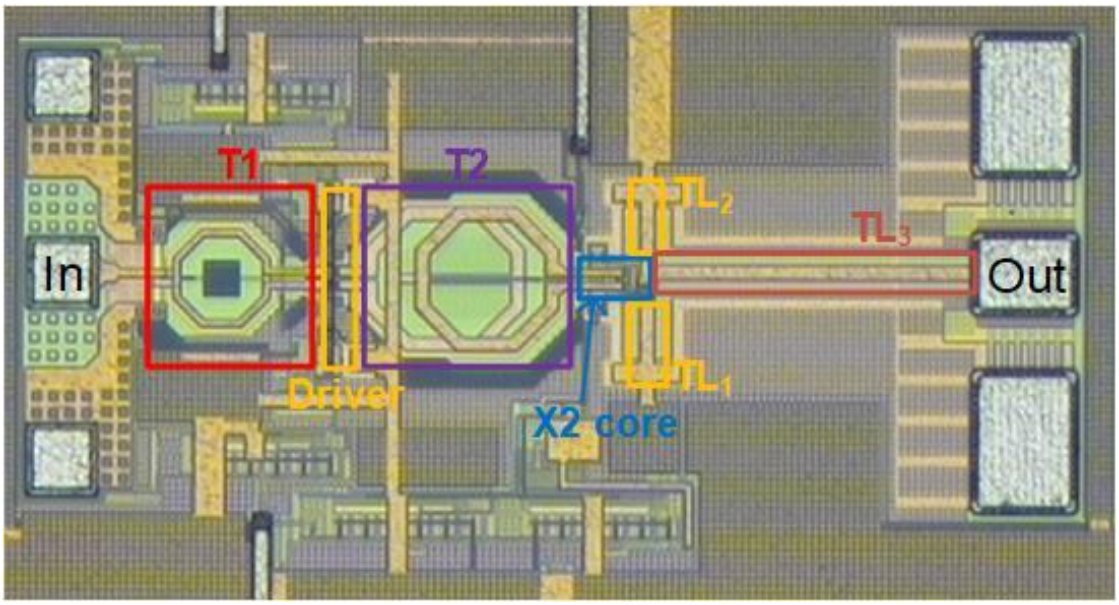


Figure 3.7. Microphotograph of the D-band doubler

down-converted to smaller windows to reconstruct the full D-band spectrum. Reconstruction of the spectrum is not merely an act of concatenating the small windows together, because there are practical challenges to address such as harmonic spurs in the LO and images. In Appendix II some details are presented about reconstruction of the D-band spectrum. To double check the precision of the absolute values of the readings, the D-band output can also be measured using a power meter, as shown in Figure 3.6c.

A microphotograph of the realized frequency doubler is shown in Figure 3.7. All the simulations were done using the Spectre engine and the inductors and transmission lines were modeled using EMX which is a 2.5D electromagnetic simulator. The performance of the test chip was experimentally verified at two different supply voltages, V_{CC}=2V and V_{CC}=3V. Figure 3.8 shows the output power and leakage of the fundamental frequency component versus frequency with P_{in} constant at -5dBm. With V_{CC}=2V, the output power, P_{out}, peaks at 4.3dBm at 130GHz, and the corresponding power conversion gain is 9.3dB. P_{out} stays above 0dBm from 114GHz to 148GHz, corresponding to 26% fractional bandwidth. With the supply voltage increased to 3V, the output power at center frequency rises to 8.1dBm, and the conversion gain to 13.1dB. P_{out} is maintained above 0dBm from 108 GHz to 155GHz, corresponding to a fractional bandwidth of 35.7%. The leakage of the fundamental component was measured from 55GHz to 70GHz due to instrument limitations and it is better than 32dBc for both supply voltages.

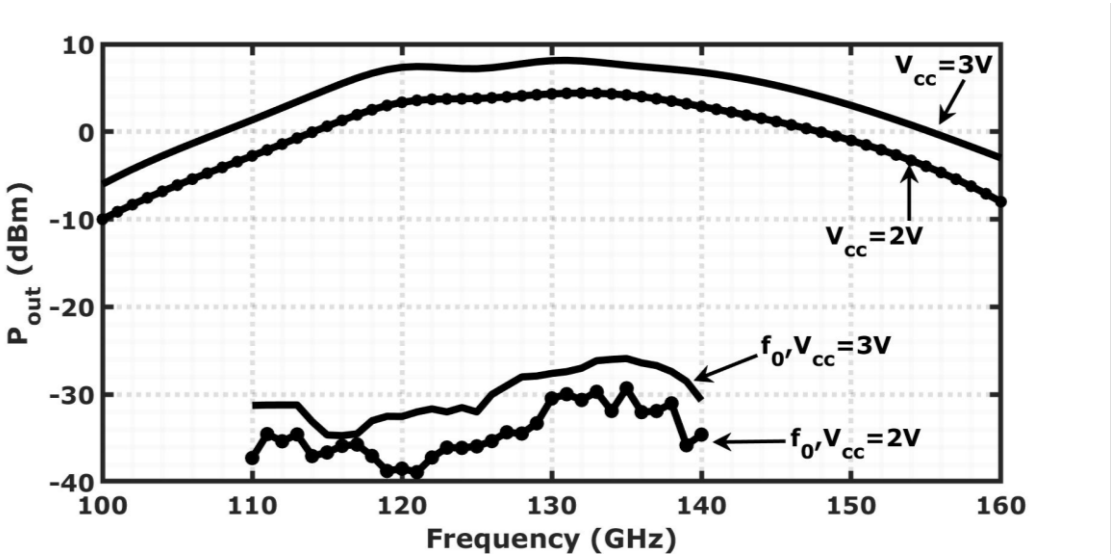


Figure 3.8. Pout and leakage of the fundamental tone versus frequency with Pin=-5dBm

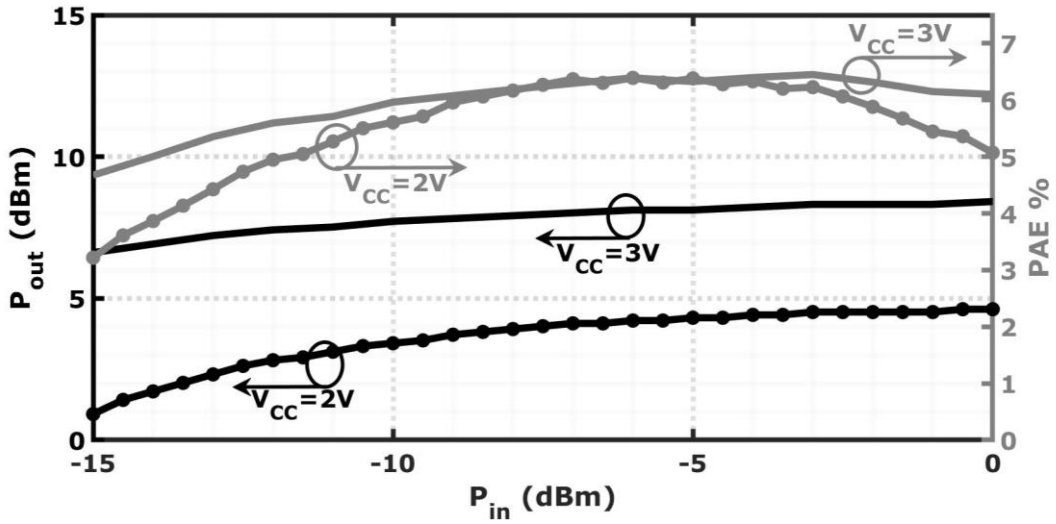


Figure 3.9. Pout and PAE versus Pin at 130GHz

Figure 3.9 shows the output power and PAE vs P_{in} at 130GHz for V_{CC}=2V and 3V. In both cases, the variation of P_{out} is less than 2dB for P_{in} > -12dBm and P_{out} saturates to the maximum value for P_{in} > - 5dBm. At 2V supply, the on-chip driver and the doubler core draw respectively 7.4mA and 11.3mA, corresponding to 37.4mW total power dissipation. With the supply voltage raised to 3V, the DC current of the doubler core is increased to 26mA and the total DC power dissipation is 97.5mW. From Figure 3.9 the PAE reaches the same maximum value of 6.3%, with the two supply voltages, at P_{in} = -5dBm.

The measured performances are summarized in Table 3.1 and compared against previously reported frequency doublers with the output frequency close to or above 100GHz, mostly in BiCMOS technology. The proposed frequency doubler demonstrates the highest conversion

gain, PAE and, with 3V supply, the highest output power.

In order to provide a quantitative measure for comparison of the mmWave frequency multiplier designs while taking into account the technology differences, a figure of merit (FoM) is proposed[6]:

$$FOM = 100 * CG \times \left(\frac{f_{out}}{f_{max}}\right)^2 \times \frac{P_{out}}{P_{DC}} \quad (3.4)$$

The conversion gain (CG) is normalized to $(f_{max}/f_{out})^2$ because, at given output frequency, f_{out}, it takes advantage from a higher intrinsic device power gain, which is proportional to f_{max} [50]. Moreover, higher output power needs higher DC power consumption and the FoM normalizes P_{out} to P_{DC}. The calculated FoM is reported in the last column in Table 3.1. At 2V and 3V supplies, the presented frequency doubler reaches respectively 4x and 9x higher FoM compared to previous works.

Table 3.1. Measurement summary and comparison with doublers with outputs in D-band

Ref	Tech/ f_{max}	f_{out}* (GHz)	P_{out}** (dBm)	CG** (dB)	P_{DC} (mW)	PAE** (%)	FoM
This work, V_{CC}=2V	BiCMOS / 330GHz	114-148 (26%)	4.3	9.3	37.4	6.35	9.5
This work, V_{CC}=3V	BiCMOS / 330GHz	108-155 (36%)	8.1	13.1	97.5	6.3	21
[46]	BiCMOS / 500GHz	136-174 (24.5%)	5.6	3.8	36	5.88	2.32
[47]	BiCMOS / 350GHz	105-135 (25%)	6.5	1.5	40	3.26	1.85
[21]	BiCMOS / 330GHz	101-128 (23.6%)	1	0	69	0	0.22
[42]	BiCMOS / 330GHz	105-137.5 (27%)	3	-2.5	32	<0	0.47
[43]	BiCMOS /NA	128-138	-2.9	-3.6	>7.2	<0	NA
[44]	28nm CMOS /NA	105-135 (25%)	3	-2.2	14	<0	NA
[45]	65nm CMOS /250GHz	95-150 (45%)	3	-8	22.8	<0	0.33

* Above 0dBm. Estimated from plots for other works.

** At peak P_{out}

The initial target for the doubler's output frequency range was 140-160GHz. However, the measurements showed a frequency downshift from 150GHz to 130GHz, thus all the characterizations were reported based on the actual measured performance. However, the

[6] To the best of the author's knowledge, no FoM has been proposed in the literature for this type of circuits.

minimum DREAM requirement for output power was larger than -10dBm in the frequency range of interest and the results shown in Figure 3.8 show that the doubler can be safely integrated in the D-band radio despite this frequency shift. The reason for the difference between simulations and measurements has been investigated and partly traced back to the inaccuracies in modeling of the passive elements in the output matching network. In particular, TL_1-TL_3 were laid out around the tightly merged Q_3 and $Q_{1,2}$ (see Figure 3.7), and shared a common ground plane which served as the current return path for all of the transmission lines. Therefore, it was not possible to define a separate ground point for each of the transmission lines. In the EM simulations, a common ground point was defined for TL_1-TL_3 and it was where the ground mesh around $Q_{1\text{-}3}$ met the bottom plate of C_T as the local ground of the circuit, where eventually all the return currents had to circulate back into the branch comprised of $Q_{1,2}$ and Q_3. Moreover, since the whole structure was too big to be simulated at once and with high precision, it was both broken down to smaller pieces and the precision options of the EM simulator were relaxed. These simplifications and the vague definition of the ground associated with each transmission line made the modeling prone to errors. i.e., the effective inductance of TL_1 was modeled less than the real value. Hence, the real oscillation frequency was lower than simulations as it is primarily set by the equivalent inductance of TL_1. Another plausible reason for the discrepancy is that the STMicroelectronics' design kit is experimentally validated only up to 110GHz, hence the simulations were based on extrapolations of the models. Therefore, some inaccuracies in the models of the active devices are also expectable.

Figure 3.10 shows a comparison between the measured and simulated output reflection

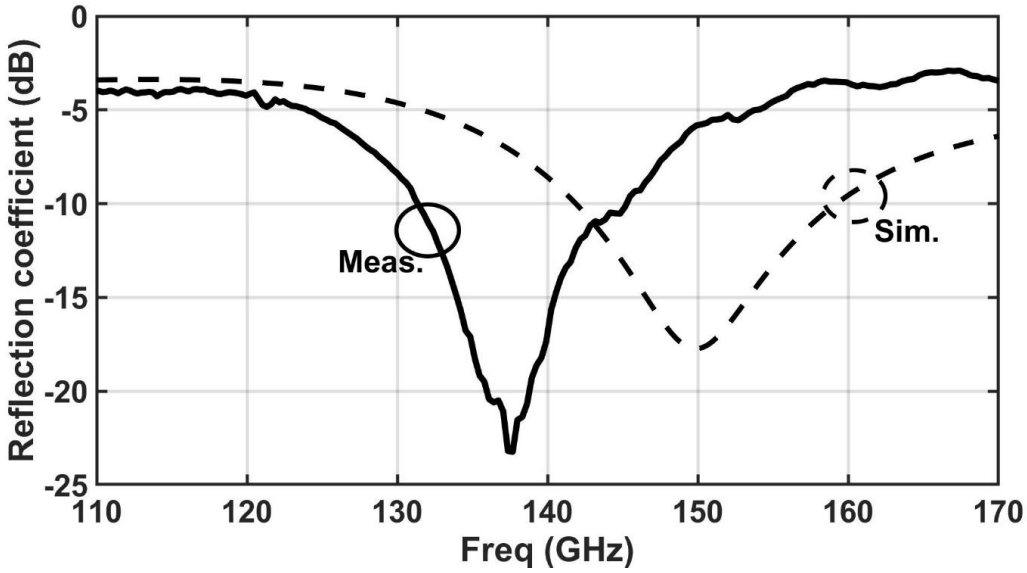


Figure 3.10. Output reflection coefficient of the doubler chip

coefficients. The downshift in the frequency of the notch indicates that the resonance frequency of the output network was lower than simulated, and so was the free running frequency of the oscillator. Therefore, the peak output power was delivered close to the actual free running frequency, which was around 130GHz.

Chapter 4 Summary and future work

4.1 Summary

A frequency multiplication chain was designed to provide LO at mm-wave frequencies to be used in a D-band wireless transceiver, within the framework of the DREAM project. The frequency multiplication chain was designed to up-convert the input LO signal from X-band to D-band using a multiplication factor of 12. This multiplication factor was realized in two separate chips, a frequency multiplier by 6 followed by a frequency doubler with output at D-band.

Multiplication by 6 in the first chip was achieved by cascading a tripler and a doubler. A novel circuit topology was proposed for the tripler circuit. The active core was devised to approximate the trans-characteristic of a 3rd order polynomial that generates only the 3rd harmonic of a sinusoidal input signal. The tripler circuit was implemented in a 55nm SiGe-BiCMOS technology as a separate break-out chip. Measurements showed that the driving signal and the 5th harmonic were suppressed over >15dB variations of the input amplitude, thanks to an envelope detector circuit that configures parameters of the circuit to accommodate to the input signal level. Moreover, the circuit demonstrated the highest reported suppression of the undesired tones over 16% factional bandwidth. In comparison to the previously reported works in the literature, the proposed solution demonstrated > 10dB improvement of undesired harmonic tones rejection with operation bandwidth and core power dissipation aligned with state of the art.

A frequency doubler followed by an output buffer were cascaded after the tripler to realize the frequency multiplier by 6 chip. A differential input and differential output topology was proposed for the doubler circuit which was based on the conventional push-push doubler. The output buffer was based on injection locking technique to improve efficiency and signal purity at the output. Output of the sextupler chip peaked to 1.7dBm at 74.4GHz when driven with a 0dBm input signal, and remained within 3dB variation from 65.5GHz to 83.5GHz, corresponding to 24% fractional BW. In this frequency range, the leakages of all harmonics are below -30dBc and at the center frequency are as low as -50dBc. Moreover, in the BW required for the DREAM project (70-80GHz), all harmonics are suppressed by more than 40dBc. In addition, at center frequency, the output saturated when the input power reached -3dBm, and from -3dBm to 10 dBm, variation of the output power was limited to 1dB. Also,

the harmonic rejection ratio was better than 40dBc for input power larger than -4dBm. Compared to previously reported works, the main advantage of the presented work is high suppression of the undesired harmonics at the output while the bandwidth and efficiency are aligned with the state of the art.

The D-band doubler, the second chip of the frequency multiplication chain, included a pre-driver and a core doubler. The core doubler circuit comprised a push-push pair for second-harmonic generation, and a stacked common-collector Colpitts oscillator which works as a common-base injection-locked amplifier to boost the conversion gain and output power. As a result, the power conversion gain of the frequency doubler is increased by up to 10dB, compared to the push-push pair alone. The proposed frequency doubler delivered P_{out} up to 8dBm at 130GHz with 13dB conversion gain and 6.3% Power Added Efficiency. Moreover, P_{out} variation was less than 2dB for P_{in} > -12dBm and P_{out} saturated to the maximum value for P_{in} > - 5dBm. A Figure of Merit was proposed to benchmark frequency doublers and the presented chip showed up to 9 times improvement compared to previously reported designs in the same frequency range. At a short glance, the presented frequency multipliers demonstrated the highest power conversion gain with output power and PAE aligned or better than previously reported frequency doublers in silicon operating in the same frequency range.

In summary, measurement results of the test chips showed superior performance with respect to the previously reported works in the literature and passed the performance requirements of the DREAM project. At the time of writing this thesis, a demonstrator of the DREAM's D-band radio is already designed and assembled, in which a high frequency RF-board hosts the chipset, including the proposed sextupler chip and the D-band doubler which is integrated inside the up/down converters. The Flip-Chip bonding process is undergoing and experimental results of the full transceiver will be available by the end of the project schedule, early 2021.

4.2 Future work

There were several novelties incorporated in the design of the circuits throughout this research activity. Some of these techniques offer prospects of improving the performance of the available designs toward more efficiency and robustness. For example, the technique used in the D-band frequency doubler was an aggressive and risky design approach because the circuit components were made of the parasitic elements of the transistors which suffer

uncertainty in their precise values. However, the results appeared to be very promising and superior to the previously reported techniques. Therefore, it makes sense to investigate its principles more deeply to arrive at more reliable design approaches, and/or make modifications to the circuit topology to further improve the achievable performance.

Nevertheless, there are many other established ideas and design approaches that were not adopted in this work because their advantages were not in the interest of the DREAM project. For example, distributed designs offer very wide bandwidth and are very suitable for use at mm-Wave as the size of passive elements shrinks at these frequencies. However, low signal purity is a main drawback of these designs. Combining the techniques and the know-how achieved in this research with the well-established techniques can lead to designs that offer wide bandwidth, high efficiency, high signal purity, and robustness at the same time. For example, a frequency multiplier whose output covers the whole D-band spectrum (from 110 to 170GHz) with other metrics aligned with the state of the art can offer a robust and general solution for all the transceivers working in the this frequency range.

Appendices

Appendix I

In section 2.2 the analysis was shown for the case in which the tripler and doubler were approximated by only two terms. In this appendix the same analysis is performed by including the 4th and 5th order non-linearity terms to approximate performances of the doubler and tripler respectively. Also a more realistic scenario was considered by obtaining the nonlinearity coefficients such that the 4th and 5th harmonics were 10dB lower than the fundamental leakage at the output of each block when excited by a single tone. Assuming the input to be of the form $x = \cos(\omega_0 t)$ and that the doubler is balanced and memoryless, i.e. it does not generate odd-order harmonics and the operation frequency is low enough, its output can be approximated by the following polynomial:

$$y = \frac{3}{2(3\rho - 4)}\, x + x^2 + \frac{4}{3\rho - 4} x^4 \qquad \text{(A.1)}$$

Where ρ is the doubler's suppression of the tone at f_0 with respect to $2f_0$. Similarly, assuming the same input and that the tripler is balanced, the tripler's output can be approximated by the following polynomial:

$$w = \frac{9\gamma - 8}{4(3\gamma - 5)}\, x + x^3 + \frac{4}{3\gamma - 5} x^5 \qquad \text{(A.1)}$$

Where γ is the tripler's suppression of the tone at f_0 with respect to $3f_0$. Following the same approach as in section 2.2, two possibilities for the order of the multipliers are considered: *Tripler first* and *Doubler first.*

A. Doubler First:

When the doubler is the first block in the chain, its input is a single tone at ω_0. Therefore, using (A.1) and omitting the DC component, it's output can be approximated by:

$$y = \frac{1}{\rho} \operatorname{Cos}(\omega_0 t) + \operatorname{Cos}(2\omega_0 t) + \frac{1}{3\rho} \operatorname{Cos}(4\omega_0 t) \qquad \text{(A.3)}$$

The doubler's output is then fed to a tripler. In this case, the tripler's output can be obtained by substituting (A.3) in (A.2). Keeping only the tones closest to the desired tone $(6\omega_0 t)$, the output will be:

Appendix

$$w \cong H4\,\mathrm{Cos}(4\omega_0 t) + H5\,\mathrm{Cos}(5\omega_0 t) + H6\,\mathrm{Cos}(6t) + H7\,\mathrm{Cos}(7\omega_0 t) + H8\,\mathrm{Cos}(8\omega_0 t) \tag{A.4}$$

Where:

$$H4 = \frac{2980 + 7290\rho + 7695\rho^2 + 1539\gamma\rho^2 + 6075\rho^3 + 2187\gamma\rho^3 - 243\rho^4 + 2187\gamma\rho^4}{972(-5 + 3\gamma)\rho^5}$$

$$H5 = \frac{19 + 260\rho + 360\rho^2 + 90\rho^3 + 54\gamma\rho^3 + 45\rho^4 + 81\gamma\rho^4}{36(-5 + 3\gamma)\rho^5}$$

$$H6 = \frac{630 + 965\rho + 2025\rho^2 + 243\gamma\rho^2 + 1935\rho^3 + 81\gamma\rho^3 + 243\gamma\rho^5}{324(-5 + 3\gamma)\rho^5} \tag{A.5}$$

$$H7 = \frac{290 + 1800\rho + 1215\rho^2 + 81\gamma\rho^2 + 810\rho^3 + 486\gamma\rho^3 + 405\rho^4}{324(-5 + 3\gamma)\rho^5}$$

$$H8 = \frac{45 + 180\rho + 580\rho^2 + 270\rho^3 + 45\rho^4 + 81\gamma\rho^4}{108(-5 + 3\gamma)\rho^5}$$

From equations (A.5) it can be seen that the relative values of H4-H8 with respect to H6 can be numerically evaluated by assigning values to ρ and γ.

B. Tripler First:

Following the same approach as in the previous case, the normalized output of a balanced tripler excited by a single tone at ω_0 can be approximated by using (A.2):

$$y = \frac{1}{\rho}\,\mathrm{Cos}(\omega_0 t) + \mathrm{Cos}(3\omega_0 t) + \frac{1}{3\rho}\,\mathrm{Cos}(5\omega_0 t) \tag{A.6}$$

The tripler's output is then fed to a doubler. In this case, the tripler's output can be obtained by substituting (A.6) in (A.1). Keeping only the tones closest to the desired tone $(6\omega_0 t)$, the output will be:

$$w \cong H4\,\mathrm{Cos}(4\omega_0 t) + H5\,\mathrm{Cos}(5\omega_0 t) + H6\,\mathrm{Cos}(6t) + H7\,\mathrm{Cos}(7\omega_0 t) + H8\,\mathrm{Cos}(8\omega_0 t) \tag{A.7}$$

Where:

Appendix

$$H4 = \frac{49 + 168\rho + 108\rho^2 + 18\gamma\rho^2 + 48\rho^3 + 54\gamma\rho^3}{18(-4 + 3\gamma)\rho^4}$$

$$H5 = \frac{1}{2(-4 + 3\gamma)\rho}$$

$$H6 = \frac{40 + 84\rho + 168\rho^2 + 18\gamma\rho^2 + 27\gamma\rho^4}{18(-4 + 3\gamma)\rho^4}\} \quad \text{(A.8)}$$

$$H7 = 0$$

$$H8 = \frac{9 + 44\rho + 27\rho^2 + 24\rho^3 + 9\gamma\rho^3}{9(-4 + 3\gamma)\rho^4}$$

Similar to the previous case, the relative values of H4-H8 with respect to H6 can be numerically evaluated by assigning values to ρ and γ. Assuming $\rho = \gamma = 30$ to evaluate equations (A.5) and (A.8) gives the results listed in Table A.1 which are graphically depicted in Figure 2.3.

Table A.1. Numerical values for harmonic ratios based on equations (A.5) and (A.8)

	$\frac{H6}{H4}$	$\frac{H6}{H5}$	$\frac{H6}{H7}$	$\frac{H6}{H8}$
Doubler first, (A.5)	20dB	20dB	47dB	29dB
Tripler first, (A.8)	23dB	68dB	∞	32dB

Appendix II

In this section the procedure of combining the windows of the D-band spectrum down-converted to IF and reconstructing the D-band spectrum is described. The D-band spectrum was down-converted by moving the LO signal in 1.2GHz steps to cover an IF range between 600MHz and 1800MHz. Then, these windows of the spectrum were concatenated to obtain the full D-band spectrum.

After concatenation, the spectrum needs some more processing to remove the images and *false tones* from the spectrum. *False tones* here refer to the tones that appear in the down-converted spectrum but are not truly present in the associated frequency, i.e $f_{IF} + f_{LO}$ (f_{IF} being the frequency of the tone inside the IF window and f_{LO} being the frequency of the applied LO). This happens because the built-in multiplier of the LO is not ideal and generates tones at integer harmonics of the input LO, as well as the 12^{th} harmonic and these spurious tones create the *false tones*. As an example, if a tone at 132.6GHz enters the *waveguide test* port, it appears at 600MHz IF if LO frequency is equal to 132GHz. However, if we rise the LO to 158.4GHz, the 10^{th} harmonic of the input LO appears at 132GHz, down converts the input tone to 600MHz, and falsely indicates a tone at 159 or 157.8GHz. We used a simple trick to overcome this issue, which was moving the LO frequency slightly up or down and checking if the tone under investigation moved by the same value in the expected direction. Moving the LO frequency by Δf, causes the IF tone to move in the spectrum by the same amount, while the false tones move by a different value, $\frac{10}{12}\Delta f$ in the above example. Figure A.1 shows the flowchart of this algorithm that was developed to obtain a true spectrum. Not shown in this chart, for each frequency first the input power was set using the reading from the power meter connected to the *Reference IF* port of the transmitter module and the offset data corresponding to that frequency obtained before. Once the input was set, the algorithm was run to obtain the output spectrum for that input.

As this procedure seems very time consuming and prone to human mistakes, all measurements were done in an automated manner. All instruments were connected to a PC using GPIB[7] interface to receive commands and send back data. A basic code was written for each instrument using SCPI[8] commands or native languages of instruments, all in MATLAB or C++. These basic codes were used inside more top-level routines to perform the desired

[7] General Purpose Interface Bus
[8] Standard Commands for Programmable Instruments

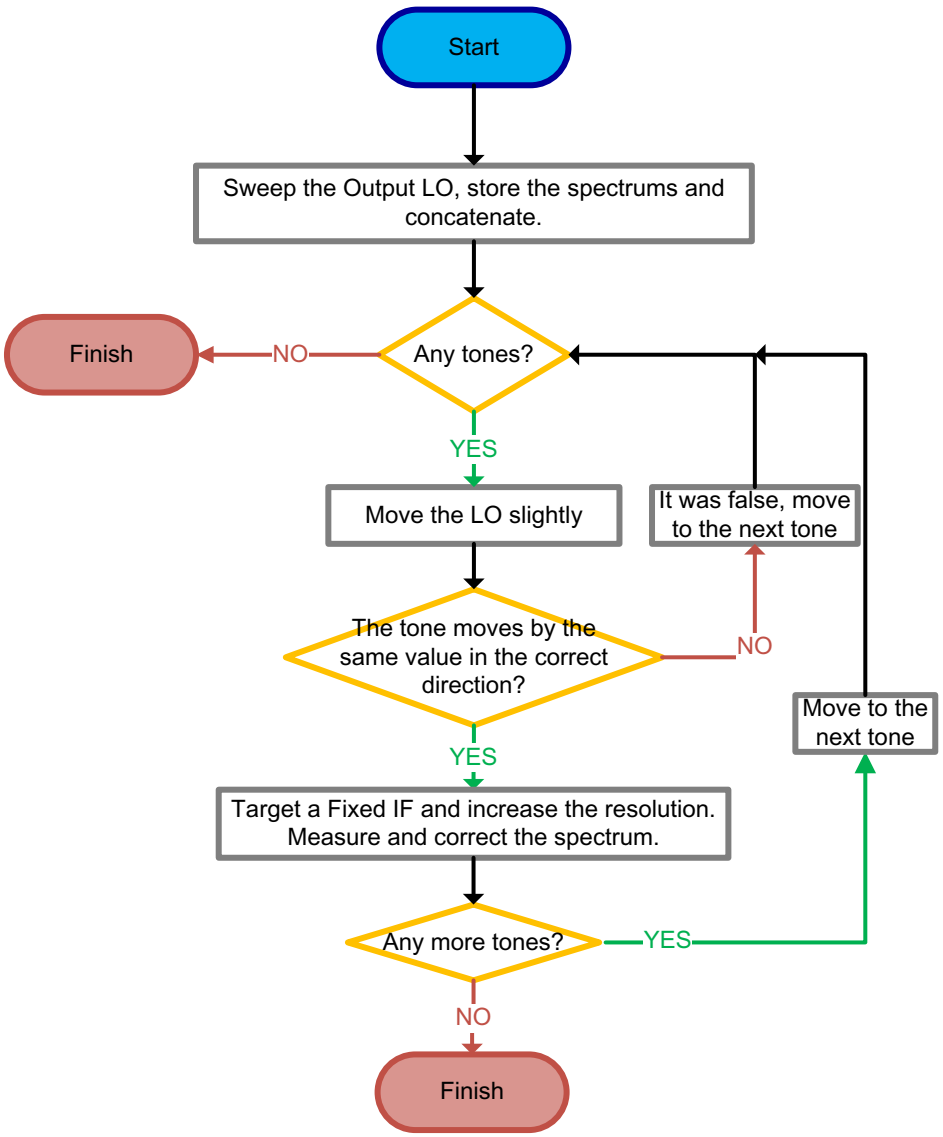


Figure A.1. Flowchart of the algorithm developed for cleaning the spectrum from false and image tones.

measurements, such as sweeping the frequency at a fixed input power, sweeping the input power at a fixed frequency, etc , while incorporating algorithms such as the one described. In order to facilitate these measurements (and similarly characterization of the instruments and measuring of the losses before doing the measurements), graphical user interfaces (GUI) were developed to show the progress of the routines in real time. Figure A.2 shows a GUI used for measurement of the D-band doubler chip.

Appendix

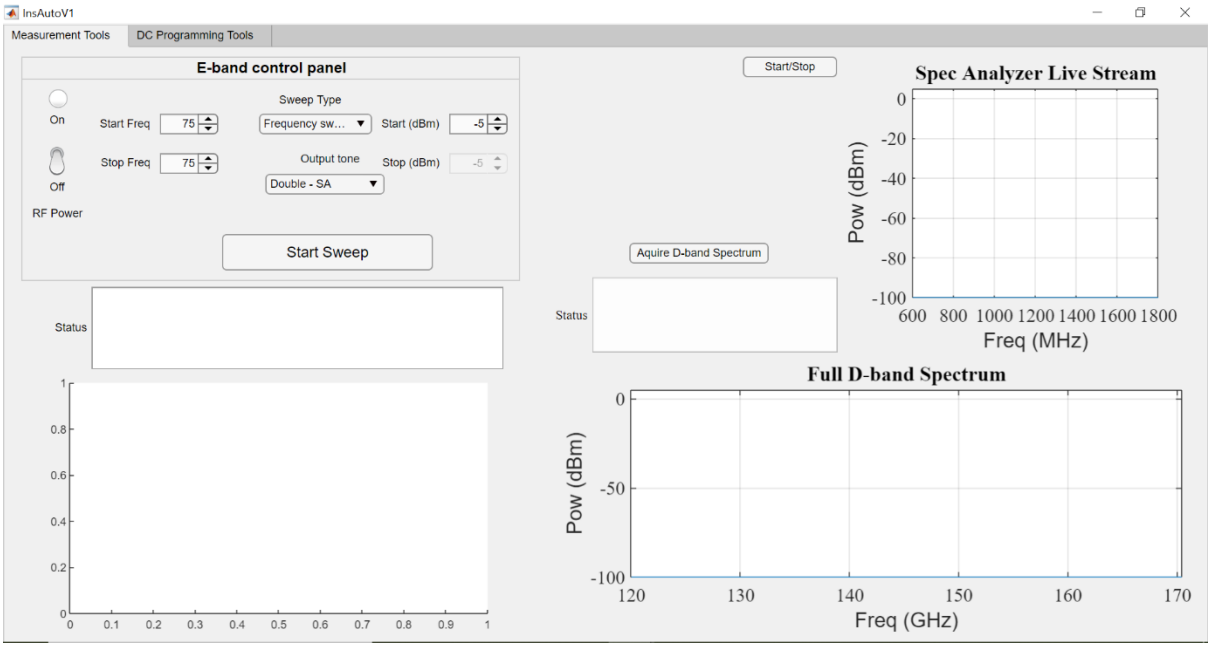


Figure A.2. GUI developed to facilitate measurement of the D-band doubler

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