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Highly–Linear Full-Duplex Receiver with Auxiliary Path and Adaptive Self-Interference Cancellation

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Abstract

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Highly Linear Full-Duplex Receiver with Auxiliary path and Adaptive Self-Interference Cancellation

by Dario Prevedelli

The demand of larger RF bandwidths and more efficient transceiver architectures have pushed many research groups to investigate a new emerging technique called Full-Duplex (FD). The FD paradigm potentially increases the spectral efficiency of a factor of two compared to well-known architectures like Time Division Duplexing (TDD) and Frequency Division Duplexing (FDD). Since transmission and reception are done simultaneously, the main challenge is caused by the transmitter (TX) leakage which falls in the receiving (RX) path and potentially degrades its signal integrity. The required TX suppression varies from 90 to 120dB. To reach this target, the FD receiver requires many different cancellation processes. The first suppression employs a hybrid transformer which is a four ports network that interfaces TX, RX, Antenna ports and Balancing Impedance. The Balancing Impedance emulates in frequency the antenna's one. Once this condition is fulfilled, the hybrid transformer behaves like an ideal circulator and the transmitter is electrically isolated by the receiver. The antenna impedance can change rapidly in frequency, therefore, only 40dB of isolation (ISO) is considered a reachable value. The second cancellation process is realized with a Digital-to-Analog (DAC) converter that works in current mode. The DAC's goal is to cancel out the residual TX leakage current at the output of the

first receiver building block, the Low Noise Transconductance Amplifier (LNTA). To provide a proper current in both magnitude and phase, an adaptive digital filter mimics the receiver impulse response and minimizes the correlation between the received and transmitted signals. The adaptive filter can suppress only linear contributions which are strictly correlated to the TX signal. The third cancellation process removes the TX noise/distortion contributions by the main receiving path. In this case, a mixer-first auxiliary receiver (AUX-RX) down-converts only the TX signal. Then, another adaptive digital filter combines the two receivers' output to get extra cancellation. Thanks, to this last cancellation, the main receiver is immune to TX-EVM. The AUX-RX is also suitable to suppress reciprocal mixing effect. The receivers have been implemented in TSMC 28nm technology. The main and auxiliary receivers have gain, NF and In-Band IIP3 of 33/-7dB, 6.4/42dB and 15/56dBm, respectively. The AUX-RX has competitive SNDR compared to other works in literature. System simulations show an overall TX suppression larger than 90dB with less than 2dB of NF degradation.

In this manuscript two other works are illustrated with measurement results. The former is a mixer-first topology designed in TSMC 40nm to prove that high SNDR is achievable. The latter is another receiver which employs a Single-Ended to Differential LNA. Its application is focused on Multi-Input-Multi-Output (MIMO) and Carrier Aggregation (CA) scenarios where the count pad is critical. In this last work the baseband gain, the NF and the Out-of-Band IIP3 are 48dB, 3,4dB and -3,7 dBm, respectively. This chip has been designed in TSMC 28nm technology and occupied an active area of 0.08mm^2. Its power consumption is 22mW.

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3) A Mixer-1st Auxiliary Receiver for analog Self-Interference Cancellation and S2D LNA for MIMO and CA scenarios

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Abbreviations

FDD……..Frequency-Division Duplexing

TDD…….Time-Division Duplexing

BS…….Base Station

SoC……...System on Chip

FD……..Full-Duplex

OOB……..Out-of-Band

IB……In-Band

NF……..Noise Figure

AUX……..Auxiliary

D2S……..Differential to Single ended

S2D…….Single ended to Differential

RX……Receiver

TX……Transmitter

BW……..Bandwidth

PA……Power Amplifier

SI…….Self-Interference

LMS…….Least-Mean-Square

MSE……Mean-Square Error

FIR……..Finite Impulse Response

EVM……Error Vector Magnitude

PSK……Phase Shift Keying

QAM…..Quadrature Amplitude Modulation

DAC…...Digital-to-Analog Converter

ADC…...Analog-to-Digital Converter

ENOB…Equivalent Number of Bit

OSR…...Over-Sampling Ratio

DEM……Dynamic Element Matching

DWA…..Data Weighted Averaging

RTZ……Return-To-Zero

OTA……Operational Transconductance Amplifier

TIA……..TransImpedance Amplifier

LNA…….Low Noise Amplifier

FF……FeedForward

SNDR….Signal-to-Noise-Distortion Ratio

SQNR….Signal-to-Quantization-Noise Ratio

ISO……..Isolation

FoM……Figure of Merit

RF……..Radio Frequency

BB…….BaseBand

IL……Insertion Loss

RL……..Return Loss

VSWR…Voltage Standing Wave Ratio

Q…….Quality Factor

MIMO…..Multi-Input-Multi-Output

CA……..Carrier Aggregation

CG……..Common Gate

CS……..Common Source

MGTR…Multi Gate TRansistors

LO…….Local Oscillator

DSP…..Digital Signal Processing

SNR…..Signal Noise Ratio

SDR…..Signal Distortion Ratio

IIP3……Input third Intercept Point

SAW….Surface Acoustic Wave

XC…….Cross-Coupled

CM…….Common-Mode

PM…….Phase Margin

PART 1

Toward Full-Duplex Transceivers Basic Concepts and Challenges

This chapter is focused on the analysis of standard communication solutions and to highlight the main challenges of a new emerging topology called "Full-Duplex". In the end, some basic RF concepts and metrics are introduced.

1.1 Standard solutions to communicate

The technology scaling and the costs reduction requirements have pushed the electronic world to integrated more sophisticated systems in a single chip (SoC). Today, a wireless device can manage many different communication standards with their own bands and modulation schemes [1]. The entire sub-6GHz spectrum is now completely busy. Currently, the most used standards to communicate are simply two: the Frequency-Division Duplexing (FDD) and the Time-Division Duplexing (TDD). The former foresees to simultaneously send and receive data using two different bands, while the latter shares the same band using two different time slots. In Fig. 1.1 a simplified description of the two schemes is shown. In both topologies, the presence of a duplexer filter at the transceiver input is mandatory to relax linearity requirements in subsequent stages. Indeed, the transmitted signal behaves like a blocker (or jammer) for the receiver (RX) which potentially degrades signal integrity. The filtering effect is often accomplished by an off-chip Surface Acoustic Wave (SAW) filter which are expensive, bulky and difficult to tune in frequency. Moreover, their extensive use in modern architectures like Multi-Input-Multi-Output (MIMO) and Carriers Aggregation (CA), it would bring a huge area consumption and unacceptable increment of costs [2]. Recently, SAW-less solutions have shown their effectiveness in FDD/TDD architectures. Their functionality is based on an integrated Radio Frequency (RF) high-linear filter which is easier to tune in frequency. Then, the main filtering effect is shifted in baseband domain. In this way, the off-chip filters are not anymore required but the receiving path needs more linearity to face transmitter (TX) leakage and RF blockers [2], Fig. 1.2.

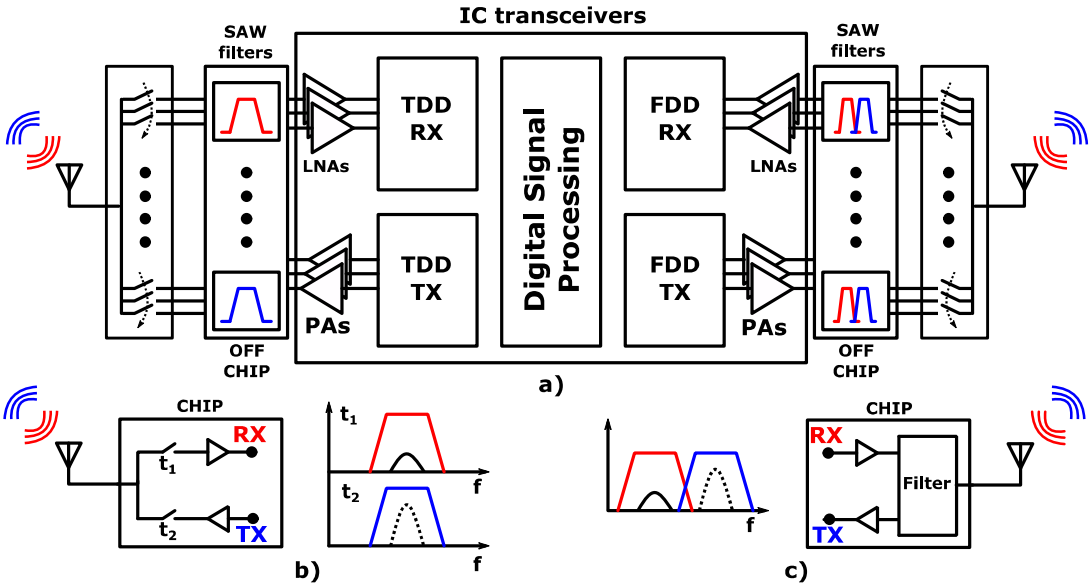


Fig. 1.1: a) A generic TDD/FDD transceiver architectures with off-chip SAW filters. b), c) The highlights of their spectrums.

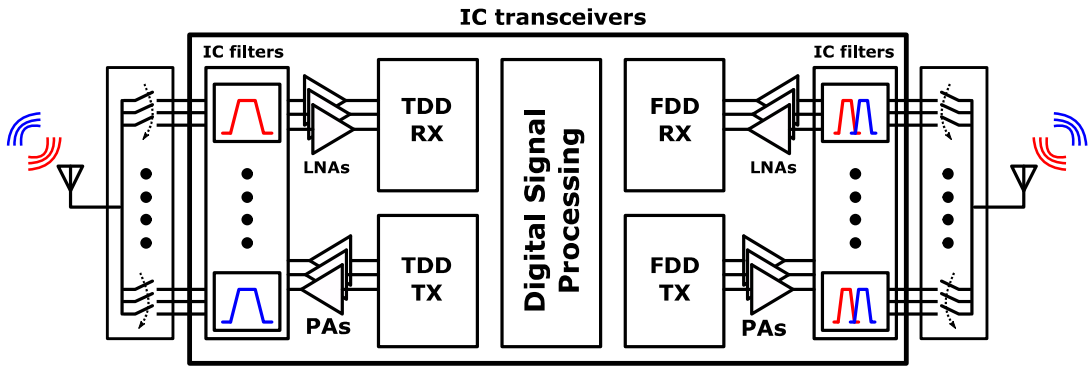


Fig. 1.2: A SAW-less TDD/FDD transceiver architectures with integrated RF filters. In other solutions, the filters can be removed to shift the entire filtering effect in baseband domain.

1.2 Full-Duplex Paradigm

In previous sub-section, the FDD and TDD techniques are introduced. Their spectral efficiency is at least affected by a factor of two than a Full-Duplex architecture [3]. Indeed, in TDD, the available band is share in two different time slots, while in FDD two RF bands are mandatory. On the contrary, a FD solution foresees to simultaneously transmits and receives data using the same band. However, this scenario opens new challenges that in previous architectures are mitigated or not present at all:

1. The TX power is leaked in the RX band and potentially saturates the receiver.
2. The RX needs higher linearity to manage In-Band (IB) TX leakage.

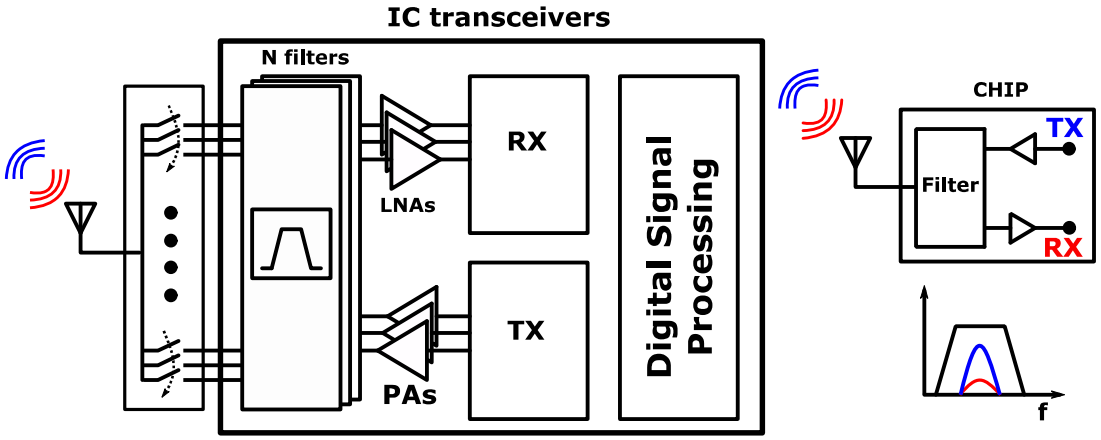


Fig. 1.3: A generic FD transceiver with integrated RF filters. On the right, the spectrum differences compared to TDD/FDD topologies.

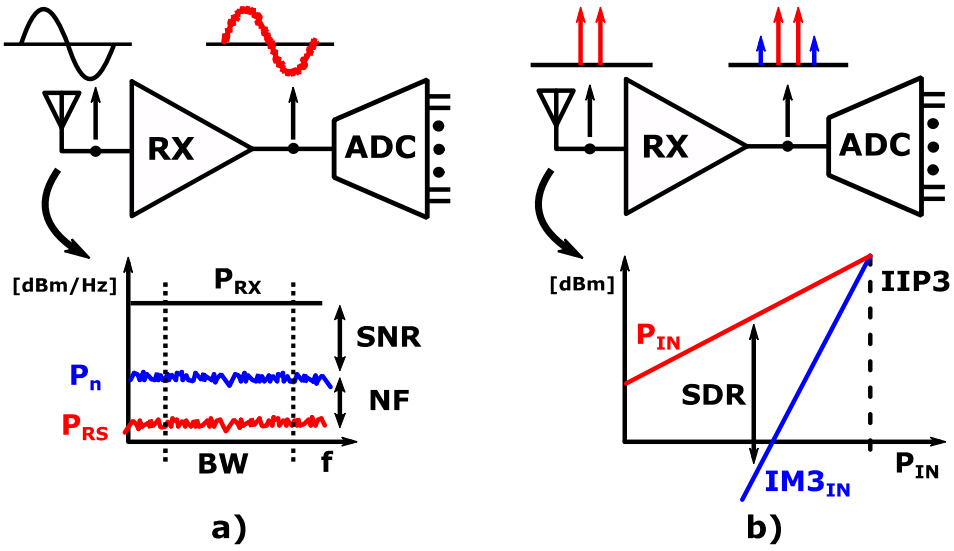


Fig. 1.4: The input-referred noise and distortion plots. a) The definition of SNR, NF and noise floor. b) The non-linear response with graphical description of IIP3, SDR and $IM_{3,in}$.

3. The TX leakage develops in-band reciprocal mixing.
4. The TX noise and distortion increase the receiver noise floor.

All these challenges must be faced carefully to design a reliable FD receiver and some of them, as will be shown in chapter 2, become the bottlenecks of the entire system. Despite these challenges, the FD transceiver is currently under investigation by several research groups for its potential benefit in data throughput and new generation devices [4]. In Fig. 1.3 a building block FD transceiver is shown.

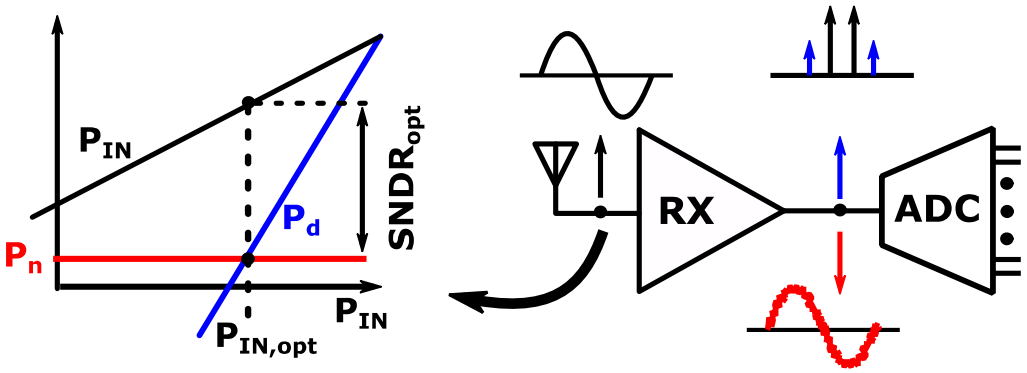


Fig. 1.5: The input-referred receiver noise and distortion. On the left, the definition of $SNDR_{opt}$.

1.3 Useful metrics

1.3.1 Signal to Noise Ratio (SNR)

Any electronic circuit develops an electric noise which is superimposed to the received signal. The noise is generally uncorrelated to the signal and it can be analysed with statistic theories. The SNR is a useful metric to understand the signal degradation due to the noise presence. The formula is reported below:

$$\mathrm{SNR} = \frac{\mathrm{P_{sig}}}{\mathrm{P_n}} \tag{1.1}$$

$\mathrm{P_n}$ and $\mathrm{P_{sig}}$ are noise and signal powers, respectively. When, the SNR is equal to 0dB, the signal power is equal to the noise one.

1.3.2 Receiver Sensitivity and Noise Figure

The receiver sensitivity is the minimum detectable input power and is expressed as:

$$\mathrm{P_{sens}} = \mathrm{P_{RS}}|_{\mathrm{dBm/Hz}} + \mathrm{NF}|_{\mathrm{dB}} + 10\log(\mathrm{BW}) + \mathrm{SNR}|_{\mathrm{dB}} \tag{1.2}$$

$\mathrm{P_{RS}}$ is the input-referred antenna noise and is equal to -173.8dBm/Hz. The receiver bandwidth and the Signal-to-Noise Ratio depend on the modulation format and are indicated as BW and SNR, respectively. The Noise Figure (NF) describes the receiver noise performance:

$$\mathrm{NF} = \frac{\mathrm{SNR_{IN}}}{\mathrm{SNR_{OUT}}} \tag{1.3}$$

The larger is the receiver noise contribution and larger will be the NF. The sum of the first three terms in equation (1.2) is also called receiver “noise floor” and it represents the receiver input-referred integrated noise.

$$\text{Noise Floor} = \mathrm{P_n}|_{\mathrm{dBm/Hz}} = \mathrm{P_{RS}}|_{\mathrm{dBm/Hz}} + \mathrm{NF}|_{\mathrm{dB}} + 10\log(\mathrm{BW}) \qquad (1.4)$$

This value is important to determine other important constraints like linearity. Indeed, the receiver distortion must be smaller than the noise floor to avoid significant degradation on the final SNR.

1.3.3 Linearity

The transfer function of any electronic device can be expressed through a third order Taylor’s series as below:

$$\mathrm{Y} = \mathrm{a_1 X} + \mathrm{a_2 X^2} + \mathrm{a_3 X^3} \qquad (1.5)$$

X, Y are the input and the output signals, respectively. The linear gain is represented trough $\mathrm{a_1}$, while $\mathrm{a_2}$ and $\mathrm{a_3}$ are the non-linear components of second and third order. When, the signal X is a single tone of amplitude A and frequency ω_1, the equation (1.5) becomes:

$$\mathrm{Y} = \mathrm{a_1 A}\cos(\omega_1 \mathrm{t}) + \mathrm{a_2 A^2}\cos^2(\omega_1 \mathrm{t}) + \mathrm{a_3 A^3}\cos^3(\omega_1 \mathrm{t}) \qquad (1.6)$$

Focusing on third order component, the equation (1.6) is now:

$$\mathrm{Y} = (\mathrm{a_1 A} + \frac{3\mathrm{a_3 A^3}}{4})\cos(\omega_1 \mathrm{t}) + \mathrm{a_2 A^2}\cos^2(\omega_1 \mathrm{t}) + \cdots \qquad (1.7)$$

The first part of (1.7) is constituted by the linear coefficient plus a new contribution due to third order distortion. In general, the $\mathrm{a_1}$ and $\mathrm{a_3}$ signs are opposite which determine a gain compression on the linear part. The input power which determines a deviation by the linear behaviour of 1dB, is called 1dB compression/extension point.

Another metric is derived by a two tones test. In this case, the signal X in (1.5) must be substituted by two tones having equal magnitude but different frequencies (ω_1, ω_2). The third order behaviour develops two spurious tones which can fall in the operating band ω_0 degrading its signal integrity. Considering, two input tones $\mathrm{A}\cos(\omega_1 \mathrm{t})$, $\mathrm{A}\cos(\omega_2 \mathrm{t})$ and (1.5), the equivalent equation becomes:

$$Y = a_1 A(\cos(\omega_1 t) + \cos(\omega_2 t)) + a_2 A^2(\cos(\omega_1 t) + \cos(\omega_2 t))^2 + a_3 A^3(\cos(\omega_1 t) + \cos(\omega_2 t))^3 \quad (1.8)$$

$$Y = \frac{3}{4} a_3 A^3[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] + \cdots \quad (1.9)$$

If one of two intermodulation tones in (1.9) is equal to ω_0, the linear component is degraded. The metric which describes this effect is called “Input Third Intercept Point” (IIP3) and it is also described as

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad (1.10)$$

$$IIP3 = \frac{P_{in} - IM_{3,in}}{2} + P_{in} \quad (1.11)$$

A_{IIP3} in (1.10) is the input that develops a spurious signal with equal magnitude. The IIP3 is defined by (1.11) where P_{in} and $IM3_{in}$ are the input tones and the input-referred intermodulation powers, respectively. Like SNR in (1.1), it is possible to define another metric called Signal-to-Distortion Ratio (SDR):

$$SDR = \frac{P_{sig}}{P_d} \quad (1.12)$$

In Fig.1.4 are shown the IIP3 and Noise Floor. In (1.13) is shown another equation to describe the second-order distortion. In this case, the metric used is called “Input Second Intercept Point” (IIP2).

$$IIP2 = 2P_{in} - IM_2, in \quad (1.13)$$

The non-linear contribution in (1.13) is greatly reduced if the system employs a fully-differential or “balanced” topology [5-7].

1.3.4 Signal to Noise-Distortion Ratio Optimum ($SNDR_{OPT}$)

Considering the previous equations, it is possible to derive the best achievable SNDR. The SNR and SDR have different trends referred to the input signal power. The former is directly proportional, while the latter is inversely proportional. Therefore, it exists an input power that develops a SNDR optimum. In detail, when the distortion power is equal to the receiver noise floor, Fig. 1.5.

$$SNR = SDR = \frac{P_{sig}}{P_n} = \frac{P_{sig}}{P_d} \Longrightarrow P_n = P_d \quad (1.14)$$

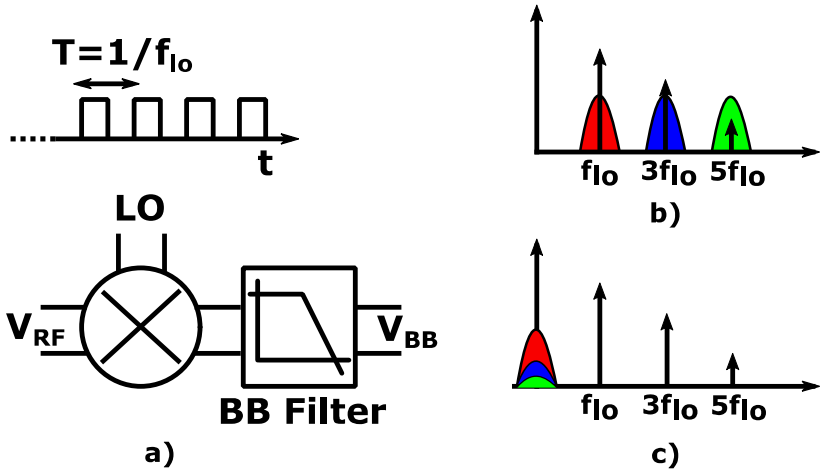


Fig. 1.6: The harmonic mixing effect. a) A generic mixer driven by a square wave clock. b) The spectrum referred to the mixer input with the spurious tones. c) The spectrum at the receiver output after mixing effect.

$$\mathrm{P_n} = \text{Noise floor} = \mathrm{P_d} = \mathrm{IM_{3,in}} = 3\mathrm{P_{in}} - 2\mathrm{IIP3} \tag{1.15}$$

$$\mathrm{P_{in,opt}} = (\text{Noise floor} + 2\mathrm{IIP3})/3 \tag{1.16}$$

$$\mathrm{SNDR_{opt}} = \frac{\mathrm{P_{in,opt}}}{\mathrm{P_d}} \tag{1.17}$$

$\mathrm{P_{in,opt}}$ represents the input signal which provides the best SNDR.

1.3.5 Harmonic mixing

To convert an RF signal to a digital information, its spectrum is first shifted at low frequency thanks to a mixer device [1]. This process is also called down-conversion. The mixer is generally driven by a square wave signal which can be expressed using the Fourier's series, as follow:

$$\mathrm{X}(\omega) = \sum_{\mathrm{n}=1}^{\infty} \frac{2\mathrm{A}}{\mathrm{n}\pi} \sin\left(\frac{\mathrm{n}}{2}\pi\right) \delta(\omega_{\mathrm{lo}} - \mathrm{n}), \quad \mathrm{n} = \mathrm{odd} \tag{1.18}$$

A is the square wave amplitude while $\delta(\omega)$ is the delta function. The spectrum in (1.18) has infinite tones equally spaced by multiples of ω_{lo}. The first harmonic, which has the higher coefficient, is used to down-convert the RF wanted signal while the other tones down-convert unwanted bands which increase the receiver noise floor. This effect is called harmonic mixing, Fig. 1.6 [8].

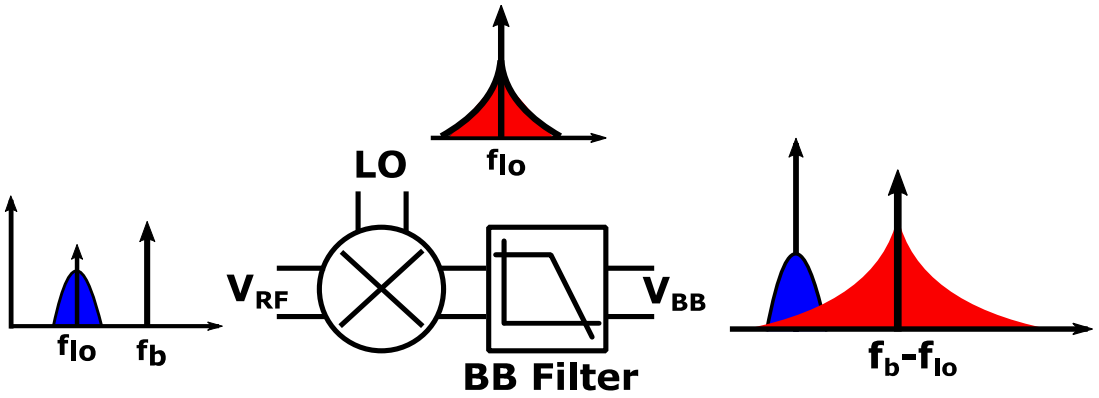


Fig. 1.7: The reciprocal mixing effect. At the input, the wanted signal (blue) and a blocker (black). At the output, the convolved phase noise degrades the receiver noise floor.

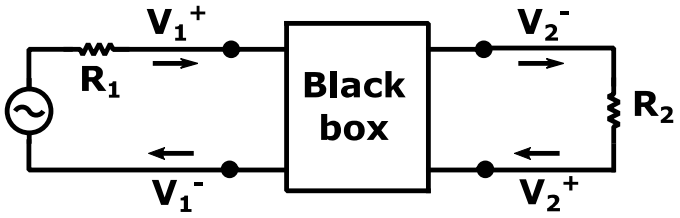


Fig.1.8: A generic 2-ports black box with input and output waves.

1.3.6 Reciprocal mixing and phase noise

The formula in (1.18) represents an ideal clock spectrum. In practice, the mixer is driven by a noisy clock with bell-shapes spectrums, Fig.1.7. This kind of noise is also called “phase noise”. Considering a single tone, the phase noise (Φ_n) can be represented as follow:

$$X(t) = A\cos(\omega_{lo}t + \Phi_n(t)) \qquad (1.19)$$

The noisy clock limitation rises clearly when a large out-of-band blocker is down-converted. The result is baseband signal convolved with the mixer’s phase noise. Now, a part of its noise falls in the receiver band degrading the RX noise floor. The phase noise is referred to the input signal in dBc. A possible solution to mitigate this problem is to employ selective RF filters at the receiver input.

It is important to highlight a critic scenario when the blocker is very close or superimposed to the received signal as in FD receivers. In this singular situation, the receiver noise floor may be fully dominated by reciprocal mixing [9].

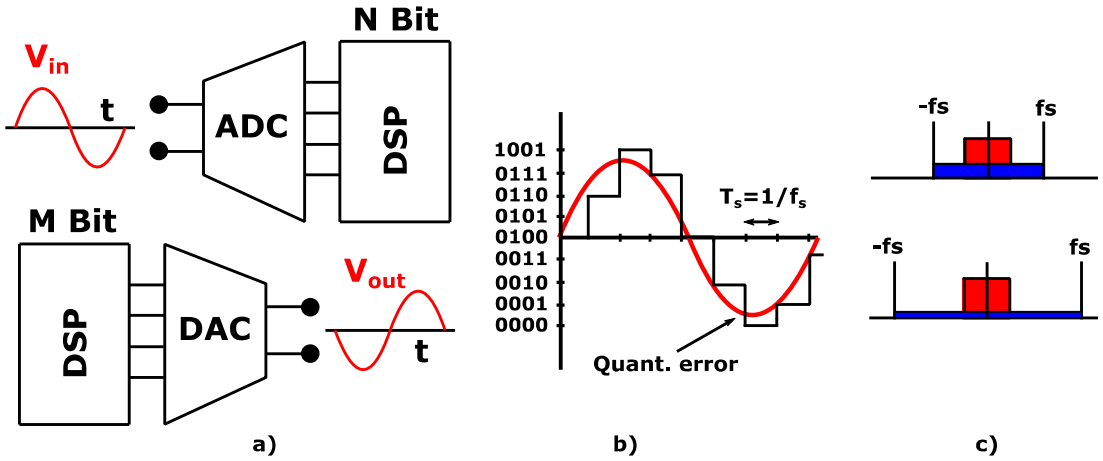


Fig. 1.9: a) The building block representation of DAC and ADC. b) An intuitive description of quantization noise. c) In blue the quantization noise spectrum vs the sampling frequency.

1.3.7 S-parameters

The S or "scattering" parameters are used to describe the frequency response of a black box. They are set in a quadratic matrix of order N, where N is the number of ports. Considering the plot in Fig. 1.8, an unknown two ports box is described as follow:

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} \tag{1.20}$$

where s_{nm} are the scattering parameters and V^+ ,V^- are the incident and the reflected power waves, respectively. The s_{11} can be expressed as:

$$s_{11} = \frac{V_1^-}{V_1^+} \text{ for } V_2^+ = 0 \tag{1.21}$$

fixing V_2^+ to zero, the s_{11} is the power ratio between the reflected and the incident waves at input port 1. In other words, it represents the input matching. The s_{21} can be expressed as:

$$s = \frac{V_2^-}{V_1^+} \text{ for } V_2^+ = 0 \tag{1.22}$$

This parameter represents the amount of power delivered to the output load. It is also called network gain [10].

1.3.8 Basic converter parameters

An analog information is generally converted in digital domain being easier to manage, store and manipulate [11-12]. The Analog-to-Digital (ADC) converter

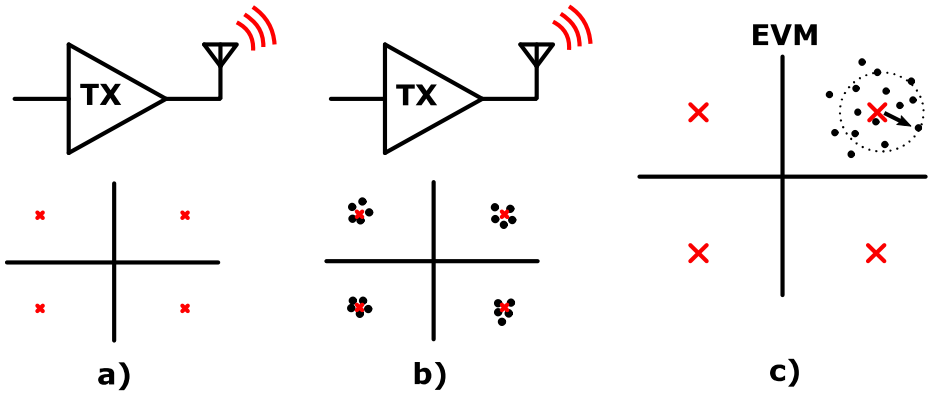


Fig. 1.10: a) An ideal QAM constellation, b) real transmitted symbols, c) definition of EVM.

Table 1.I: Release 14

Constellation	EVM [dBc]
QPSK or BPSK	-15
16 QAM	-18
64 QAM	-21.9
256 QAM	-29

EVM values from Release 14 version 14.3.0.

generates a stream of bit from an analog signal while the Digital-to-Analog (DAC) converter performs the opposite operation. Both these devices are used to connect the two worlds: analog and digital. A relevant property is their resolution which is determined by the number of bit and the sampling frequency. Below the definition of Signal-to-Quantization-Noise Ratio (SQNR) for any kind of converter:

$$\mathrm{SQNR} = 6.02 * \mathrm{ENOB} + 1.76 + 10\log\left(\frac{\mathrm{f_S}}{2 * \mathrm{BW}}\right) \tag{1.23}$$

$\mathrm{f_S}$ is the sampling frequency which must be at least twice signal bandwidth (BW) to respect Nyquist's theorem. Every time the sampling frequency is increased by a factor of 2, the SNQR is improved of 3dB that is equivalent to gain 0.5bit in resolution. The Equivalent Number-Of-Bit (ENOB) represents the effective number of bits of a converter. In general, in Nyquist converters, this number is always smaller than the physical number of bits being degraded by converter noise and distortion. The SQNR, which is generally represented in dB provides the difference in power between a full-scale signal and the noise/distortion powers, Fig.1.9.

1.3.9 EVM

A communication system foresees to send and receive data trough electrical signals which have different phases and magnitudes between each other [1]. To improve data throughput, the RF systems communicates through symbols which are mapped in a constellation scheme. Some of the most important are: Phase Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM). Ideally, the transmitter should provide an output signal equals to an available symbol. In practice, due to the transmitter noise and distortion, the output symbol has a causal deviation by the expected value, Fig. 1.10. The metric which describes this deviation is called Error Vector Magnitude (EVM) and is expressed as:

$$\mathrm{EVM} = \frac{1}{\mathrm{P_{avg}}}\frac{1}{\mathrm{N}}\sum_{\mathrm{j=1}}^{\mathrm{N}} \mathrm{e_j^2} \tag{1.24}$$

where e is the magnitude error and $\mathrm{P_{avg}}$ the average signal power. This parameter is referred to the TX output power in dBc. Some EVM values from Release 14 version 14.3.0 are illustrated in Table 1.I [13].

PART 2

A Full Duplex Receiver with Adaptive TX Leakage Cancellation

This chapter is focused on a Full-Duplex receiver suitable for 5G applications. Starting from their challenges to the design implementation, all the building blocks are analysed and discussed. In the end, the simulations results are shown together with a comparison table.

2.1 Challenges and previous works

As introduced in the previous chapter, the Full Duplex paradigm foresees to transmit and receive data simultaneously employing the same band. Its main challenge is caused by transmitter leakage (TX-leakage) or self-interference (SI) which leaks in the receiving path. In the best scenario, when the receiver (RX) is not clipped by TX-leakage, the received signal is completely covered by it, Fig. 2.1. In mobile devices, the TX output power is larger than 20dBm. To preserve receiver functionalities and performance, the TX-leakage power should be reduced below the RX noise floor. With the market demands for higher data throughput, the current receivers need bandwidths in the order of tens of MHz setting their noise floor to almost -90dBm. Therefore, the required echo-suppression must be large as 100/120dB.

In literature other works tried different strategies to improve the overall TX-to-RX isolation. One solution employs two antennas or non-magnetic circulator among TX and RX paths. Unfortunately, only 20-25dB of isolation has been proving in measurements [14-15]. On-chip circulators can provide 40dB of echo reduction, but they have limited TX power handling capability. In any case, all these solutions are far away from achieving more than 100dB of total TX-leakage suppression. A different approach is shown in Fig. 2.2 [16-17]. It exploits two analog Finite Impulse Response (FIR) filters. The former provides a first rough RF cancellation in the LNA input, the latter a larger BaseBand (BB) TX-leakage suppression at the receiver output. This architecture has proved 80dB of total echo reduction, where 30dB are provided by a wideband off-chip circulator. Despite the consistent TX-isolation improvement, this approach has important drawbacks that potentially limit any further improvement or practical employment:

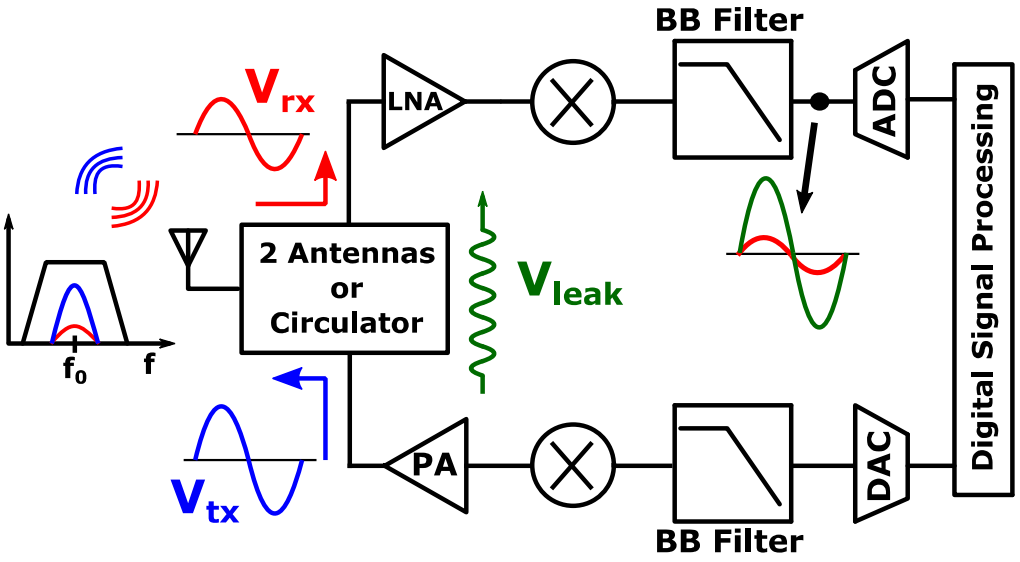


Fig. 2.1: A generic Full-Duplex transceiver. The transmitted and received signals are shown in blue and red, respectively. In green, the TX-leakage in the RX path.

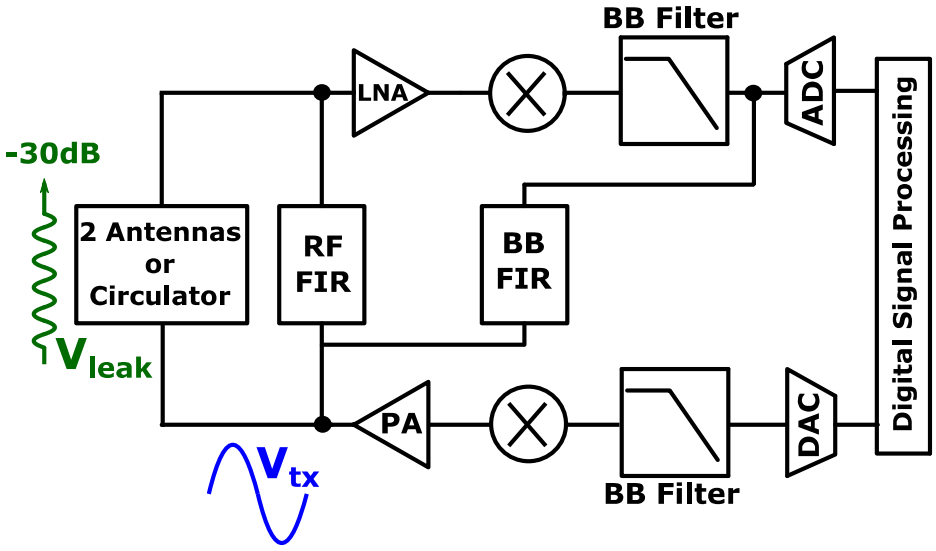


Fig. 2.2: A transceiver topology which has realized 80dB of TX-isolation. Two FIR filters suppress TX leakage in both RF and BB domains.

- The cancellation bandwidth increases proportionally with the analog FIR filters order. Hence, to achieve wider bandwidths results in injecting more uncorrelated noise in the receiver.
- Active cancellers handle large input signal and high linearity is mandatory.
- Active cancellers power consumption is considerable in the receiver power breakdown.

Also digital cancellation techniques have been exploring but only 30dB of isolation has been proved in literature [4-18].

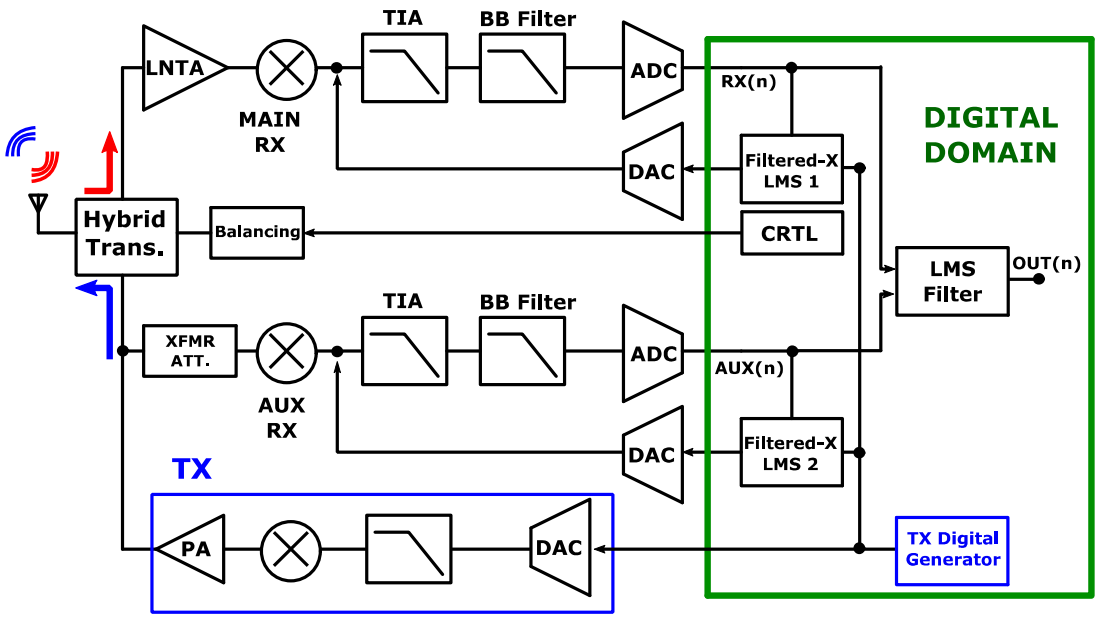


Fig. 2.3: The proposed FD transceiver with adaptive self-interference cancellation. In the green block, the whole digital part with three LMS adaptive filters. On the top, the main receiver with the DAC output connected to TIA input. In the middle, the auxiliary receiver and in the blue block the off-chip transmitter.

In summary, the common trend in the FD receiver design is to employ different cancellation processes to improve TX-leakage isolation. At RF, a wideband device (e.g. a passive component) provides a first rough isolation. Then, an analog echo-canceller is realized with a digital support. In the next sub-section, a FD receiver which provides an isolation larger than 80dB and overcomes many of the previous drawbacks is analysed and presented.

2.2 The proposed architecture

The proposed architecture is shown in Fig. 2.3. The transmitter, the receiver and the antenna ports are connected in RF domain through a hybrid transformer. In well defined conditions, the hybrid transformer behaves like an ideal circulator which electrically isolates the TX/RX path. This block can provide a first integral isolation of 40dB. The TX-leakage is a filtered version of the TX signal, which is the result of the frequency-dependent mismatch between the antenna and the balancing impedances. After the hybrid transformer, a standard direct conversion receiver until the ADC output is designed. The TIA input is connected to a current-

mode DAC whose goal is to cancel out any residual TX-leakage coming from the mixer output. The DAC provides an output current with equal magnitude but opposite phase with respect to the TX-leakage. The cancellation process must be performed precisely to avoid adding any unwanted signal in the RX path. The proper required current depends on two main factors: the transmitted symbol and the whole system impulse response which is time and temperature dependent. A Filtered-X Least-Mean-Square (Filtered-X LMS) digital filter adaptively sets up the system impulse response and provides proper codes to the DAC. The Filtered-X LMS filter can track only linear impulse response and strictly related to the ideal transmitted signal. Therefore, the TX noise and distortion cannot be cancelled though this technique. The Table 1.I in the previous chapter shows some EVM values referred to TX output power. With a TX output power of 20dBm, the receiver noise floor would be fully degraded by TX-EVM. To overcome this limitation, the Power Amplifier (PA) output is connected to an auxiliary receiver (AUX-RX) which detects only the TX signals, including its noise and distortion. An attenuator reduces the input power to relax linearity requirements in the subsequent stages. Then, another DAC is employed to cancel the TX linear component in the auxiliary receiver. Finally, in fully digital domain, an LMS Finite-Impulse-Response (LMS-FIR) filter combines the two receivers' outputs to properly cancel TX-EVM.

In summary, the architecture provides three cancellations:

1. The hybrid transformer provides a first rough SI-cancellation in RF domain.
2. The DAC cancels the residual TX-leakage in baseband with the help of a digital support, the Filtered-X LMS filter.
3. The auxiliary receiver together with a digital LMS-FIR filter suppress TX-EVM.

A potential receiver limitation is the reciprocal mixing between the noisy clock and the SI-leakage. As introduced in (1.3.6), this effect would fully degrade the main receiver noise floor. Moreover, this effect is exponentially greater than FDD/TDD applications being the blocker In-Band. To mitigate this problem, DACs and mixers share the same clock making the system reciprocal mixing insensitive.

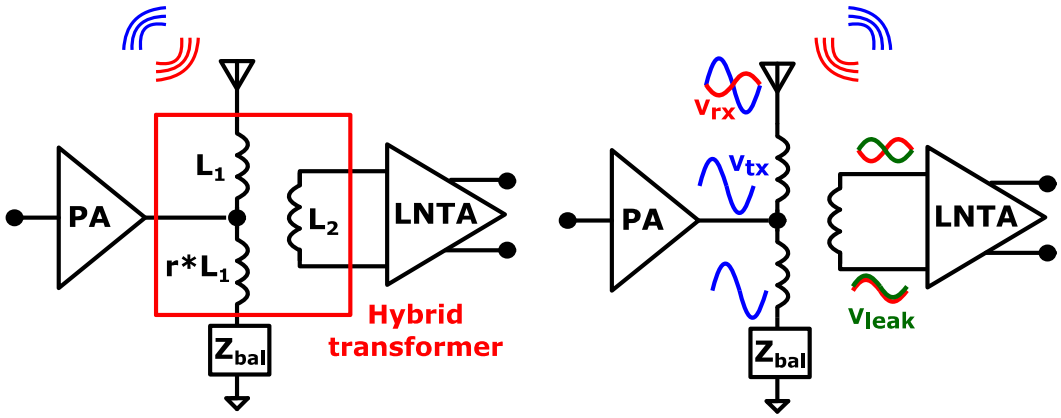


Fig. 2.4: A hybrid transformer that interconnects TX and RX paths. On the right, a simplified time-domain description of the isolation effect.

2.2.1 Hybrid Transformer and Balancing Impedance

The hybrid transformer is a passive 4-ports network which interconnects TX-to-RX path, Fig.2.4 [19-24]. The TX output node is connected to the primary center-tap while the receiver input to the secondary coil. The last two ports are connected to the antenna and to a passive network called “Balancing Impedance”. The Balancing Network aims to emulate the antenna impedance in its working band. When this condition is fulfilled, the hybrid transformer behaves like an ideal circulator which electrically isolates the TX-RX path. Intuitively, the TX output power (blue in Fig. 2.4) is equally split between the antenna and the balancing impedances. This condition develops in the primary coil a common-mode signal which is cancelled out in the secondary. On the contrary, the received signal (red) is mainly present on the antenna node and it electrically passes through the receiving path. The amount of Self-Interference power suppressed through the hybrid transformer is called “Isolation” or “ISO” and is expressed as:

$$\mathrm{ISO} = \frac{\mathrm{G_{TX}}}{\mathrm{G_{ANT}}} \tag{2.1}$$

$\mathrm{G_{TX}}$ and $\mathrm{G_{ANT}}$ are the TX output and the antenna nodes to RX input transfer functions, respectively. Once the balancing condition is ensured, the hybrid transformer has two important impacts in the transceiver performance: the RX NF and the TX Insertion Loss (TX-IL) are at least 3dB.

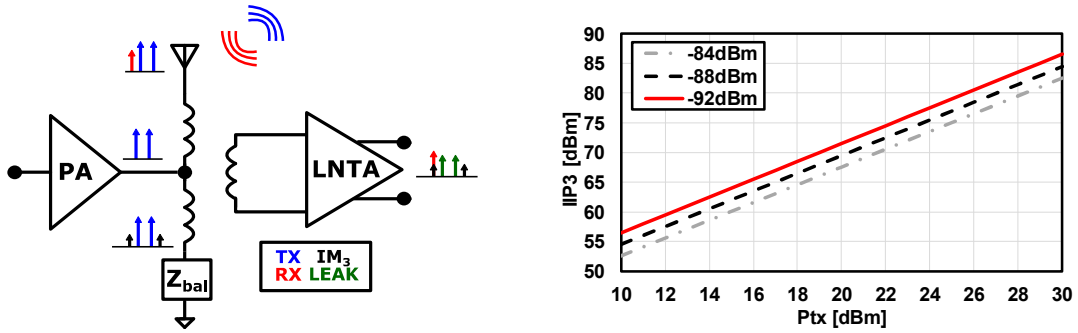


Fig. 2.5: The hybrid transformer behaviour in frequency domain with the balancing distortion. The picture highlights its minimum required linearity to get a distortion power equals to the receiver noise floor.

In a desired scenario, a wideband balancing condition would provide large SI-ISO in the entire working band. In practice, the frequency-dependent antenna impedance makes this condition impossible. Therefore, a tuneable balancing impedance is mandatory. In the past, tuneable RC loads have been employed showing their effectiveness in applications where the impedance variation is limited. In many commercial handheld devices, the antenna impedance has also inductive behaviour which cannot be covered with RC solutions. On the contrary, resonant LC networks can overcome this limitation and cover a larger set of impedances.

Another important aspect is the balancing impedance linearity. With 20dBm of TX output power, an insertion loss (IL) of 4dB, a receiver noise floor of -88dBm ($\mathrm{P_n}$), the minimum required IIP3 is 68dBm.

$$\mathrm{IIP3} = \frac{\mathrm{P_{in}} - \mathrm{IL} - \mathrm{P_n}}{2} + \mathrm{P_{in}} - \mathrm{IL} = \frac{20 - 4 + 88}{2} + 20 - 4 = 68\mathrm{dBm} \qquad (2.2)$$

The value in (2.2) highlights an important aspect. The balancing network must be highly linear and without a proper design choice it would become the system bottleneck, Fig 2.5.

The proposed balancing impedance architecture

The proposed balancing impedance is a resonant CLC network shown in Fig.2.6. One node is connected to the hybrid transformer, while the other to an external and highly linear 50Ω resistor as nominal value. Tuning both capacitors and inductor, the balancing impedance covers a large set of impedance values.

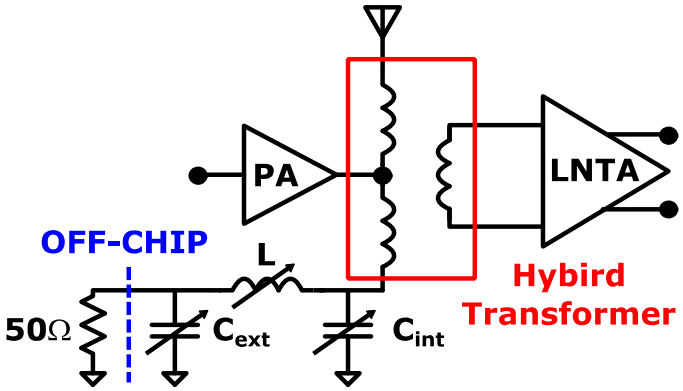
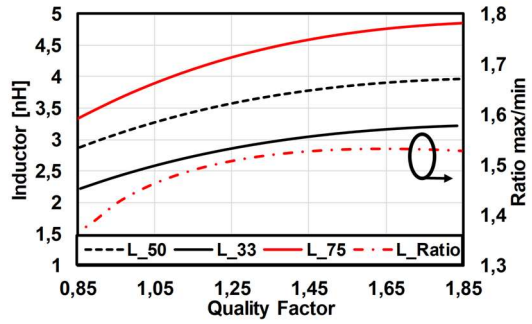
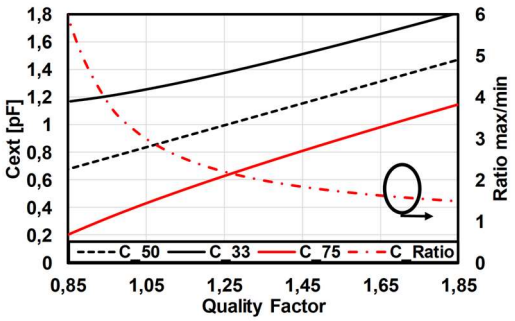
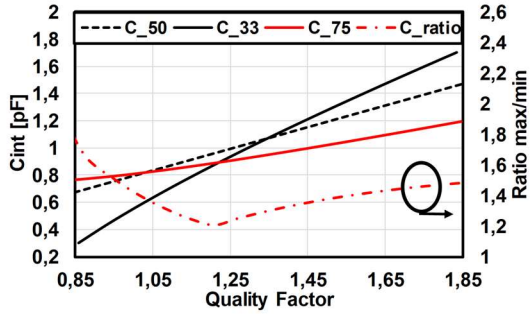


Fig. 2.6: The hybrid transformer connected to the proposed balancing impedance. The CLC network is connected to a fix highly linear off-chip 50Ω.







Parameter	Value
Cext	1,5pF/0,8pF=1,87
Cint	1,2pF/1pF=1,2
L	4,6nH/3nH=1,5
Q	1,4
Freq.	2GHz

Fig.2.7: The required CLC networks to realize three different impedances (30Ω, 50Ω, 70Ω) vs the required quality factor Q. The table summarizes the chosen values at 2GHz.

Moreover, the CLC network provides large redundancy which is mathematically proven in Appendix A. Its design depends by three main aspects:

1) The achievable ISO.
2) The VSWR to cover.
3) The quality factor (Q) and bandwidth (BW).

The TX-ISO depends by the impedance difference between the antenna and the balancing network and is defined as:

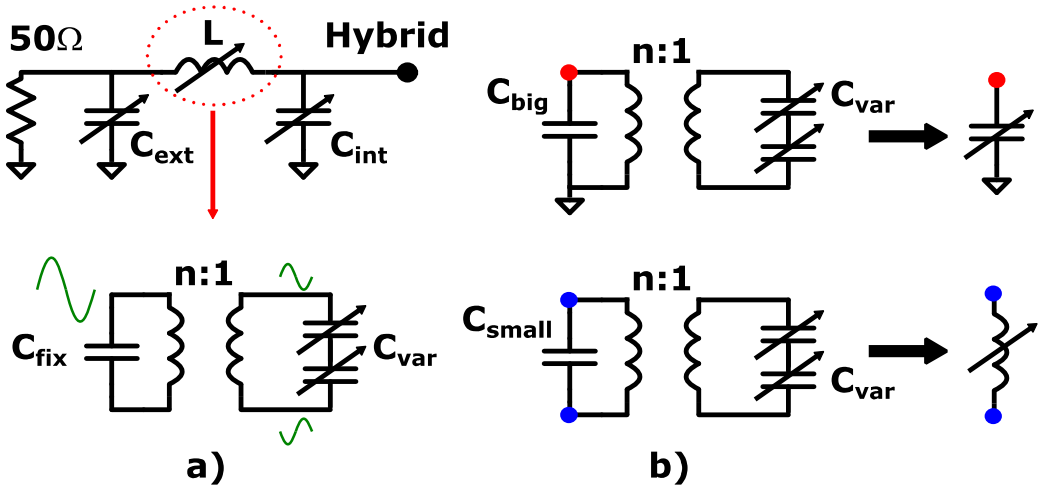


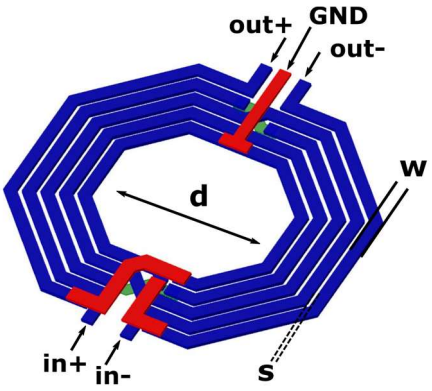
Fig. 2.8: a) The description of each tuneable component. b) The input fix capacitance determines the proper functionality.

$$\mathrm{ISO} = 20\log|\Gamma_{\mathrm{ant}}(\omega) - \Gamma_{\mathrm{bal}}(\omega)| - 20\log\left(\frac{1+\mathrm{r}}{\sqrt{\mathrm{r}}}\right) \qquad (2.3)$$

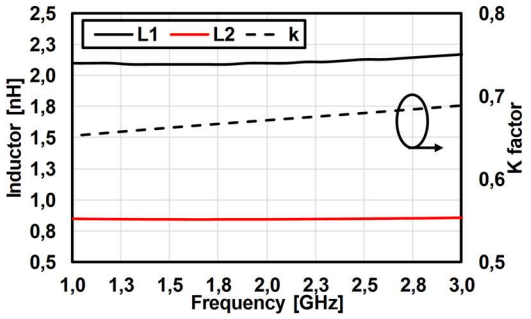
$\Gamma(\omega)$ and r are the reflective coefficient and the transformer symmetry, respectively. In a symmetric solution ($r = 1$), to realize 40dB of ISO less than 4% of impedance difference is required, therefore, any component of the CLC network requires at least 5 bit of resolution The Voltage Standing Wave Ratio (VSWR) is a useful metric to describe the impedance variation in frequency. In the Smith's chart, it is represented through a circle with constant radius center at 50Ω. In many applications, the required VSWR is 1,5:1 fixing the antenna real impedance deviation from 33Ω to 75Ω. The CLC's quality factor Q describes the balancing impedance deviation in frequency from its nominal value. In this work, the balancing impedance targets are to reach at least 40dB of integral ISO with a VSWR of 1,5:1 and low as possible quality factor Q.

The CLC components tuning range

The tuning range of each CLC component must be chosen carefully due to its redundancy, Fig. 2.7. The three plots show all the possible CLC configurations versus the required quality factor to realize three different impedances: 33, 50 and 75Ω at 2GHz. The plot of $\mathrm{C_{ext}}$ shows that for low Q values, its required ratio $\mathrm{C_{max}}/\mathrm{C_{min}}$ is extremally high making difficult to implement it in practise. Instead, the inductor and the capacitor $\mathrm{C_{int}}$ have larger ratio for high Q values. Therefore, it exists a middle value of Q which provides a practical tuning range. A Q of 1,4



Parameter	Value
d	104um
s	3um
w	8um



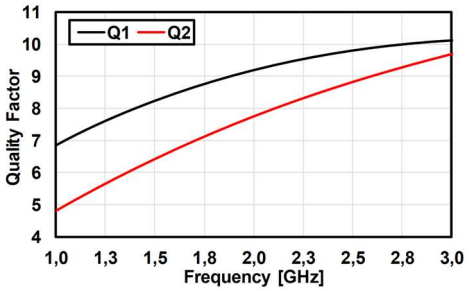


Fig. 2.9: The transformer employed in the CLC network. On the right, the inductors and quality factors values vs frequency.

provides an ON/OFF ratio less than two for all the three components, while the table in Fig. 2.7 shows the required components values.

The inductor is the larger component for the area occupation point of view. To employ a tuneable inductor and to reduce its area consumption, a tuneable capacitance C_{var} is added in parallel to a fix inductor L_{fix}. The equivalent inductance L_{eq} becomes capacitance dependent:

$$L_{eq} = \frac{L_{fix}}{1 - L_{fix} C_{var} \omega^2} = L_{fix} * K = L \qquad (2.4)$$

The tuning cell designs

A TX output power of 20dBm is equivalent to a peak-to-peak voltage of 6,32V. The available TSMC 28nm technology can sustain only 1 or 1,8V on its nodes. For this reason, a transformer 2:1 is employed to reduce the output voltage swing in the secondary coil relaxing reliability and linearity constraints, Fig.2,8. The same transformer is used for each component of the CLC network. The change of functionality between inductance and capacitance behaviour depends by a fixed capacitance in the primary coil. When, the resonance between the transformer's inductance load and the input fixed capacitor is larger than the

working frequency, the equivalent impedance is an inductor. On the contrary when the resonance frequency is below, it behaves like a capacitor. Concerning the CLC's inductor, the fix inductance is given by the transformer's load while the variable capacitance by the tuneable part in the secondary coil.

The transformer inductances for the primary and secondary coils are 2.1nH and 0.84nH, respectively. At 2GHz working frequency, their Qs are 9,1 and 7,75, respectively, with a coupling factor k of 0.67, Fig.2.9. The single capacitive tuning cell is shown in Fig.2.10. It has two NMOS transistors in series to a fixed capacitor $\mathrm{C_{on}}$. When the switching cell is ON, both the transistors enter in triode region and the equivalent impedance becomes $\mathrm{C_{on}}$=300fF. In OFF state, the two NMOSs are turned off and the equivalent impedance becomes a series combination among $\mathrm{C_{on}}$ and $\mathrm{C_x}$.

$$\mathrm{C_{on-state}} = \mathrm{C_{on}} \text{ and } \mathrm{C_{off-state}} = \frac{\mathrm{C_{on}C_x}}{2(\mathrm{C_{on}} + \frac{\mathrm{C_x}}{2})} \tag{2.5}$$

The presence of C_x in parallel to the NMOS transistors allows to realize reliable and highly linear devices. Their effect is more evident in OFF state. About the device reliability, $\mathrm{V_t}$ is a high impedance node with a voltage swing equal to the input signal. In this scenario, if a negative swing crosses the NMOS threshold voltage, the input signal would change the switches state making the equivalent capacitance time and input voltage dependent. Instead, the capacitors C_x provides an AC current path to ground that equally divides the voltage signal in the intermediate nodes. To further improve reliability, all the nodes are connected to fixed DC voltage references through resistors $\mathrm{R_1}$ and $\mathrm{R_2}$. About the distortion, it is generated differently in the two working states, ON and OFF. The former is developed by transistor's finite ON resistance $\mathrm{R_{on}}$, the latter by junction's capacitance in $\mathrm{V_t}$ and $\mathrm{V_b}$ nodes. The junction capacitance is expressed as:

$$\mathrm{C_j} = \frac{\mathrm{C_{j0}}}{\left(1 + \frac{\mathrm{v_R}}{\mathrm{V_j}}\right)^{\mathrm{m}}} \tag{2.6}$$

The parameter C_{j0} represents the junction capacitance at bias 0, while V_j and m the voltage threshold and grading coefficient, respectively. All these parameters are technology depend. The v_R is instead the junction reverse voltage and increasing its value the junction capacitance decreases developing less distortion. The resistor $\mathrm{R_1}$ and $\mathrm{R_2}$ with their reference voltages also accomplish

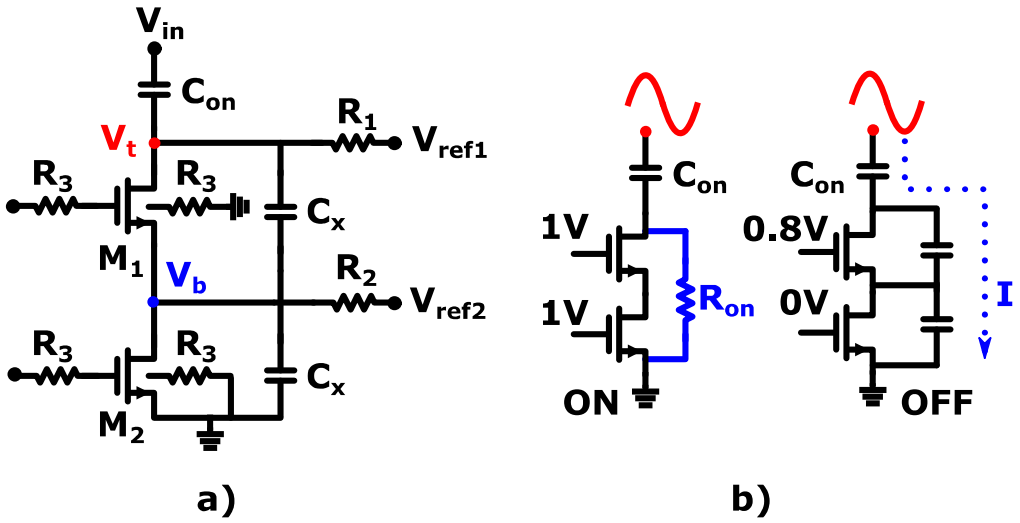


Fig. 2.10: a) The single tuning cell design. b) The two different operating regions.

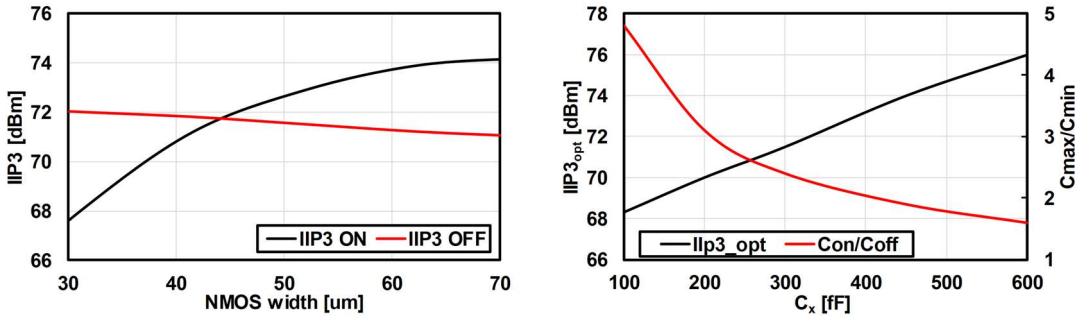


Fig. 2.11: The generated distortion for different NMOS sizing and fix C_{on}=300fF. On the right, the trade-off between $IIP3_{opt}$ and C_x.

this function. The V_{ref1} and V_{ref2} nominal values are 1.8V and 1V, respectively. The implemented transistors are also triple-well with floating bulk. In this way, the bulk nodes experience a voltage swing referred to the input signal to further improve OFF state linearity and reliability.

The transistor sizing is designed to develop equal distortion in both operating states, ON and OFF. In ON state, the input to V_t node transfer function has a high-pass shape. So, increasing the transistor width, the equivalent resistor R_{on} decreases performing more filtering and less distortion.

$$\frac{V_t}{V_{in}} = \frac{SC_{on}R_{on}}{1 + SC_{on}R_{on}} \tag{2.7}$$

On the contrary, larger transistor increases junction capacitance (2.6) and the relative distortion in OFF state. Therefore, there exists a “sweet” sizing for each

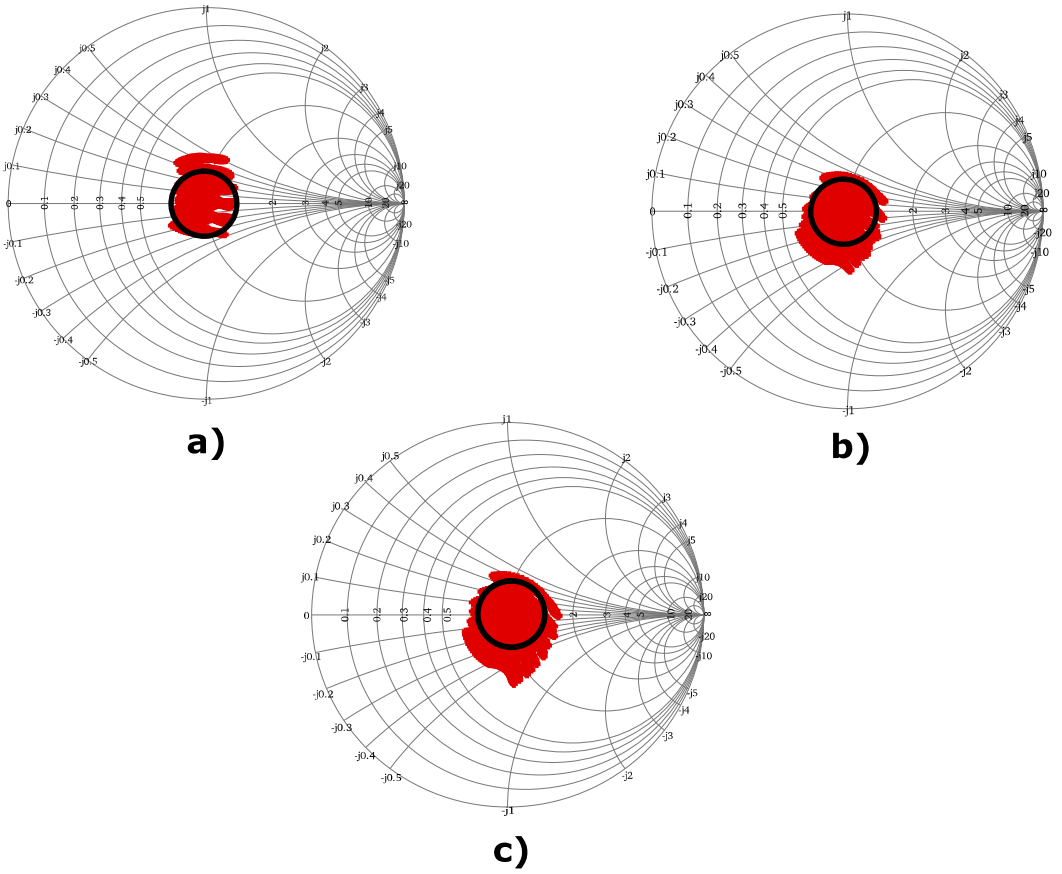


Fig.2.12: The covered impedances for different LO frequencies. The black circle represents a VSWR of 1.5:1. a), b) and c) are at 1.8, 2 and 2.2 GHz carrier frequency, respectively.

value of C_{on} that determines an equal IIP3 in both states, Fig. 2.11. The transistors size is set to 41,6um/30nm for both M_1 and M_2 providing more than 70dBm of IIP3.

The C_x value determines another trade-off between OFF-state distortion and achievable tuning range $C_{on-state}/C_{off-state}$. Considering, 20dBm of TX output power and the minimum required tuning range in Fig. 2.7, C_x = C_{on}= 300fF develops a tuning cell with enough ON/OFF tuning range (more than 2) and linearity.

In Fig. 2.12, the simulation results show all the covered impedances with the designed CLC network and in different working frequencies from 1,8 to 2,2 GHz. In Fig. 2.13, the achievable ISO with a constant 50Ω antenna impedance hybrid transformer, RX-RL and TX-IL parameters. In detail, the CLC configurations show more than 60dB of ISO in the peak value and an integral isolation of 40dB over

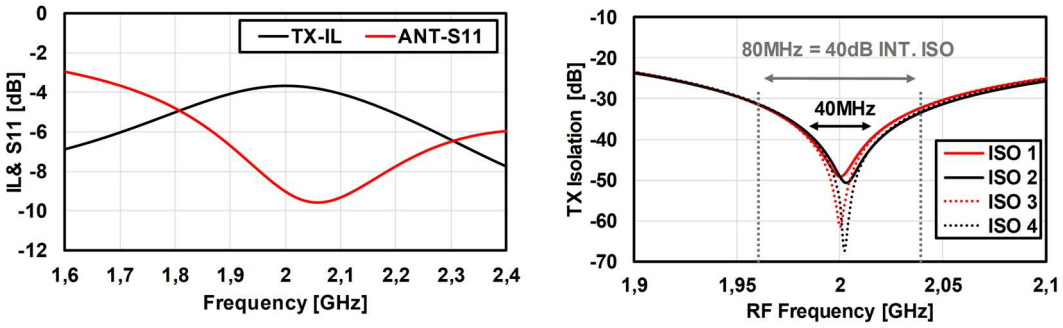


Fig. 2.13: On the left, the hybrid transformer S-parameters. On the right, the TX output referred achievable isolation with 4 different balancing impedance configurations.

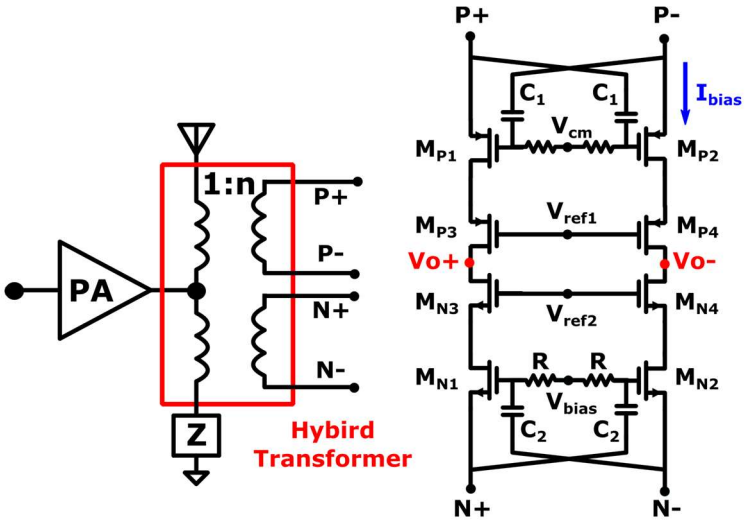
Table 2.I: Balancing impedance comparison table

	[20] TMTT '13	[21] TMTT '14	[22] TMTT '17	[24] ESSCI RC '14	[15] TMTT '19	[23] TMTT '16	THIS WORK
Technology	90nm CMOS	65nm CMOS	28nm CMOS	180nm SOI	SAW	180nm SOI	28nm CMOS
Band [GHz]	1,7-2,2	1,7-2,2	1,7-2,1	1,7-2,2	0,9	1,9-2,2	1,8-2,1
BW [MHz][(a)]	200	<20	20	160	23	300	32-40
ISO [dB]	>40	40	40	40	20	>40	40
Inductive impedances[(x)]	NO	YES	NO	YES	-	YES	YES
TX_{max} power [dBm]	27	27	N/A	27	>27	27	>24
IL [dB]	4.7	4,5	4	3	2.9	3,7	4
IIP3 [dBm][(k)]	N/A	55	40-50	<50	41	>65	**>70**
VSWR	1	2	N/A	N/A	N/A	1,5	1,5
Area [mm^2]	0.6	2,2	0,72	0,67	Off-chip	1,75	**0,7**

[(a)]The RF bandwidth with isolation >40dB. [(x)]The balancing covers inductive impedances. [(k)]Referred to balancing impedance.

80MHz of RF bandwidth. The IIP3, referred to PA output, is always larger than 73dBm proving that the solution adopted can realize highly linear devices.

The Table 2.I gives a comparison table with other solutions in literature. This network is the first one to provide an IIP3>70dBm with limited chip area consumption and large VSWR. The only work which provides a comparable IIP3 is [23] which employs a dual-frequency balancing condition. In this way, the isolation bandwidth is extremely higher but at cost of 2,5 times area consumption.



Para.	Value
$M_{P1,2}$	135um/30nm
$M_{P3,4}$	33,6um/30nm
$M_{N1,2}$	135um/30nm
$M_{N3,4}$	33,6um/30nm
C_1	1.2pF
C_2	490fF
V_{ref1}	0,7V
V_{ref2}	1,1V
V_{dd}	1,8V
I_{bias}	3mA

Fig. 2.14: The proposed LNTA connected to the hybrid transformer. The table summarizes the transistors sizing and power consumption.

2.2.2 Hybrid Transformer and LNTA

The Common-Gate (CG) based LNA is a good topology to provide low noise, high linearity and low power consumption. A push-pull topology halves the required current for a given transconductance gain and improves its compression point. A hybrid transformer with two secondary coils connected to a push-pull LNA has been already presented in [22], proving good linearity and noise performance. The proposed CG LNA is presented in Fig. 2.14 and foresees to implement the same architecture. The cross-coupled (XC) topology improves LNA noise/distortion performance and common-mode (CM) rejection by CM TX-leakage due to transformer parasitic capacitors. A coplanar structure highly reduces parasitic improving CM leakage isolation. Contrary on standard solutions [1], the LNA is not power matched enabling to improve both noise and linearity performance. The hybrid transformer provides a high output impedance to the input transistors, forcing their noise/distortion to recirculate improving LNA's NF and IIP3. In balancing condition where the antenna and the balancing impedances are the same, e.g. 50Ω = R_s, and a transformer turns ratio of n, the transformer output impedance is:

$$Z_{hy} = 2R_s n^2 \tag{2.8}$$

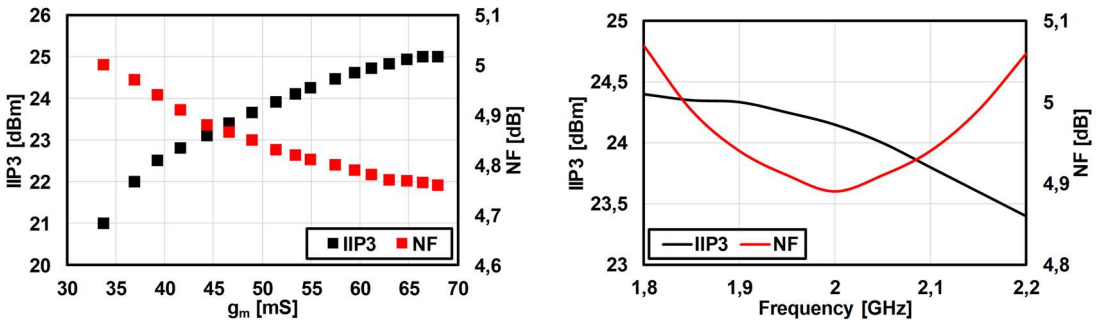


Fig. 2.15: On the left, the LNTA performance vs transconductance gain. On the right, the NF and IIP3 vs LO frequency.

A smaller LNA input impedance is realized with high transconductance gain forcing its noise/distortion to recirculate more effectively. Moreover, the push-pull structure with the feedforward capacitors allow to reach high transconductance gain with moderate power consumption. The transconductance gain from the antenna to the LNA output and the LNA noise factor are:

$$G_m = \frac{2ng_m}{1 + 2n^2 g_m R_s} \tag{2.9}$$

$$F = 2 + \frac{\gamma}{2n^2 g_m R_s} \tag{2.10}$$

In (2.9), for large g_m values, the denominator is approximated by $2n^2 g_m R_s$ simplifying $G_m \approx 1/nR_s$. The equation (2.10) shows that increasing g_m or hybrid transformer output impedance $2R_s n^2$, the noise factor is reduced up to a minimal theoretical value of 3dB. The LNA IIP3 is expressed as:

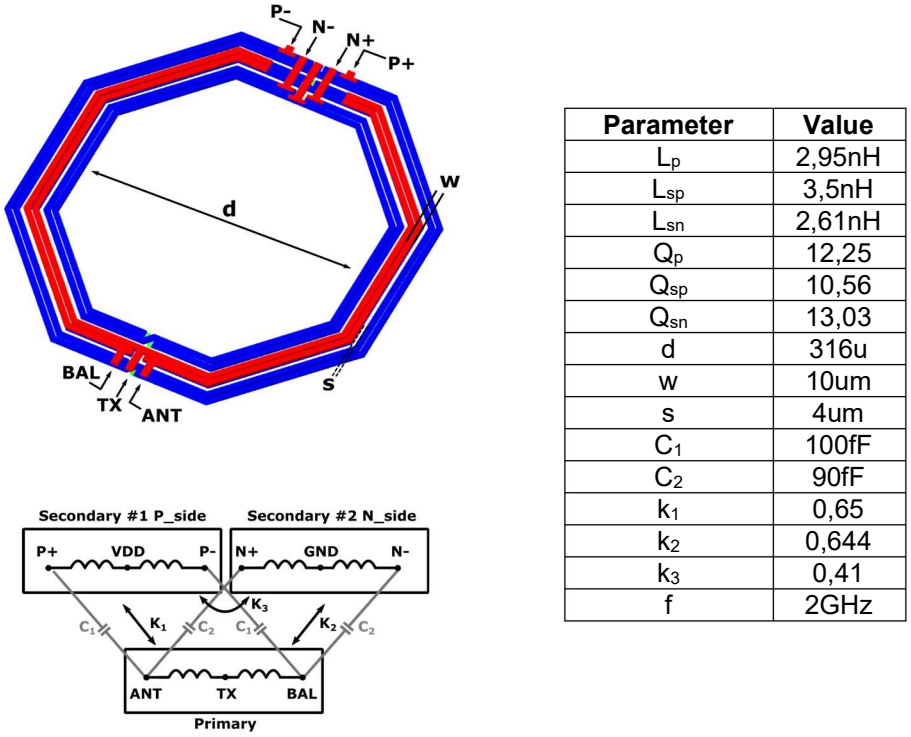
$$IIP3 = \sqrt{\frac{4g_m}{3g_{m3}n^2}}(1 + 2g_{m3}R_s n^2)^{\frac{3}{2}} \tag{2.11}$$

g_{m3} is the transconductance third-order nonlinear coefficient. As in (2.10), increasing g_m or $2R_s n^2$, the LNA IIP3 improves significantly thanks to the recirculation effect, Fig. 2.15. The transformer loss degrades LNA noise performance making the equation (2.10) not valid anymore. Lumping the losses with a single resistor R_p in parallel to the primary coil, the equation (2.10) is changed in:

$$F = 2 + \frac{4R_s}{R_p} + \frac{\gamma}{2n^2 g_m R_s}\left(\frac{2R_s + R_p}{R_p}\right)^2 \tag{2.12}$$

Table 2.II: The LNA noise breakdown at 2GHz

BAL+ANT	Hybrid Losses	LNA	TOT F=3,07
66%	19%	15%	100%



Parameter	Value
L_p	2,95nH
L_{sp}	3,5nH
L_{sn}	2,61nH
Q_p	12,25
Q_{sp}	10,56
Q_{sn}	13,03
d	316u
w	10um
s	4um
C_1	100fF
C_2	90fF
k_1	0,65
k_2	0,644
k_3	0,41
f	2GHz

Fig. 2.16: The hybrid transformer with its sizing parameters.

For infinite Q, the equation (2.12) is restored to (2.10). In Fig. 2.16 the designed transformer is shown, and it employs a coplanar structure to reduce parasitic capacitances. The primary inductor is 2,95nH, while the two secondaries for P and N sides are 3,5nH and 2,61nH, respectively. The parasitic capacitances between the primary coil and the two secondaries are 90fF and 110fF. At 2GHz working frequency, the coupling factors 1 and 2 are 0,65 and 0,644 respectively while the cross coupling is only 0,41. The LNA burns 3mA of current for each branch and it has a transconductance gain of 50mS.This design choice allows to provide competitive IB receiver performance as described in simulation results section. The LNTA noise breakdown at 2GHz is shown in Table 2.II. The LNA output is AC coupled to the mixers with two series capacitances of 2pF.

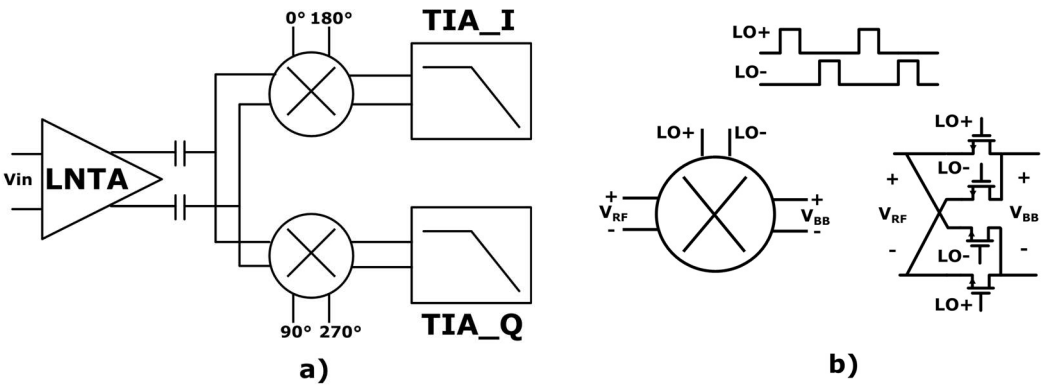


Fig. 2.17: a) The implemented main receiver architecture from hybrid to TIA output. b) The current driven passive mixer schematic.

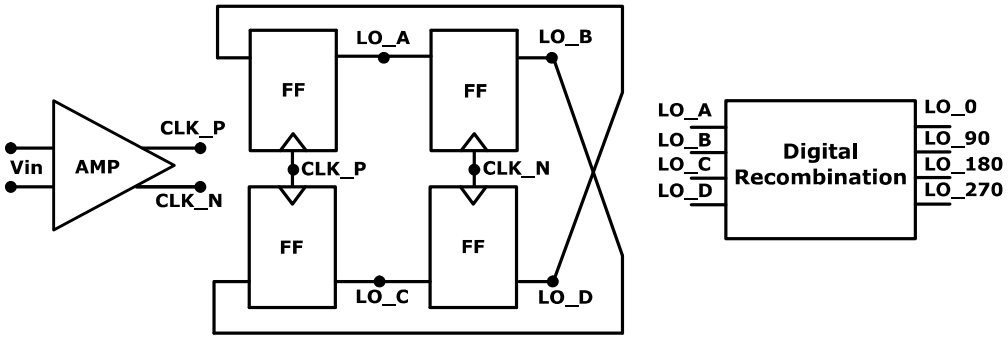


Fig. 2.18: The building blocks representation of the frequency synthesizer.

2.2.3 Mixers and Frequency Divider

The down-conversion process is realized through Current-Driven Passive Mixers with 25% Duty-Cycle [25-26]. In literature, they have proved superior linearity and noise performance than active topologies, Fig. 2.17. The switches are NMOS transistors sized with 40um/30nm which realize an ON impedance of 12Ω each one. Considering, an RF input current in the order of units of mAmp, the developed drain-source voltage drop is still small enough to not bring mixer circuit in compression. The switches gates are driven by a frequency divider of 2 with 1,2V of power supply which generates the I and Q phases. A 0,9V external voltage is applied to the gates to realize proper switching operation, while the transistors drain voltages are fixed by subsequent stage at 0,6V nominal voltage. The divider structure foresees an input pre-amplifier in series to a latch-based divider as in the picture, Fig.2.18. The amplifier forces the input differential signal with twice working frequency to be a rail-to-rail output signal that drives the latch-

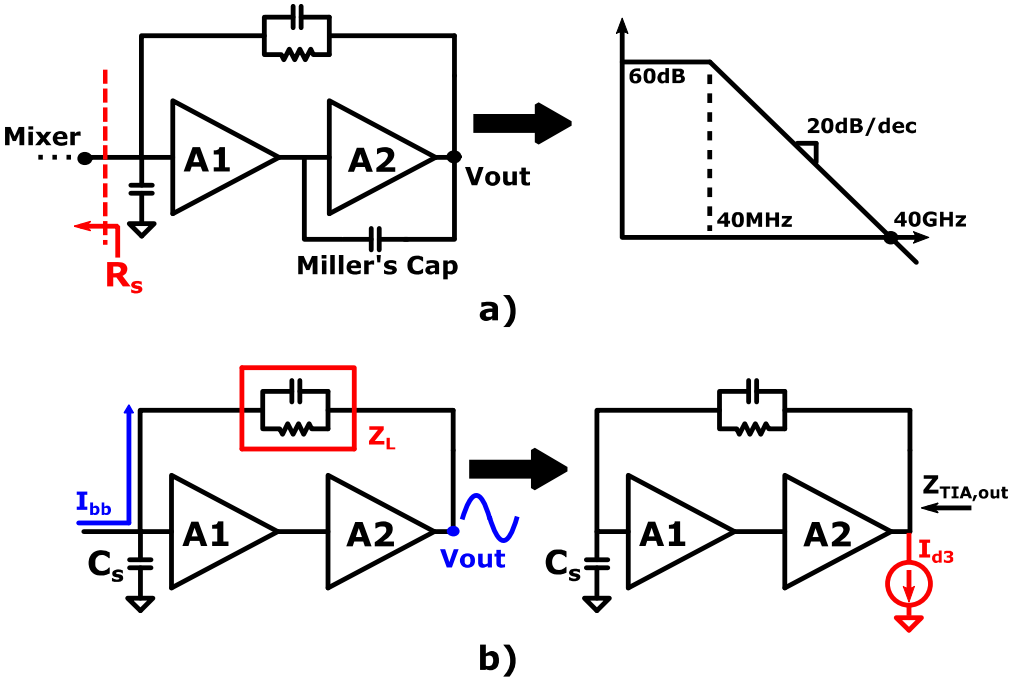


Fig.2.19: a) A Miller's compensated OTA with the required gain-bandwidth product. b) The IB TIA non-linear response representation.

based divider. The 4 phases are both connected to the main and to the auxiliary receivers. In this way, the same phase noise is shared by them developing a correlated reciprocal mixing. This practise allows to provide an extra digital cancellation of any residual reciprocal-mixing in post processing.

2.2.4 The TransImpedance Amplifier (TIA)

The IB Operational-Transconductance Amplifier (OTA) distortion is dominated by the last gain stage which sustains the entire output voltage swing. Its non-linear behaviour can be modelled as a current generator connected to the output node, Fig. 2.19 (I_{d3}). The TIA output impedance should be made as low as possible to reduce its non-linear contribution. The TIA output impedance is described as follow:

$$Z_{TIA,out} = \frac{Z_S + Z_L}{1 + G_{loop}} \tag{2.13}$$

The equation (2.13) shows two possible solutions to reduce it:

1. Reduce Z_S or Z_L

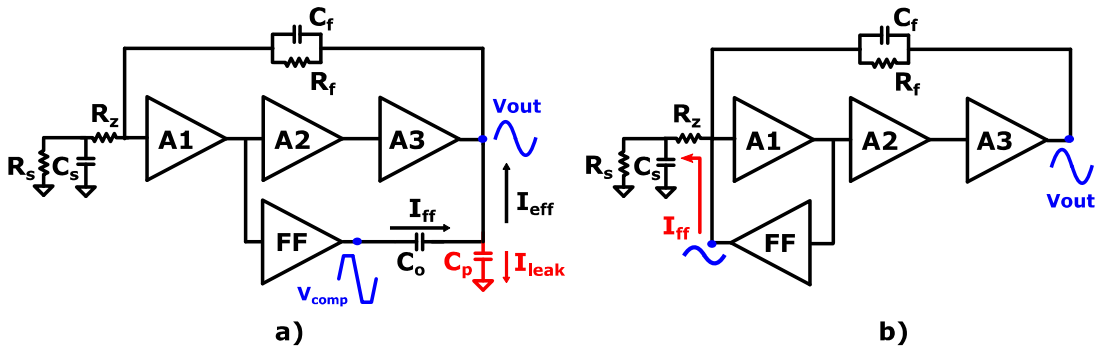


Fig.2.20: a) A standard three gain stages FF compensated OTA. b) The proposed modification with local feedback.

2. Increase the loop gain G_{loop}

The impedance Z_L is designed to develop a proper receiver gain and filtering, while Z_S is the TIA driving impedance that is derived by switching capacitor effect on the mixer input. The impedance Z_S can be modelled through a fixed resistor of 500Ω. Therefore, the two impedances are difficult to tune or are fixed by design. On the contrary, the TIA loop gain can be increased easily with OTA's number of stages reaching high open loop gain >60dB. To provide a constant In-Band linearity, the loop gain must have its dominant pole at least equal to the filter pole, in this case 40MHz. An OTA based on Miller's compensation technique would require a unity gain frequency of 40GHz, leading to unacceptably high-power consumption, Fig.2.19. A solution with two coincident poles at 40MHz would reach 0dB gain at 2GHz. For stabilization purpose, some zeros are introduced in the loop getting more than 60deg of phase margin at the cut-off frequency [27-28]. The Feed-Forward (FF) based compensation solutions have been exploring in the past to ensure TIA stability at high frequency [29]. This technique has proved its effectiveness but with some important drawbacks. In theory, the FF stage bypasses the intermediate stages, with their own poles, becoming the dominant loop at high frequency. In practice, it requires high transconductance gain to be effective and a stacked topology it saves on power dissipation. These requirements reduce the FF stage voltage headroom, and it forces the TIA to have limited linearity. When using stacked transconductors, large ac coupling capacitors are required and their parasitic added to the subsequent stage load reduce the loop effectiveness. A different approach is shown in Fig.2.20 and it overcomes many of the previous limitations employing local feedback in the OTA's virtual ground. The OTA has two gain paths: one, at

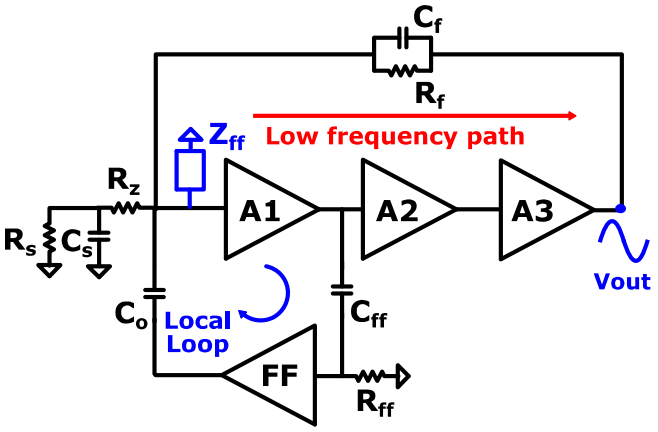


Fig. 2.21: The OTA details with focus on the two main loops and the loading effect by local feedback on the driving impedance.

low frequency, has three gain stages A_1, A_2 and A_3 and ensures high IB gain. The second one to introduce a zero at high frequency into the loop gain for stability purpose. In this topology, the FF stage is connected to the virtual ground where minimum voltage swing is present and the large capacitor C_S reduces parasitic impacts, requiring less current consumption. The calculations in Appendix B prove its superiority versus a standard FF compensation, Fig. 2.21. A large capacitor (C_S) is generally connected to the OTA's virtual ground to ensure out-of-band filtering. The capacitor C_S is fixed to 7pF developing with the driving impedance R_s=500Ω a first low frequency pole at 40MHz. In Fig. 2.22, the details of all the stages are shown. The first stage employs a differential PN topology that realizes high transconductance gain g_{m1} = 12mS and low input referred noise with half current consumption I_1 = 600uA. The second stage is a differential pair P-side with zero-pole doublet effect at 2GHz developed with capacitor C_H = 20fF and resistor R_H = 4kΩ. At low frequency, the transconductance gain is fixed by $M_{p4,5}$ while at high frequency C_z is a short circuit with $M_{n4,5}$, improving the overall gain of 6dB. The second stage draws 100uA and develops a low frequency pole at 240MHz. The effect of this pole is cancelled out with a zero introduced in the first stage through C_{ff} = 450fF and R_{ff} = 1,5kΩ. The capacitor C_{ff} determines a low frequency pole in the first stage coincident with $R_S C_S$.The third gain stage is a standard class AB with a transconductance gain of 8.2mS and it draws 400uA. Its pole is cancelled out with the zero introduced by the load in the feedback. Considering, the zero-pole cancellation summary, only two low frequency poles remain in the loop gain: the first stage ($R_1 C_{ff}$) and the driving impedance ($R_S C_S$),

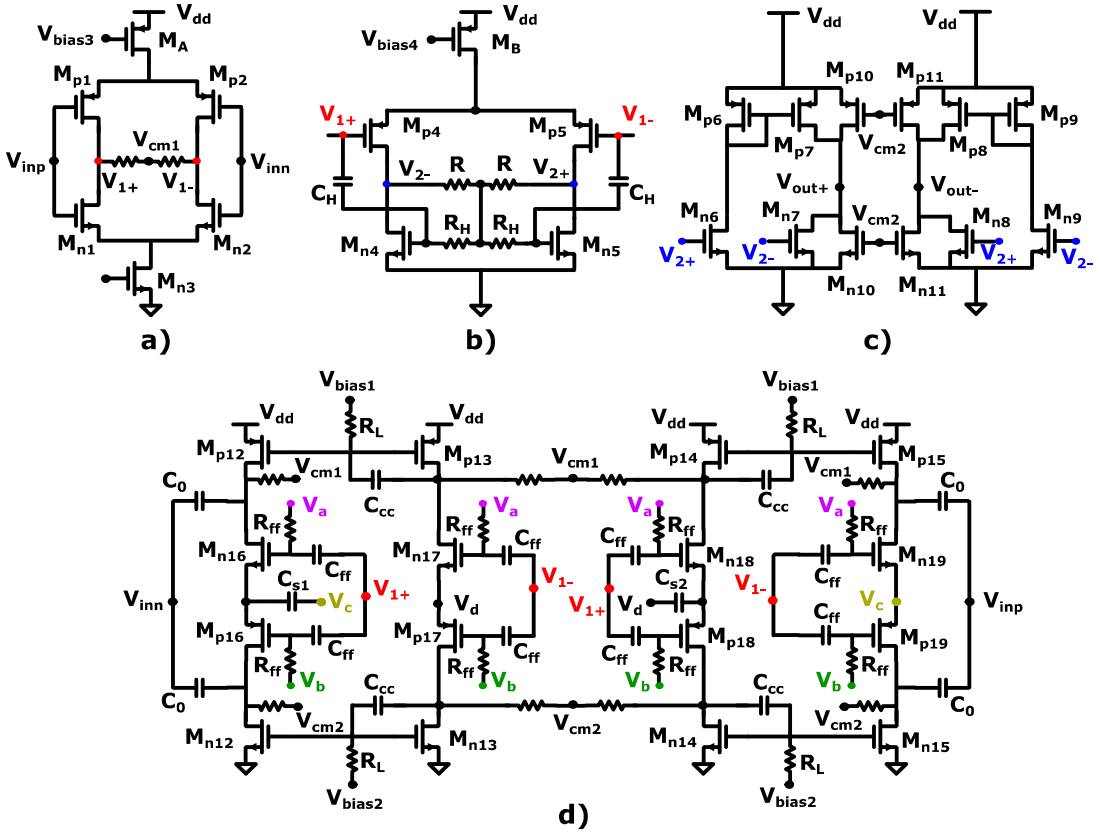


Fig. 2.22: a), b) and c) The first, second and third gain stages, respectively. d) The FF gain stage with a stacked topology.

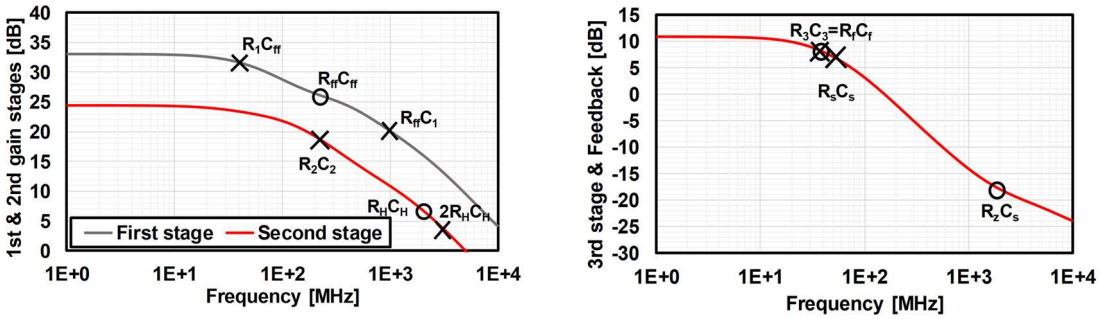
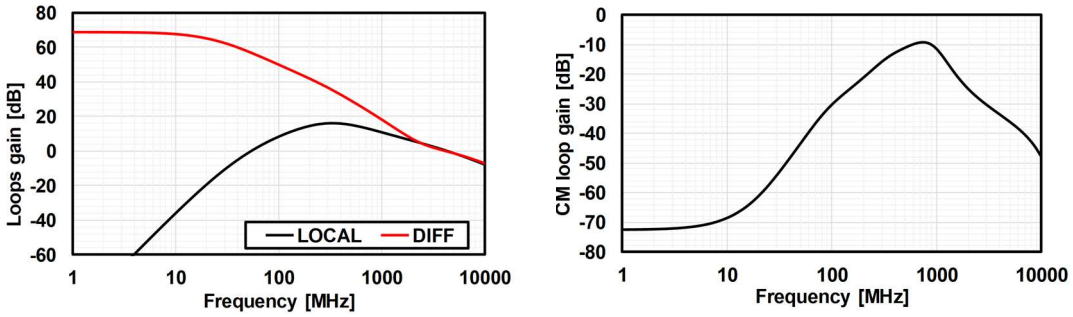


Fig.2.23: The zero-pole cancellation summary. On the left, the first and second gain stages. On the right, the third gain stage and feedback loop.

both at 40MHz. A resistor R_z = 15Ω in series with capacitor C_S develops a high frequency zero at 1,5GHz to further improve phase margin near cut-off frequency. The FF stage is a differential PN structure with current reuse approach to boost its transconductance gain. The $G_{m,ff}$ is equal to 35.2mS with 1.5mA current consumption. The structure provides excellent common mode rejection for ensuring OTA stability condition. Indeed, the OTA low frequency path has three inverting gain stages which ensure stability in both common and differential



	TT			SS			FF			SF			FS		
Temp. [°C]	-25	25	100	-25	25	100	-25	25	100	-25	25	100	-25	25	100
GBW [GHz]	5,5	5,1	4,6	5,7	5,4	5	4,3	3,9	3,5	5,4	5	4,3	5,6	5,3	4,7
PM [deg]	54,8	60	65,2	40	45,8	53	69,3	70,7	73	54,8	60	65	55	60	65,7
Gain [dB]	66,9	66	63,3	66,5	65	62,9	67,6	66	63,8	67	65,6	63,5	66,6	65,2	63

Fig.2.24: The differential and common mode loop gains. The local feedback becomes the dominant loop at 2GHz. In the Table, the PVT corners results are shown proving TIA stability.

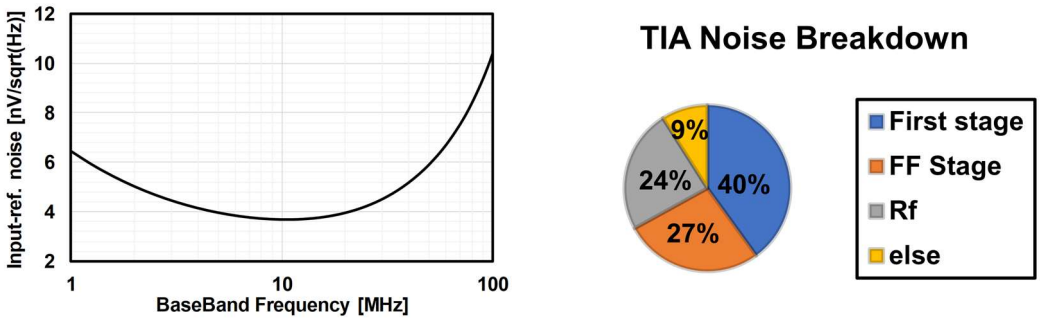


Fig.2.25: The main receiver TIA noise performance when is driven by 500Ω fix impedance.

modes, while at high frequency has only two stages. Crossing the output wires, it is possible to provide negative feedback to the differential mode while the common mode remains positive. Therefore, a strong common mode rejection is required for the FF stage to ensure low common mode gain at high frequency. The local feedback loads the input driving impedance reducing its value and degrading TIA's noise and distortion, Fig 2.21 in blue. Therefore, it is fundamental to disable the local feedback in the receiver band. A first high pass filtering is realized with the capacitor C_{ff} and the resistor R_{ff} which develop a pole at 240MHz in the local feedback. The input PN structure is capacitively degenerated with $C_{s1,2}$ providing another order of filtering with a zero in the origin. The last filtering is provided at the output nodes with capacitors C_o. To further extend low frequency filtering, a capacitor C_{cc} is introduced in the FF stage disconnecting

Table.2.III: The TIA Sizing

Parameter	Value
$M_{p1,2}$	48um/150nm
$M_{n1,2}$	60um/150nm
M_{n3}	64um/100nm
M_A	64um/100nm
$M_{p4,5}$	12um/150nm
$M_{n4,5}$	8um/100nm
M_B	10um/150nm
$M_{p6,9}$	4um/100nm
$M_{n6,9}$	8um/100nm
$M_{p7,8}$	24um/100nm
$M_{n7,8}$	56um/100nm
$M_{n10,11}$	2um/100nm
$M_{p10,11}$	8um/100nm
$M_{n13,14}$ & $M_{p13,14}$	4um/30nm
$M_{n12,15}$ & $M_{p12,15}$	20um/30nm
$M_{n17,18}$ & $M_{p17,18}$	4um/30nm
$M_{n16,19}$ & $M_{p16,19}$	20um/30nm
C_0	700fF
C_{cc}	300fF
C_{s1}	2pF
C_{s2}	400fF
C_{ff}	112fF
R_{ff}	12kΩ

half circuit providing extra 6dB of current attenuation. The voltage supply of the entire TIA is 1,2V and its power consumption is 4mW. In Fig.2.23, all the zeros and poles for each stage are shown proving TIA stability. The simulation results prove a DC loop gain of 66dB with two dominant poles at 40MHz as expected. The phase margin is larger than 60deg around the cut-off frequency of 5.1GHz and robustness in all the PVT corners is proved. Compared to similar topology [30], this TIA is unconditionally Stable. The common-mode loop gain is always below 0dB proving its stability, Fig. 2.24. The differential-mode local feedback is the dominant loop gain at high frequency, and it shows a 3rd order high pass filtering as expected. The resistor R_f and the capacitor C_f in feedback are equal to 2,9kΩ and 1,4pF, respectively. Noise simulations with noiseless driving impedance of 500Ω proves an input-referred noise almost flat in the entire band <4nVswrt, Fig. 2.25. Table 2.III shows the TIA sizing.

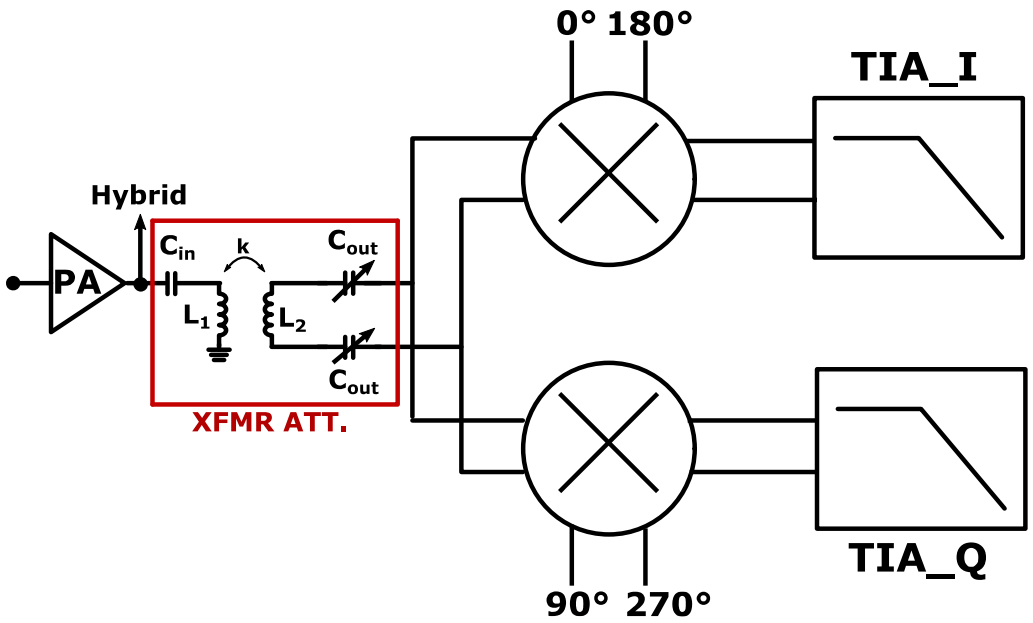


Fig.2.26: The mixer first auxiliary receiver building blocks representation.

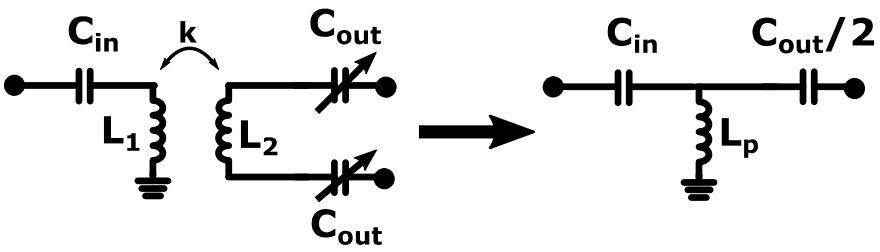
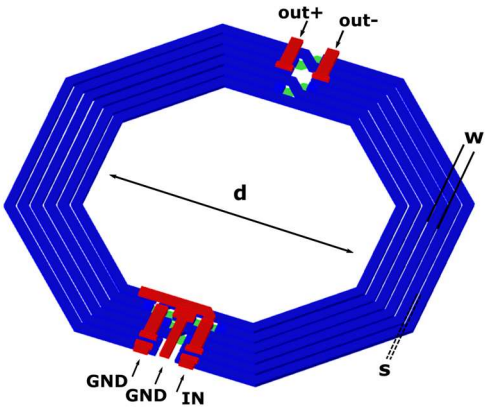


Fig.2.27: The simplified description of the input attenuator.

2.2.5 Auxiliary Receiver (AUX-RX)

The auxiliary receiver is added in the whole system to extract the TX-EVM which would strongly degrade the main receiver noise floor. This extra receiving path requires high SNDR to allow proper digital cancellation. Indeed, any spurious content in the auxiliary path is added in power to the main one. Moreover, the AUX-RX must provide high linearity performance when large input power signal is applied to its input. In the past, mixer-first receivers have proved high linearity performance [31-36]. Unfortunately, in literature, the optimum SNDR is still far away to sustain input power signals larger than 10dBm. The common trend is to design power-matched receivers with low noise performance but limited power handling capability. On the contrary, a not power-matched mixer-first topology overcomes this limitation allowing to get higher SNDR with the maximum input signal. The employed auxiliary receiver is shown in Fig. 2.26. A passive tuneable transformer-based attenuator interconnects the PA output node to the auxiliary



Parameter	Value
d	237um
s	2um
w	8um

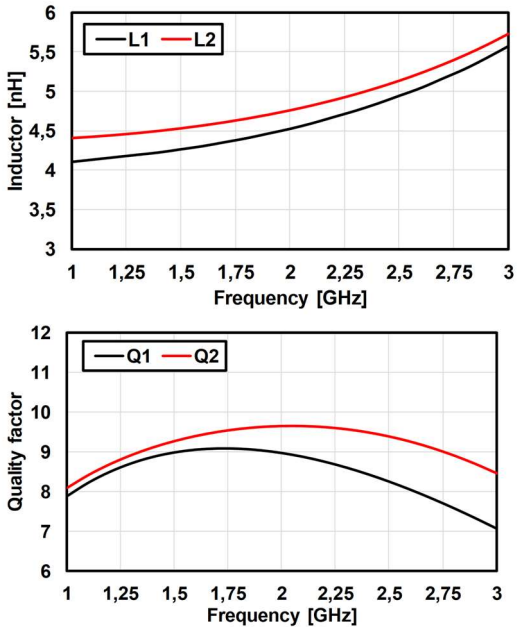


Fig.2.28: The transformer employed in the attenuator.

receiver input. The attenuator is necessary to develop a first rough wideband TX suppression and to relax linearity constraints in the subsequent stages. Moreover, it provides high input and output impedances, Fig. 2.27. The former to not load PA output node which would degrade TX-IL, the latter to develop high driving impedance to the TIA. The attenuator is a single-ended input to differential output transformer with series input and output capacitances C_{in} and C_{out} that dominate the input and output impedances Z_{in} and Z_{out}, respectively. At high frequencies, both Z_{in} and Z_{out} become a series combination between the two capacitors. This effect develops a larger impedance at high frequency reducing harmonic mixing. The transformer inductive load together with the capacitors C_{in} and C_{out}, develop a zero-pole doublet resonances as shown in equation (2.14-2.15).

$$Z_{IN} = \frac{S^2 L_p (C_{in} + \frac{C_{out}}{2}) + 1}{S C_{in} (S^2 \frac{L_p C_{out}}{2} + 1)} \tag{2.14}$$

$$Z_{OUT} = \frac{S^2 L_p (C_{in} + \frac{C_{out}}{2}) + 1}{\frac{S C_{out}}{2} (S^2 L_p C_{in} + 1)} \tag{2.15}$$

For the sake of simplicity, the transformer load is only an inductor in parallel to the input scaled by transformer coupling factor squared. The PA and the BB

impedances are neglected being smaller contributions. Analysing the equations (2.14) and (2.15), it can be proved that a proper design choice can fix both zero-pole doublets between the working frequency and the first spurious tone at $3f_{lo}$. This design choice allows to have high input and output impedances in the working frequency and benefits of a smaller capacitance in the first spurious tone. The transformer design develops another system trade-off. A small transformer requires large capacitors to develop equal attenuation. This condition would load both PA and TIA nodes developing more TX-IL and degrading receiver noise/linearity. On the contrary, a large transformer requires less series capacitor, but it consumes larger chip area, and it develops larger parasitic capacitors with the substrate. Therefore, the transformer size is chosen as a compromise which provides the required attenuation with the best receiver performance. The RF attenuation increases proportionally the auxiliary receiver noise floor and considering 40dB of hybrid transformer TX-ISO, at least 30dB of attenuation is required. The employed transformer is shown in Fig.2.28 with a turn ratio 1:1. The inductors of the primary and secondary coils are equal to 4.5nH and 4.7nH, respectively. The quality factors are 9 and 9.7 while the coupling factor k is 0.7 at 2GHz. The input capacitor C_{in} is 175fF while C_{out} tunes from 300fF to 600fF. The tuning capacitor in the secondary coil allows to realize constant attenuation for different carrier frequencies.

Single tuning cell

The single tuning cell, as in the balancing network, is designed to sustain large input power. The transformer attenuation relaxes the output voltage swing in the secondary coil, but it is still enough to change switch state. A similar structure used in the balancing network is reused in the attenuator, Fig.2.29. In this case, only one transistor is employed being smaller the voltage to sustain. The cell is connected through two equal capacitances C_p. When the cell is in ON-state, the equivalent capacitance is $C_p/2$, otherwise, is a series combination with parasitic capacitances C_{gd} and C_{gs}. Two reference voltages are again connected through

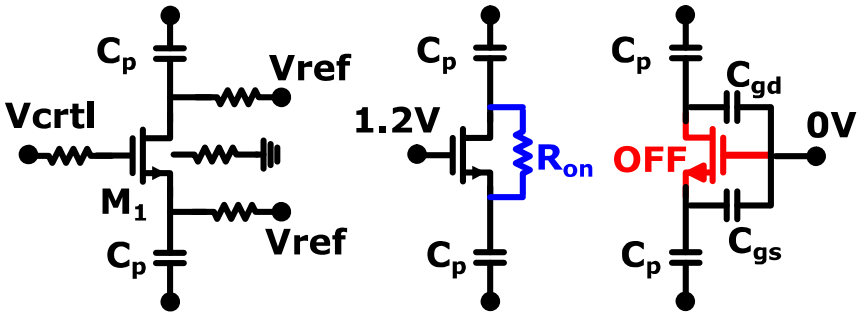


Fig.2.29: The single tuning cell description. On the right side, the ON/OFF configurations.

two resistors to M_1 drain and source. Their nominal voltages are 0.3V to provide voltage headroom in OFF-state. In ON-state, the gate is connected to 1.2V providing a V_{gs} of 0.9V. The NMOS bulk node is again floating to further enhance OFF-state linearity and reliability. The NMOS sizing ensures 60dBm of IIP3 in both the operating states. The NMOS sizing is 7.2um/60nm.

The same 1st order TIA as in the main receiver is employed also in the auxiliary receiver with equal -3dB frequency. In this case, the feedback resistor is halved to reduce its noise contribution in the receiver chain.

2.2.6 DAC

The current-mode DAC is connected to the TIA virtual ground and is necessary to further suppress TX- leakage coming by mixer. Its goal is to generate an output current with equal magnitude and opposite phase referred to the TX-leakage. Referring all the signals to the input antenna, the 20dBm TX output power has been suppressed of 40dB by the hybrid transformer. This determines a residual power difference between the TX and the receiver noise floor (e.g. noise floor= -88dBm) of roughly 70dB. The equation (1.23) requires an ENOB of 11,5bit for a Nyquist's DAC to develop 70dB of SNQR. To design a receiver robust to reciprocal mixing, the DAC shares the same mixer clock which is nominally at 2 GHz. Therefore, the OverSampling Ratio (OSR) improves the ENOB of roughly 2 bit with an OSR=25. However, design a 10bit DAC is quite challenge due to the mismatch limits. In order to relax the required physical number of bit, a digital second order sigma delta modulator is added in the DAC. Now, the equation (1.23) becomes:

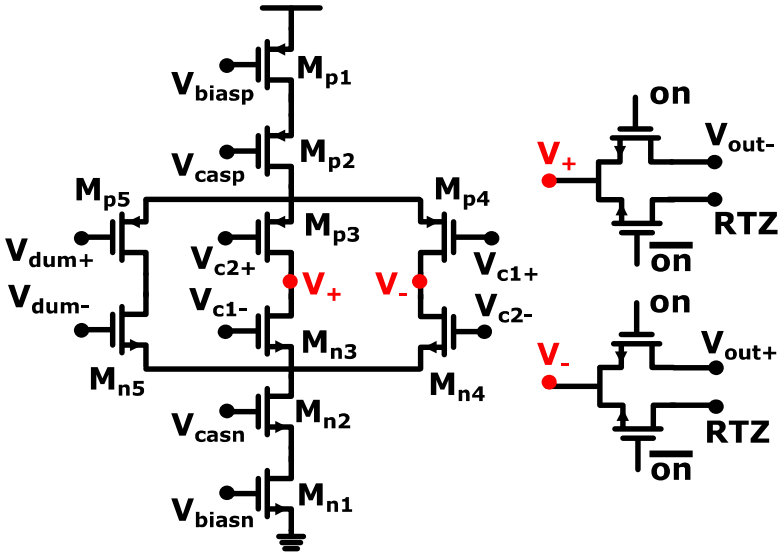


Fig.2.30: The single cell employed in the current mode DAC.

$$\mathrm{SQNR} = 6.02 * \mathrm{bit} - 12.9 + 15.05 \log_2 \mathrm{OSR} \qquad (2.16)$$

With only seven bit is possible to reach more than 100dB of SNQR. The DAC is segmented with two bit binary weighted and five thermometric. Unfortunately, the main DAC limitation is still the mismatch which develops significant distortion in the converting phase. A Data Weighted Averaging (DWA) solution is implemented in digital domain to relax mismatch constraints. The main difference with Dynamic Element Matching (DEM) approach is that a digital counter ensures to equally use all the thermometric cells. In this way, the static mismatch errors are significantly reduced in the output spectrum. A Matlab simulation ensures 12.8bit of ENOB with a SQNR of 80dB which is enough to not add any significant noise and distortion in the receiving path.

The single cell is shown in Fig. 2.30. It is a PN structure which delivers a differential current to the output nodes. The cell has two different operating points: SET and RTZ (Return-to-Zero). In the SET phase, the current is delivered to the outputs and the direction is stabilized by transistors $M_{p3,4}$ and $M_{n3,4}$. Moreover, a dummy branch is added when a cell must not deliver any current to the TIA. In the RTZ phase, the DAC is connected to a different virtual ground and no current is delivered to the TIA. The RTZ phase is fundamental to get proper cancellation. The reason is due to the mixer driving clock which is intrinsically RTZ referred to a single branch I or Q. Therefore, in order to have the same phase noise and to provide instantaneous cancellation, the DAC needs a RTZ phase. Moreover, this

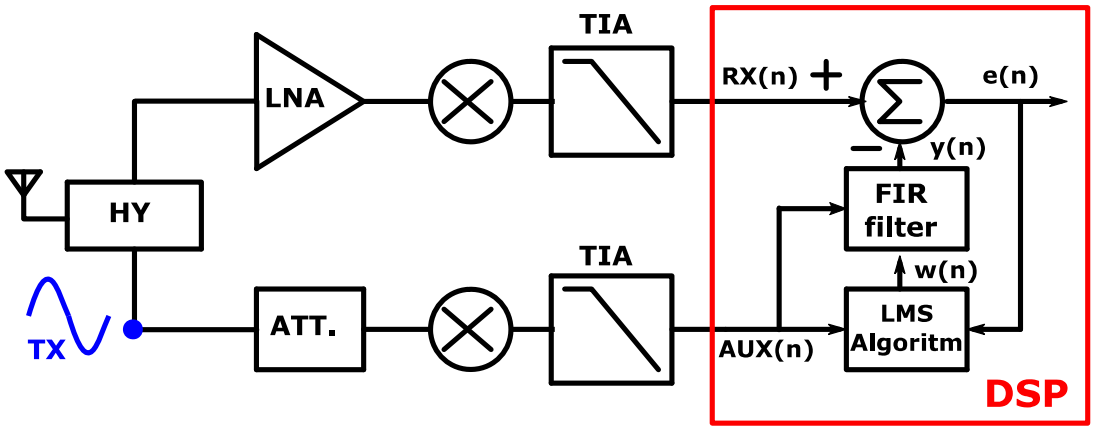


Fig.2.31: A simplified building blocks representation of the digital algorithm.

phase allows to change DAC configuration when is not connected to the TIA input. The DACs must deliver a nominal current of 1mA and 2mA for the main and the auxiliary receivers, respectively.

2.2.7 LMS-FIR equalizer

A simplified sketch to understand the LMS algorithm is shown in Fig.2.31 The TX is modelled as a voltage signal at the auxiliary receiver input. The TX leakage is down-converted to low frequency by both receivers and converted as a digital information through integrated ADCs. The two paths suffer of different time delays and transfer functions which make impossible to apply a simple digital combination in post processing. To track these variations over time, an adaptive digital filter is required. An adaptive Least-Mean-Square (LMS) Finite Impulse Response (FIR) filter provides a low-cost digital path, and it is suitable for RF applications. The algorithm provides a recursive method in the Wiener's filter theory. This solution gives a good compromised in terms of steady state error, number of computations, robustness, and rate of convergence. Below, the signals are assumed to be with zero-mean and wide-sense stationary.

The filtering process and the adaptative coefficients characterized an adaptive equalizer based on an LMS algorithm. The equations that describe an equalizer are:

$$y(n) = \mathbf{W}^{H}(n)\mathbf{AUX}(n) \qquad (2.17)$$

$$\mathbf{W}(\mathrm{n}+1) = \mathbf{W}(\mathrm{n}) + \mu \mathrm{e}^{*}(\mathrm{n})\mathbf{AUX}(\mathrm{n}) \tag{2.18}$$

$\mathbf{W}(\mathrm{n})$ are the filter coefficients vector, μ the step-size, e the error and ^{H} the Hermitian transposition. The error is also defined as:

$$\mathrm{e}(\mathrm{n}) = \mathrm{RX}(\mathrm{n}) - \mathrm{y}(\mathrm{n}) = \mathrm{RX}(\mathrm{n}) - \mathbf{W}^{\mathrm{H}}(\mathrm{n})\mathbf{AUX}(\mathrm{n}) \tag{2.19}$$

In this case, $\mathrm{RX}(\mathrm{n})$ is the signal coming from the main receiver while $\mathrm{AUX}(\mathrm{n})$ from the auxiliary one. $\mathrm{y}(\mathrm{n})$ is the FIR filter output signal. The remaining error $\mathrm{e}(\mathrm{n})$ is the instantaneous error after the combination between the main receiver and the auxiliary output signals after the equalization. In previous work [53] has been proven that when the step size μ is properly chosen, the Wiener filter provides the best solution which an LMS-based algorithm converges. Considering, the minimum Mean-Square Error (MSE) definition:

$$\begin{aligned} \delta_{\min} = \mathrm{E}[\mathrm{e}(\mathrm{n})\mathrm{e}(\mathrm{n})^{*}] &= \mathrm{E}[|\mathrm{RX}(\mathrm{n})|^{2}] - \mathrm{E}[|\mathrm{y}(\mathrm{n})|^{2}] = \sigma_{\mathrm{RX}}^{2} + \mathbf{P}^{\mathrm{H}}\mathbf{W}_{0} \\ &= \sigma_{\mathrm{RX}}^{2} - \mathbf{P}^{\mathrm{H}}\mathbf{R}^{-1}\mathbf{P} \end{aligned} \tag{2.20}$$

where E is the expected value, σ_{RX}^{2} the variance of $\mathrm{RX}(\mathrm{n})$, $\mathbf{P}$ the cross-correlation vector of the two receivers' output, $\mathbf{R}$ the autocorrelation matrix $\mathrm{AUX}(\mathrm{n})$ and $\mathbf{W}_{0}$ are the optimum filter coefficients. Now, it is possible to derive the normalized Digital Cancellation (DC) through a power ratio between the main receiver output and the minimum error $\delta_{\min}$.

$$\mathbf{DC} = (1 - \mathrm{P}_{n}^{\mathrm{H}} R_{n}^{-1} P_{n}) \tag{2.21}$$

The subscript n indicates that the vectors are normalized by input power σ_{RX}^{2}. The final equation in (2.21) shows that the steady state error is strictly dependent on statistical parameters. A larger signals correlation provides better digital cancellation. In this case, the correlation is quite large being the large signal in the same working band. Similar considerations can be extended to analyse the filtered-X LMS filters. The goal of this sub-section is to provide a rough description of the digital algorithms employed in the system. For a deeper analysis, the bibliography provides many references to previous works that have employed similar solutions [37-42].

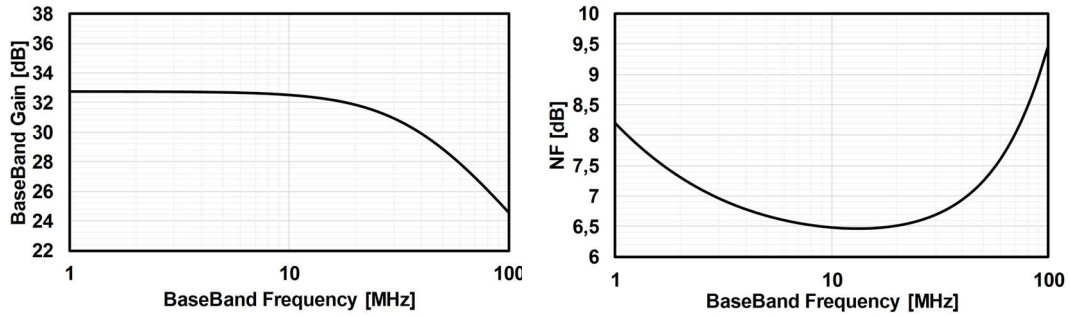


Fig. 2.32: The main receiver baseband gain and NF.

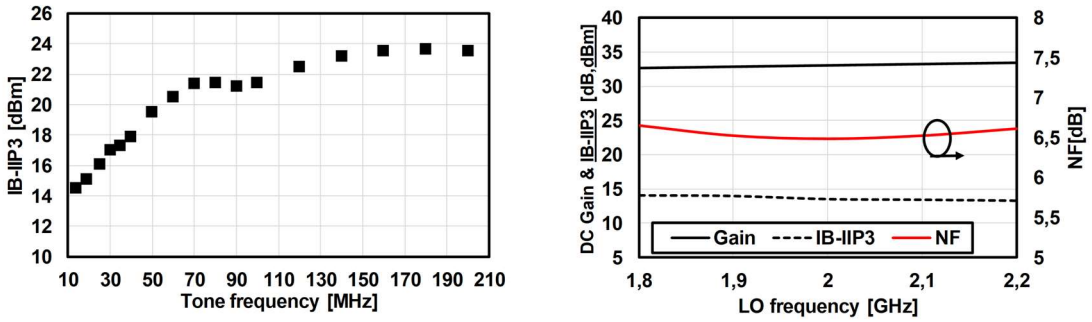


Fig. 2.33: The IIP3 vs blocker frequency and the main receiver performance vs carrier frequency.

2.2.8 Simulation results

The simulator used is Spectre, while the transformers are designed employing EMX and ADS supports. The technology used is TSMC 28nm in both receivers.

Main receiver:

The receiver transfer function from the antenna node to the TIA output has 33dB of gain with -3dB corner frequency at 40MHz. The NF is 6,4dB where 83% of the noise is developed by RF stages as describe in Table 2.IV, Fig. 2.32. The distortion is simulated with two tones test from in-band to out-of-band blockers. In band, the IIP3 is dominated by TIA distortion and is equivalent to 14dBm while, at high frequency, it improves up to 24dBm thanks to out-of-band filtering. The maximum reachable OOB-IIP3 is limited by LNTA linearity which can provide only 24dBm of IIP3, as shown in Fig. 2.15. The previous results are simulated with an RF working frequency of 2GHz. Changing the carrier frequency from 1.8GHz to 2.2GHz, the overall performance deviation is less than 1dB in the entire band,

Table 2.IV: The main receiver noise breakdown at 2GHz

BAL+ANT	LNA	HYBRID	TIA	TOTAL NF 6.4dB
48%	17%	17.8%	17.2%	100%

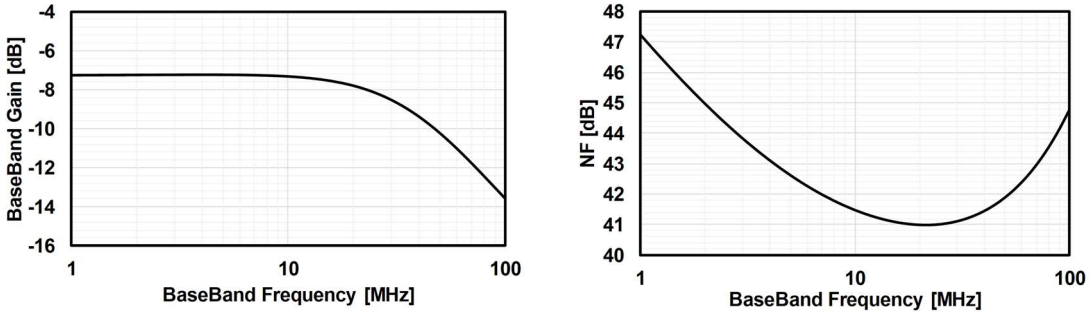


Fig. 2.34: The auxiliary receiver baseband gain and NF.

Fig. 2.33. The receiver power consumption is 32mW while, the power breakdown at 2GHz is shown in Table 2.V. Considering, a receiver gain of 33dB and an integral TX-ISO of 40dB, the TX-to-TIA transfer function is -7dB. The TX-EVM, which is cancelled in digital domain, does not develop significant distortion thanks to a high IB linearity.

Auxiliary receiver:

The AUX-RX has baseband transfer function of -7dB as the main RX. This choice allows to have equal voltage swings at the receivers' outputs. In this way, the DAC reference current is the same for both the receivers. The integral IB AUX-NF is 42dB due to 30dB of input attenuation. Instead, the IB linearity is larger as 56dBm, Fig. 2.34. The last competitive value is possible thanks to the input attenuation and the high TIA driving impedance, Fig.2.26. The derived optimum SNDR is 72,5dB with an input power of 19,7 dBm. A comparison with other works shows that the AUX-RX is the first mixer-first based receiver to provide high $SNDR_{opt}$ at large input power, Table 2.VI.

Whole system:

The employed simulator is Matlab. The simulations are done with the presence of TX-EVM and RX-LO phase noise to consider also reciprocal mixing. Moreover,

Table 2.V: The main receiver power breakdown at 2GHz

LNA	Divider	TIA	TOTAL
12.6mW (39%)	11.4mW (35%)	8mW (26%)	32mW (100%)

Table 2.VI: Auxiliary receiver comparison table

	[34] RFIC '17	[36] JSSC '15	[32] MWCL '16	[35] JSSC '10	This work
Technology	*45 SOI*	*65 CMOS*	*130 CMOS*	*65 CMOS*	*28 CMOS*
Supply [V]	*1.2*	*1.2*	*1.2*	*1.2-2.5*	*1.2*
RF Freq [GHz]	*0.2-8*	*0.15-3.15*	*0.8-1.7*	*0.1-2.4*	*1.8-2.2*
BW [MHz]	*10*	*24*	*20*	*20*	*40*
ATT. [dB]	*-*	*-*	*-*	*-*	*31*
Filter order	*2*	*1*	*1*	*1*	*1*
BB Gain [dB]	*21*	*24*	*43*	*40-70*	*-7*
NF [dB]	*2.3-5.4*	*10.3-12.3*	*8.6-12*	*3*	*42*
IB_IIP3 [dBm]	*5*	*9-19*	*-10*	*-8*	***56***
TX_{opt} [dBm]	*-29.5*	*-16,2*	*-22.9*	*-26.3*	***19.7***
SNDR [dB]	*69*	*70.5*	*66.1*	*68.5*	***72.5***
Power [mW]	*>50*	*22-46*	*65-110*	*37-70*	*20*
FoM [dBJ^{-1}]	*157*	*161.9*	*156*	*155.5*	*166*
Area [mm^2]	*0.8*	*2*	*0.63*	*0.75*	*0.5*

the non-linear behaviours of all the blocks are added to also analyse system limits. In, Fig. 2.35 is shown the overall cancellation result after the last LMS digital filter. In this case, 40dB of cancellation is already developed thanks to the hybrid transformer while extra 60dB is realized thanks to the DACs and to the post processing digital cancellation. The whole cancellation is around 100dB as expected. The TX-EVM and the reciprocal mixing do not add any significant noise contribution to the main receiver noise floor proving that the system is reciprocal mixing insensitive. The main receiver NF degradation is less than 2dB [43-44].

2.3 Conclusion

This work provides an innovative approach to suppress TX Self Interference. Moreover, the overall TX-cancellation is competitive, and the system is designed to sustain larger input power. The balancing impedance provides high linearity performance with limited area occupation. The main receiver has competitive

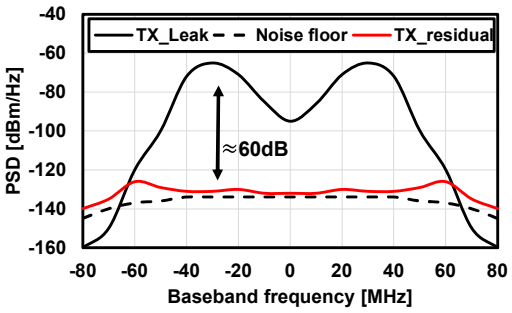


Fig. 2.35: The plot of the overall cancellation. In black, the TX-leakage after the hybrid transformer. The black dashed line is the receiver noise floor while in red the residual TX-leakage after the last LMS filter.

performance in terms of noise and IB linearity, and it employs an innovative OTA architecture to improve bandwidth-power trade-off. The auxiliary receiver is the first one in literature to provide an optimum SNDR larger than 70dB with 20dBm input power. This result is possible thanks to a not power-matched solution. The table 2.VII summarizes all the performance with other Full-Duplex works. The chip will be taped-out after the printing of this thesis and it will be a 2,5x2,5 mm^2 integrated device with more than 100 pads. The measurement results are scheduled on summer 2021.

Table 2.VII: Full Duplex comparison table

		[44] ISSCC '17	[43] RFIC '17	[17] ISSCC '18	[16] JSSC '18	THIS WORK
Architecture		Magnetic-free Circulator + Post proces.	RF DAC + Digital Canc.	EBD + RF Adaptive filters	Adaptive filter + NC PA + LO Canc.	HY trans. + DAC + LMS Filter.
RF band [GHz]		0.61-1	1-2	1.6-1.9	1.7-2.2	1.8-2.2
Technology		65nm	65nm	40nm	40nm	28nm
Voltage Supply [V]		1.2/2.4	1.5	N/A	1.2/1.8/2.5	1.2/1.8
On-chip TX-RX interface		YES	YES	YES	NO	YES
On-chip balancing		YES	-	NO	NO	YES
RF BW [MHz]		20	20	20/40/80	42	**80**
RF TX-to-RX ISO [dB]		40	64 DAC canc.	39	-	40[A]
RF TX-to-RX ISO BW [MHz]		<20	20	200	-	32-40
Cancellation	**[dB]**	40 post process.	25 post process.	34/31/26	50	60
	BW[MHz]	20	20	20/40/80	42	80
Total cancellation [dB]		80	90	73/70/65	80/85	**100**
RX NF degradation[dB]		1.7	N/A	1.6	1.55	2
Main RX NF [dB]		6.3	7-15	8.1	4	6.4+2
Main RX IB-IIP3 [dBm]		-18	N/A	N/A	-5	**14**
Main RX gain [dB]		28	35	42	20-36	33
AUX-RX NF [dB]		-	-	-	-	42
AUX-RX IB-IIP3 [dBm]		-	-	-	-	56
AUX-RX gain [dB]		-	-	-	-	-7
Phase noise reduction		N/A	YES	YES	YES	YES
Main RX power consumption [mW]		72	64	N/A	22	32
AUX- RX power consumption [mW]		-	-	-	-	20
Max. TX output power [dBm][##]		8	5	N/A	N/A	**20**
Integrated PLL		NO	NO	YES	YES	NO
System power consumption [mW]		N/A	N/A	106[#]	N/A	250[x]
TX EVM reduction		N/A	N/A	YES	YES	YES
TX-IL [dBm]		1.8	N/A	N/A	N/A	4
Z_{bal} IIP3 [dBm]		30	-	-	-	**>70**
Canceller area [mm^2]		-	N/A	0.12	N/A	-
AUX-RX area [mm^2]		-	-	-	-	0.5
Z_{bal} area [mm^2]		N/A	-	Off-chip	-	0.7
Chip area [mm^2]		0.94	6.25	4	3.5	6.25

([#]) The entire system without: PA, ADC, DAC and digital domain, ([x]) analog and digital domain. ([##]) The maximum TX output which does not degrade the main RX performance. ([A]) It is the minimum isolation reached in the ISO BW.

PART 3

A Mixer-1st Auxiliary Receiver for analog Self-Interference Cancellation and S2D LNA for MIMO and CA scenarios

This section is divided in two parts. In the first one, a Mixer 1st receiver for Self-Interference cancellation is presented with its measurement results. In the second section, a Single-Ended to Differential LNA suitable for both MIMO and CA scenarios is presented. The mixer first receiver is compliant to Full-Duplex applications, but it explores a different approach to provide analog ISO. The last receiver is a completely different topic.

3.1 A mixer-1st Auxiliary Receiver for analog Self-Interference cancellation.

The FD scenario with its spectrum efficiency and design challenges has been deeply analysed in the previous chapter. The poor isolation between TX and RX paths is a fundamental limit for any FD transceiver and must be faced carefully. A hybrid transformer is a suitable device to manage large input power and it can be used to interconnect TX/RX paths. A balancing impedance, as in the previous chapter, has high linearity performance and it allows to transmit up to 20dBm output power. However, the hybrid transformer can provide high isolation only for a limited bandwidth. A TX-ISO of 40dB is generally considered a reliable value. Therefore, more than 70dB of extra suppression is still required to not degrade RX noise floor. In digital domain, adaptive frequency equalization and non-linear pre-distortion technique can provide TX self-interference cancellation. However, a fully digital cancellation suffers from several limitations. The ADC dynamic range must be considerably increased bringing to a large power consumption. Moreover, the non-linear TX-leakage component requires complex digital architectures to cancel it. An auxiliary receiver (AUX-RX) can be used to sense the TX output power together with its non-linearity and noise (TX-EVM). An analog FIR filter can connect both AUX-RX and main RX outputs to provide proper analog TX self-interference cancellation. The main limitation is due to the AUX-RX performance. Indeed, its noise and distortion are added in the main

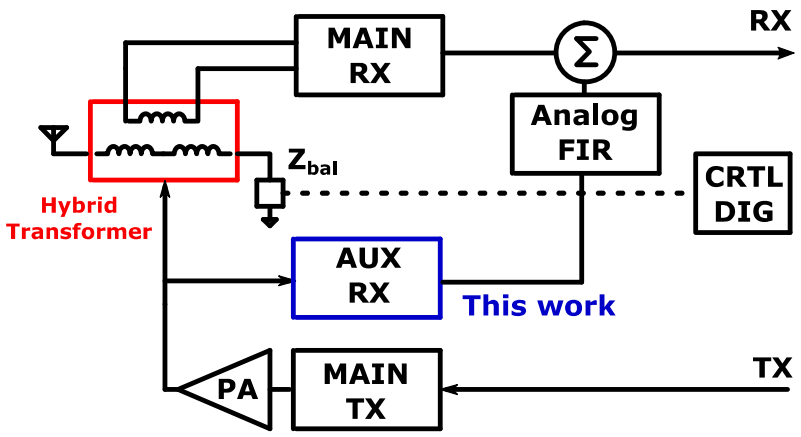


Fig. 3.1: The FD receiver with auxiliary receiver and analog SI-cancellation

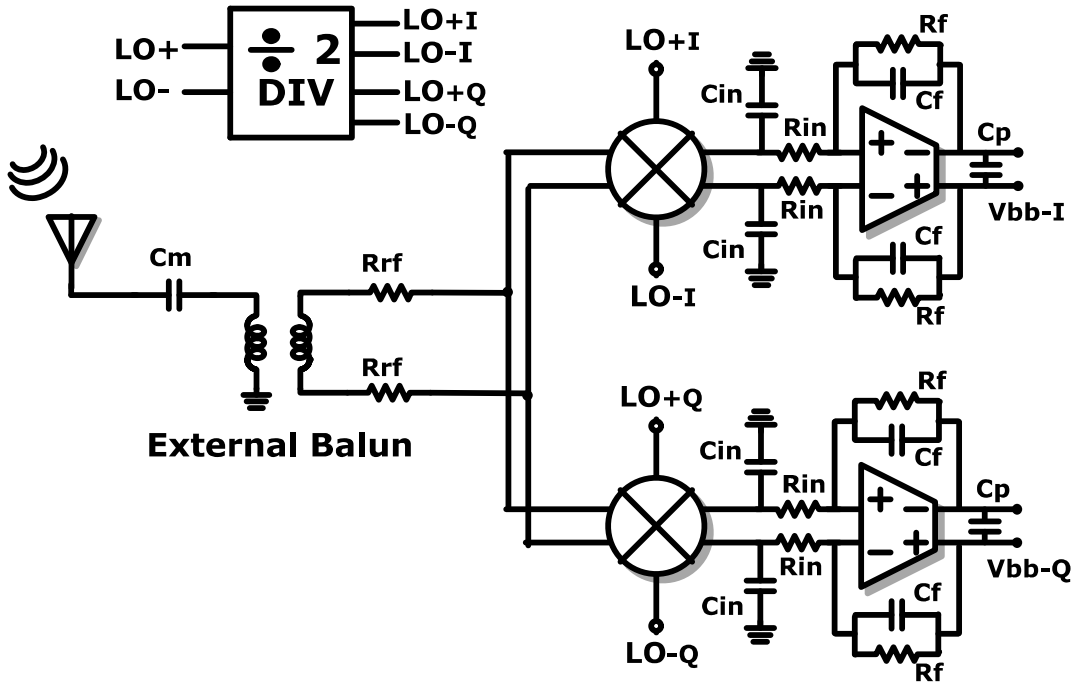


Fig. 3.2: The receiver architecture. On the left, an external balun converts a single-ended input signal to differential.

receiver noise floor, therefore, the AUX-RX requires high SNDR. The suggested solution is shown in Fig. 3.1 with analog self-interference cancellation employing highly linear and low noise auxiliary receiver.

Considering a channel bandwidth of 20MHz and a main receiver NF of 10dB, the input referred noise floor is -91dBm. With 20dBm TX output power and 40dB of hybrid isolation other 70dB of suppression is mandatory. This value determines the required SNDR of the auxiliary receiver. The AUX-RX output provides a

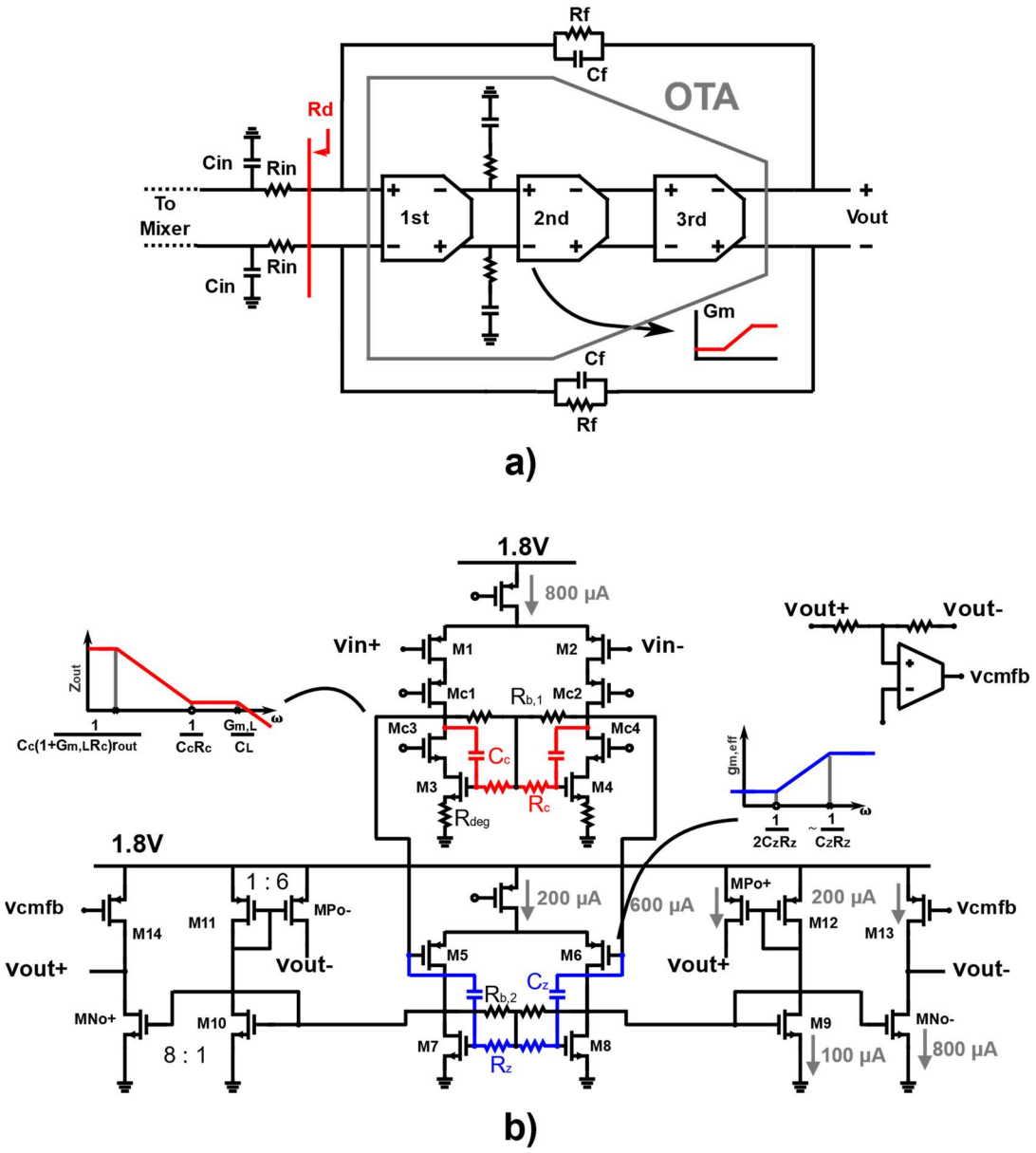


Fig. 3.3: a) The building blocks representation of the TIA. b) The details of the three gain stages.

replica of the transmitted signal which is processed by an analog adaptive FIR filter. The output signal is then subtracted out from the main receiver enabling proper signal detection. The AUX-RX SNDR impacts directly the main receiver performance because it adds uncorrelated noise in main path. Therefore, the auxiliary receiver needs high linearity performance and low power consumption to not significantly increase the system power breakdown. Respect standard receivers the auxiliary can benefit from two important aspects:

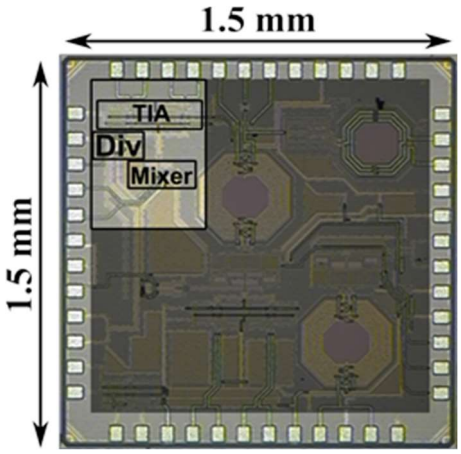


Fig. 3.4: The die photo of the auxiliary mixer 1st receiver.

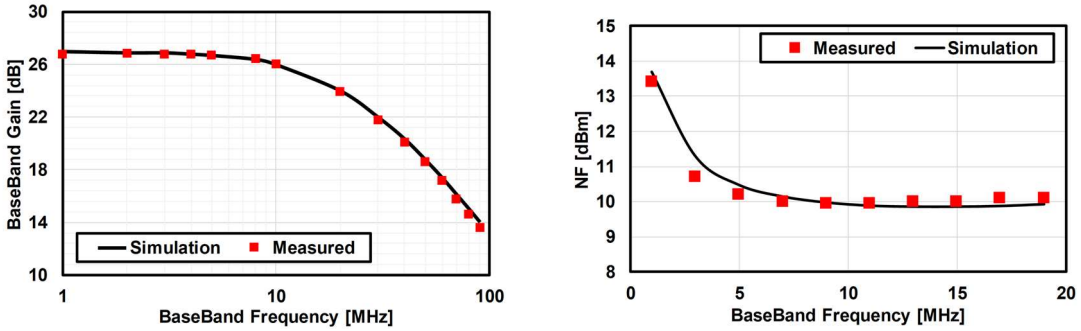


Fig. 3.5: The measured results vs simulations of receiver gain and NF

1) The power level of the signal can be fixed to a constant and known level through a highly linear passive attenuator which connects the PA output to the AUX-RX input.
2) The AUX-RX is not required to be power-matched at the input.

The first point allows the AUX-RX to operate always at the maximum SNDR, the last one to improve its achievable SNDR, as will be shown next.

The mixer first receivers have been already proposed in the past for FD architectures thanks to their high linearity performance [31-37][45]. The proposed receiver is shown in Fig.3.2. The majority of mixer first receivers is focused on out-of-band linearity which is greatly improved for the LNA absence. Instead, in the auxiliary receiver the main concern is the IB linearity. The IB distortion directly impacts the achievable SNDR and, in mixer first topology, is mainly limited by Trans-Impedance Amplifier (TIA). In this case, a different OTA topology has been employed respect the previous chapter, Fig. 3.3. It has not local feedback in the OTA virtual ground and the first stage is a telescopic cascode with degenerated

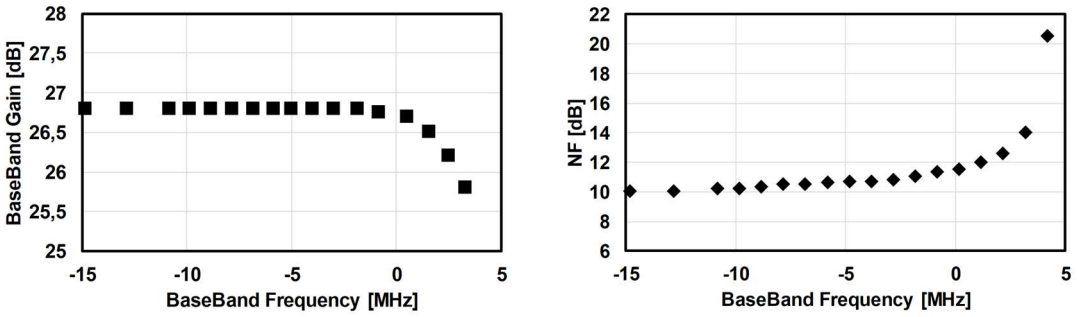


Fig. 3.6: OOB blocking results. On the left, 1dB compression point. On the right, the NF degradation.

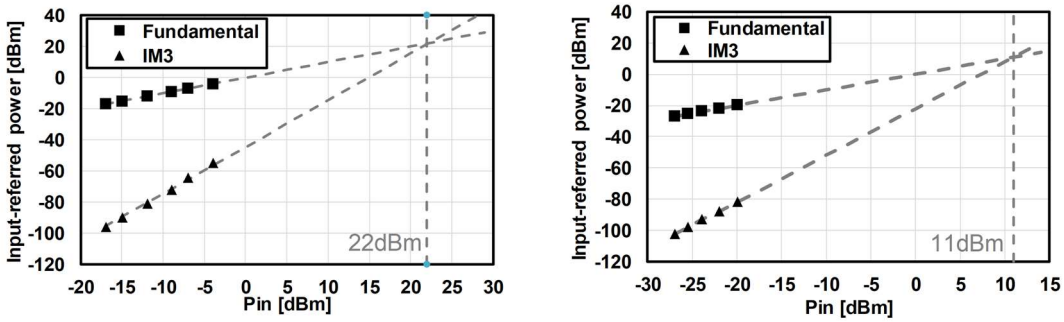


Fig. 3.7: On the left, the measured OOB-IIP3. On the right, the measured IB-IIP3

active load. The TIA IB distortion can be modelled through a current generator at the output of the last stage. In order to reduce the TIA output impedance and, consequently, the non-linear output voltage, the TIA requires high IB loop gain. A three stages amplifier is required to get enough gain but also the feedback network contributes the overall loop gain. The mixer driving impedance is generally low and fixed in power-matched mixer first topology bringing to limited IB linearity and noise performance. However, an auxiliary receiver requires an attenuation between the PA output and the receiver input to not go in saturation condition. The presence of an attenuator removes any requirements in the auxiliary receiver impedances. A small series capacitance can be used to interconnect the TX output to the RX input. This capacitance not only provides attenuation but also increases the driving impedance allowing to get larger TIA loop gain improving its noise and IB-distortion. As a result, the auxiliary receiver SNDR is significantly improved. The OTA performance in terms of stability, noise and linearity are presented in [27] with a full description.

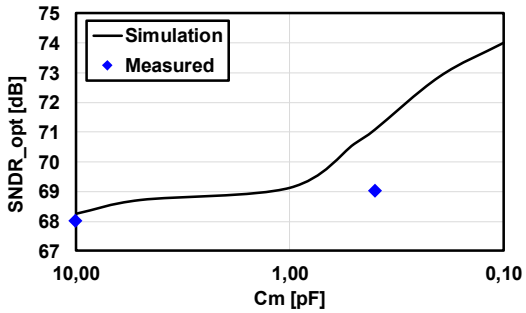


Fig. 3.8: The simulated and measured optimum SNDR vs input capacitance Cm.

Table 3.I: Mixer-First comparison table

	[34] RFIC '17	[36] JSSC '15	[35] JSSC '10	[45] THIS WORK
Technology	45 nm SOI	65nm CMOS	65nm CMOS	28nm CMOS
Supply [V]	1.2	1.2	1.2-2.5	1.8
RF Freq [GHz]	0.2-8	0.7-3.8	0.1-2.4	1-2.6
BB BW [MHz]	10	3	20	20
BB Gain [dB]	21	40	40-70	26.8
NF [dB]	2.3-5.4	2.5-4.5	3	10
IB_IIP3 [dBm]	5	-30	-8	11
SNDR [dB]	67.9	45.2	68.5	69
Power [mW]	>50mW	27.4-75.4	37-70	20
Area [mm^2]	0.8	0.23	0.75	0.31

Measurement Results and SNDR improvement

The final chip is shown in Fig. 3.4, was fabricated in 28nm CMOS technology with 1.5x1.5mm^2 chip area. The active section, including the frequency divider of 2, is only 490umx640um for an overall area consumption of 0.31mm^2. The feedback resistance R_f and the capacitance C_f are equal to 2.5kΩ and 3pF setting the TIA pole at 20MHz. The capacitance C_{in} is added in the OTA virtual ground to filter out-of-band blockers. A small resistance R_{in} is added in series to C_{in} to develop a zero at high frequency which is necessary to loop stability. Two input resistors R_{RF} ensure impedance matching through an off-chip 1:2 balun with 10pF series

capacitance Cm (Anaren B0430J50100AHF). Any TIA draws 3mA from 1.8V supply and the receiver has an overall power consumption of 20mW.

The measured down-conversion gain is 26.8dB with -3dB at 20MHz as expected. The measured noise figure is 10dB with flicker noise corner at 1MHz. The results are shown in Fig. 3.5. The out-of-band blocking results are shown in Fig. 3.6 with blocker fixed at 100MHz. The 1dB compression point corresponds to 3.3dBm while the 1dB NF to -2dBm input power. The former is limited by TIA clipping voltage while the latter by reciprocal mixing. The IIP3 was measured both In-Band and Out-Of-Band (OOB) with two tones test. The IB was tested with two tones at 3 and 5MHz while the OOB at 101 and 201MHz. The IB-IIP3 and OOB- IIP3 are 11dBm and 22dBm, respectively, Fig. 3.7.

As explain before, for an auxiliary receiver, it is important to derive the best SNDR. In this application, it should be as high as 70dB. The optimum input power is derived by (1.16) and is equal to -23dBm. So, the optimum SNDR is 68dB. In order to improve it, the off-chip capacitance Cm has been reduced to increase the driving impedance. In Fig. 3.8, the SNDR optimum vs the output capacitance Cm. The measurement results prove that a Cm of 400fF increases the SNDR to 69dB, reducing the gap from 70dB. In simulation, further Cm reduction to 100fF would still improve SNDR up to 74dB. The simulation and measurement results diverge between each other at low Cm values due to the parasitic capacitance in the output pad. Indeed, its presence limits any further SNDR improvement. This limit would not be possible if the entire auxiliary receiver were integrated. The table 3.I summarizes the measured results and compares its performance with other works. In [36] this work has similar power consumption but much less SNDR.

In conclusion, the mixer-1st auxiliary receiver has competitive performance in terms of area, power consumption and IB linearity. Moreover, it explores a not power-matched solution to further improve receiver SNDR.

3.2 A sub-6GHz band Single-ended to differential LNA for MIMO and CA scenarios.

In order to sustain the exponential growth of data-rates in handheld devices operating in sub-6 GHz band, techniques that make use of parallel receivers like Multi-Input-Multi-Output (MIMO) and Carrier-Aggregation (CA) have been explored [2]. The expectation with the proliferation of 5G is to reach systems with more than 20 receivers operating in parallel. To reduce chip costs, a wideband RF front-end that can cover the entire sub-6GHz spectrum with small area consumption is required. Considering the large number of parallel devices, to save on pin count, a single-ended input receiver is preferred [2]. However, differential topology provides better performance in common-mode noise rejection and disturbances. Therefore, the signal should be converted in differential mode as early as possible in the receiving chain. Good differential symmetry and linearity performance can be achieved with an on-chip transformer (balun) in front the mixer-first receiver or in the LNA input. However, the achievable bandwidth is limited (1-3GHz in [4]). In other work, a reconfigurable 3-coil transformer has covered the entire sub-6 GHz band at cost of very large area occupation [46].

Inductor-less LNA has small area consumption and can cover wide bandwidth [2]. In the past, a noise-cancelling common gate (CG) common-source (CS) topology has proved to be effective in the single-ended to differential transformation. However, to get low noise performance, the current signal in the CS brunch is much larger than CG developing even-order distortion. Moreover, the CG requires a current source or an off-chip inductor with noise degradation and larger area occupation. The receivers with inverter-based shunt feedback LNAs have proved small area and low noise performance in both single-ended and differential architectures [47-49]. The shunt-feedback LNAs suffer of the low impedance loading due to the mixer, forcing the LNA to have limited achievable gain. A multi-stage topology overcomes this limitation and is suitable to drive low impedance.

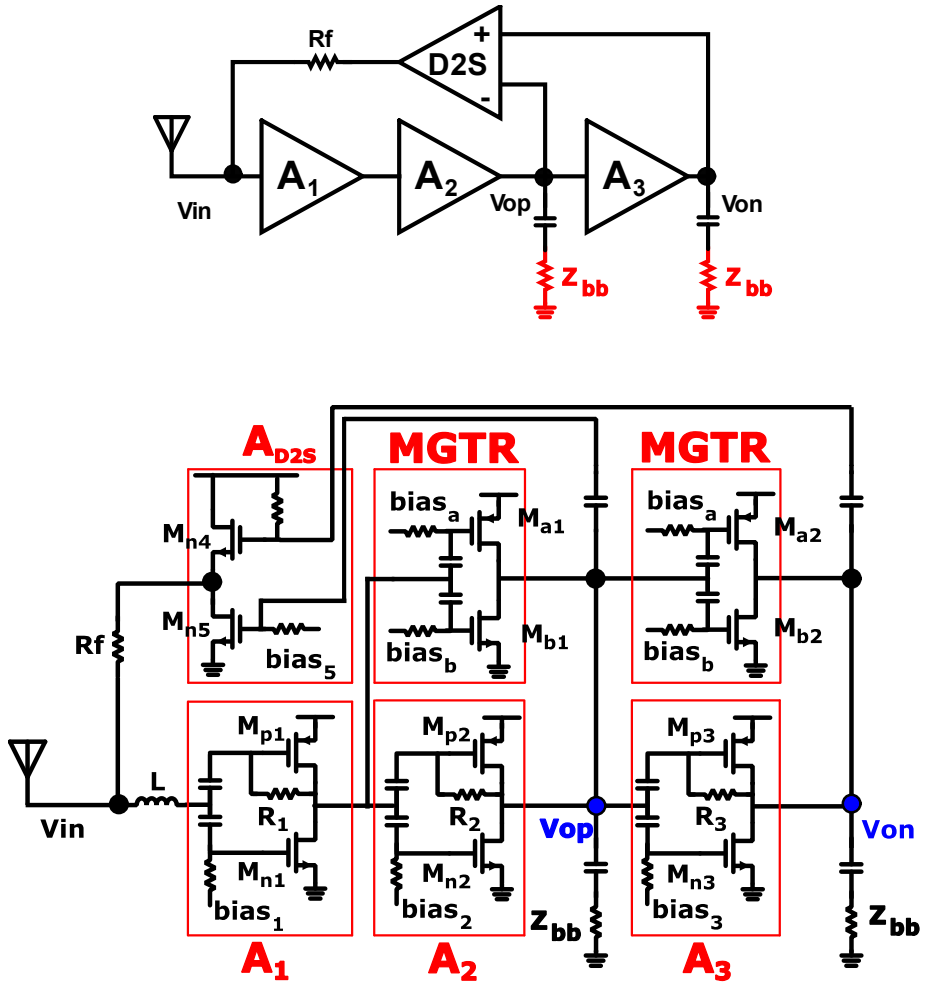
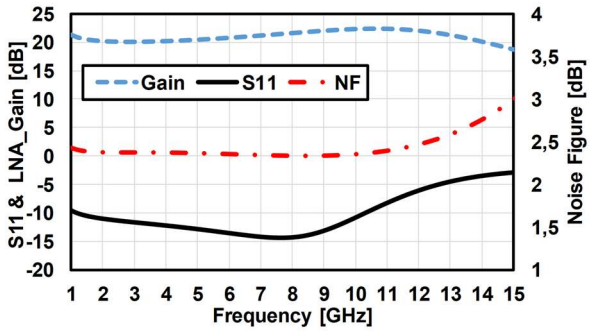


Fig. 3.9: On the top, the LNA building blocks representation. Below, the design description of each block.



Parameter	Percentage [%]
Port	54.5
1st stage	24.7
Inductor	5
D2S	4.9
Rf	4.2
Zbb	2.3
Other	4.4
Total	**100**

Fig 3.10: The LNA gain, NF and S11 performance vs LO frequency. On the right, the LNA noise breakdown at 4GHz.

The suggested LNA solution is shown in Fig. 3.9. It employs an inverter-based shunt-feedback active balun-LNA with reduced area consumption which is suitable for CA and MIMO applications.

The forward path is constituted by a gain stage A_1 followed by two inverting unity-gain stages A_2 and A_3. The last two stages have in parallel auxiliary stages Multi-

Element	Size
Mp1	48um/30nm
Mn1	40.5um/30nm
Mp2/Mp3	7.2um/30nm
Mn2/Mn3	5.4um/30nm
Ma1/Ma2	15.6um/30nm
Mb1/Mb2	9.3/30nm
Mn4/Mn5	2.4um/30nm
L	1nH
R1	28kΩ
R2/R3	20kΩ

Fig. 3.11: The LNA sizing.

Gate Transistors (MGTR) to improve LNA IIP3. The high-valued feedback resistors $R_{1\text{-}3}$ are employed for biasing purpose. The resistors Z_{BB} are the load of the following stages and estimated to be around 60Ω. The inverter-based amplifiers benefit of the CMOS scaling reaching high ft values but limited gain. The two last stages A_2 and A_3 allow to not load the first stage which develops the gain for the entire loop. The differential output $V_{op/on}$ is taken at the input and output of the third and last stage A_3 exploiting its inverting feature. A differential to single-ended (D2S) buffer combines the two LNA outputs and it drives a feedback resistor R_f providing wideband input matching.

The gain of the first stage is described as follow:

$$\mathrm{A}_1 = -g_{m1}(r_{01} \,//\, R_1) \cong -g_{m1} r_{01} \tag{3.1}$$

where g_{m1} and r_{01} are the transconductance gain and resistance of the first stage A_1. Considering, the inverting gain stage of A_2 and A_3, the entire LNA gain is equal to:

$$\mathrm{A}_{LNA} = A_1 A_2\,(1 - A_3) = -2A_1 \tag{3.2}$$

Now, is possible to derive the input matching.

$$R_{in} = \frac{R_F + \frac{1}{g_{m5}}}{(1 + A_{LNA})} // \frac{R_1 + r_{o1}}{1 - A_1} \cong \frac{R_F + \frac{1}{g_{m5}}}{(1 + A_{LNA})} \tag{3.3}$$

In (3.3) the second term is considered large. For D2S symmetry reasons, the g_{m4} is equal to g_{m5}.

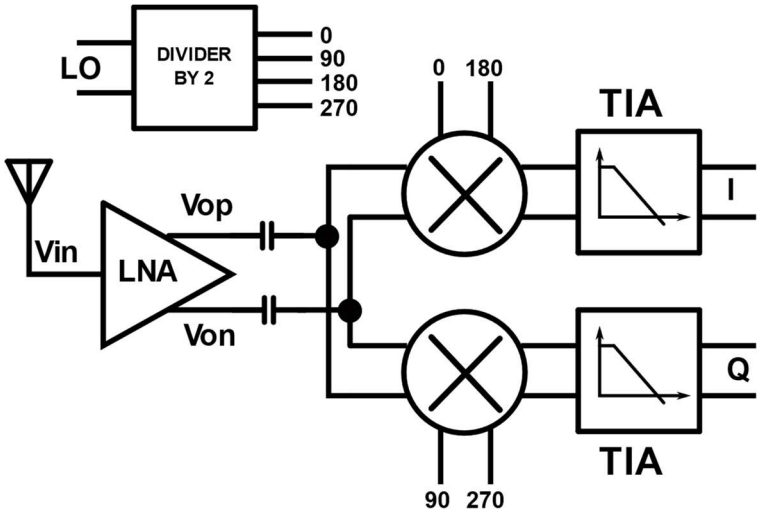


Fig. 3.12: The entire receiver building blocks representation.

About the LNA noise performance, considering the dominant contributors the LNA NF is expressed as follow:

$$F = 1 + \left(\frac{\gamma}{g_{m1}R_s} + \frac{\gamma}{g_{m2}R_sA_1^2} + \frac{\gamma/4}{g_{m3}R_sA_1^2}\right)\frac{4(1-A_1)^2}{(1-2A_1)^2} + \frac{\alpha}{1-2A_1} \tag{3.4}$$

The main three contributors are due to A_1, A_2 and A_3, respectively. The last term is due to the feedback network where α is defined as:

$$\alpha = \frac{R_{F0} + 2\gamma/g_{m5}}{R_{F0} + 1/g_{m5}} \tag{3.5}$$

If A_1 is the main gain contributor in the LNA, the equation (3.4) proves that the first stage becomes the dominant noise contributor. With a g_{m1} of 90mS and $|A_1|$=5.5, the LNA NF is equal to 2.4dB. A small inductor (1nH) peaking inductor L is added in the LNA loop. To provide low noise, the first stage requires high transconductance gain which develops large parasitic capacitance at the input node. This capacitance degrades the input matching at high frequency making the equation (3.3) not valid anymore. The inductor resonates with the parasitic capacitance extending the input matching from below 6GHz to above 10GHz with a small noise degradation. The simulated LNA NF, gain and S11 are reported in Fig. 3.10 with a noise breakdown at 4GHz.

Concerning the LNA linearity, the last two stages have large input signal, and they inject significant distortion into the loop degrading OOB IIP3. As already discuss in previous chapter, high loop gain decreases output load and allow to reach better linearity performance. In this case, the matching condition force the

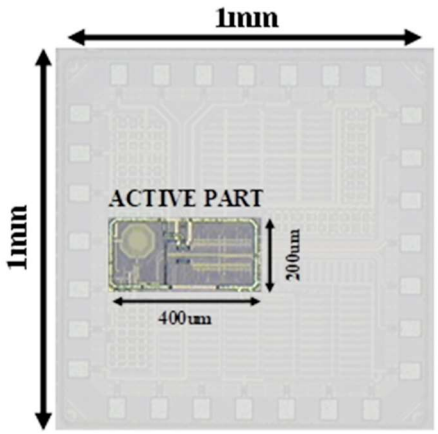


Fig. 3.13: The chip photo.

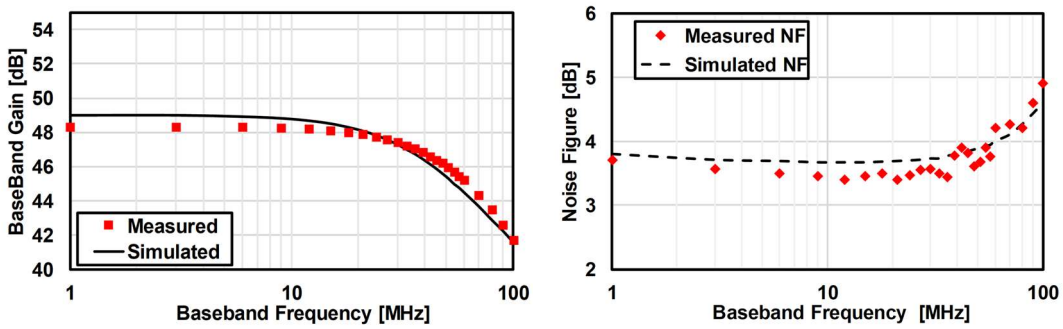


Fig. 3.14: The simulation and measurement results of gain and NF.

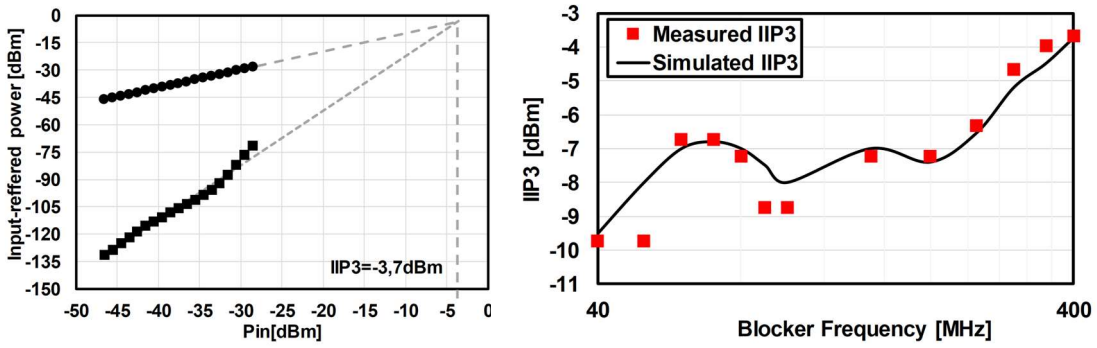


Fig. 3.15: The measured OOB-IIP3 with two tones test and the measured IIP3 vs blocker frequency.

loop gain to be just below unity, therefore, the distortion is not compressed by loop. To improve distortion, the last two stages A_2 and A_3 are implemented with two parallel inverters, MGTRs. The main stages operate in strong inversion while the MGTRs in weak inversion. These working conditions exploit the opposite signs of the two biasing points. Once, the proper biasing is delivered to the MGTRs, the third order distortion is significantly reduced. About the second order

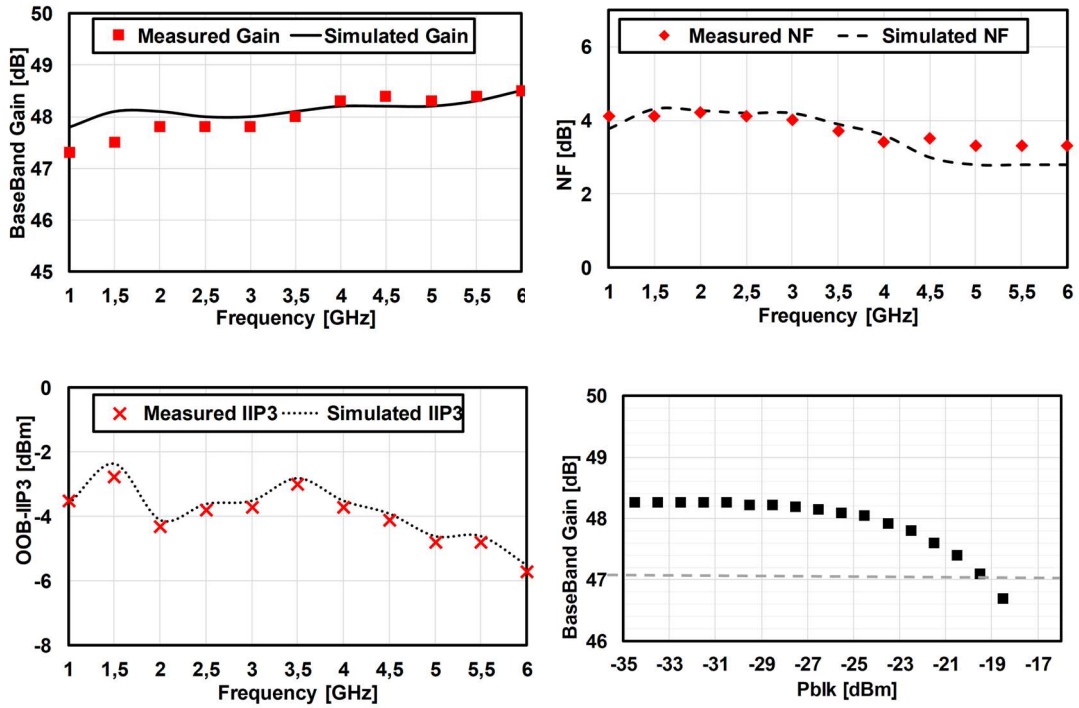


Fig. 3.16: Conversion gain, NF and OOB-IIP3 vs carrier frequency and 1dB compression point.

distortion, the P-N structure allows to provide self-cancellation in each stage. The D2S device does not contribute significantly in the LNA distortion. The source follower is degenerated by the resistor in feedback while the CS non-linear contribution is limited. Indeed, the pair M4-M5 behaves like a current mirror where the voltage to current non-linearity of M_{n4} is compensated. The sizing of each LNA elements is shown in Fig. 3.11.

Measurement Results

The wideband direct-conversion receiver front-end is show in Fig. 3.12. It has been designed in 28nm CMOS technology. It has an active balun-LNA, LO generation circuit, I and Q passive mixers and baseband TIAs. The LNA draws 7.1mA from 1V power supply. The TIA topology is the same presented in Fig. 3.3. The amplifier has unity-gain bandwidth of 1GHz, and it burns 1.8mA from 1.8V power supply. The feedback resistance and capacitance are 2.5kΩ and 1.6pF setting the TIA pole at 40MHz. The LO circuit consumes other 11.5mW at 5GHz fixing the entire receiver power consumption at 22.2mW. The chip has an active area of 0.4x0.2mm^2 while the inductor is only 0.1x0.1mm^2, Fig. 3.13. The

Table 3.II: Sub-6GHz receiver comparison table

	[50] RFIC '17	**[33] ESSCIRC '15**	**[46] VLSI '17**	**[51] JSSC '17**	**[52] THIS WORK**
CMOS Tech	14nm	65nm	65nm	28nm	28nm
RF Freq [GHz]	0.6-2.7	0.8-3	0.9-5.8	0.4-6	1-6.2
RF BW [MHz]	-	-	20	1-100	80
BB Gain [dB]	62	40	22-25	70-58	48.2
NF [dB]	3-5	5.5-7.8	2.9-3.8	2.2-3.1	3.4-4.2
IB/OOB IIP3 [dBm]	-2.5/0	-/-17	>-12.8/NA	NA/5	-10/-3.7
Balun	Passive	Passive	NO	NO	**Active**
Power [mW]	16	32-38	79-98	40	**22.2**
Area [mm^2]	0.66	0.5	4.2	0.6	**0.08**

simulated and measured results of gain and NF are shown in Fig. 3.14 with carrier frequency set at 4GHz. The down-converted gain is 48.2dB while the NF is 3.4dB at 10MHz. The two tones test has been measured with 3rd intermodulation product fixed at 10MHz. The tones are spaced by 390MHz with LO frequency at 4GHz. The OOB-IIP3 is -3.7dBm in good agreement with simulation. The 3dB/dB slope is observed up to -30dBm where the MGTRs enter in compression. The two tones have been tuned from IB to OOB showing an IB-IIP3 of -10dBm at 40MHz, Fig.3.15. The gain, NF and OOB-IIP3 performance vs carrier frequency from 1 to 6GHz are shown in Fig 3.16 together with the 1dB compression point at 4GHz. The receiver has not been tested over 6GHz frequency because the divider has not been designed to cover larger frequencies. The comparison Table 3.II summarizes the receiver performance with other works. Thanks to the active Balun-LNA, the receiver provides wide RF bandwidth, small chip area and low power consumption [33] [46] [50-52].

Conclusion

The FD technique allows to significantly improve the spectral efficiency compared to TDD and FDD solutions. Unfortunately, to operate at large TX output power, the receiver suffers many challenges that must be faced carefully. The proposed system architecture provides three cancellation techniques to suppress the TX-leakage. The first one is realized through the hybrid transformer, which provides 40dB of average isolation. The antenna impedance is frequency-dependent and limits further improvements. The second cancellation is accomplished by current-mode DACs which suppress only the TX linear components. A filtered-X LMS filter tracks the system impulse response to develop proper cancellation. Finally, an auxiliary receiver is connected to the PA output to down-convert the TX signal, including noise and distortion. An LMS-FIR digital filter combines the two receivers' output to provide the third and last cancellation in the digital domain. The receivers and DACs share the same noisy clock to make the system immune to reciprocal mixing. The simulations results show roughly 100dB of TX-leakage isolation with less than 2dB of NF degradation. This is possible thanks to the auxiliary receiver which provides more than 70dB of SNDR.

The system is designed in TSMC 28nm and it will be fabricated after the printing of this thesis. The balancing impedance provides more than 70dBm of IIP3 referred to the PA output with limited area occupation. The main and auxiliary receivers gain, NF and IB-IIP3 are 33/-1dB, 6.4/42dB and 14/56dBm, respectively. The total die area is 2.5x2.5mm^2, including analog and digital circuits with more than 100 pads, which enable extensive system characterization.

A mixer first receiver has been tested to demonstrate that this kind of receiver can provide large SNDR and is suitable to be employed as the auxiliary receivers for FD systems.

As a side project, a different receiver for MIMO and CA scenarios has been discussed. In this case, the main concerns are the active area consumption and the pad count. To meet these requirements a shunt-feedback inverter-based

balun-LNA is introduced in the receiving path. The LNA feedback allows to significantly extend the input matching and to cover the entire sub-6GHz band. The MGTRs are connected in parallel to the second and third gain stages to improve LNA OOB-IIP3. The receiver gain, NF, OOB-IIP3 and power consumption are 48.2dB, 3.4dB, -3.7dBm and 22.2mW, respectively. The area occupation is competitive with only 0.08mm^2 of active area.

Appendix

Appendix A

A standard CLC circuit is shown in Fig. A.1 together with a modified version useful to analyse it, Fig.A.1b. The inductor L is splitted with the following condition $L_1 + L_2 = L$. Thanks to the inductor division, a new node V_{mid} is defined and it becomes the central point of the entire analysis. Now, the CLC network can be analysed as two PI-matched sub-networks which are connected to their own fix resistors. R_s is a fix 50Ω resistor which represents the off-chip impedance as explain in chapter 2, while the last one represents a generic load R_{hy}. Considering the PI-matched network with fix 50Ω, the parallel RC network can be transformed in the equivalent RC series with the following formulas:

$$R_1 = \frac{R_s}{1 + Q_1^2} \tag{A.1}$$

$$Q_1 = R_s C_s \omega \tag{A.2}$$

$$C_1 = C_s * (1 + \frac{1}{Q_1^2}) \tag{A.3}$$

The previous equations show that for a fix R_s and working frequency $\omega/2\pi$, for each R_1 value is possible to derive all the other parameters as quality factor, C_1 and C_s. Once, C_1 is derived by (A.3) for a wanted R_1, it is possible to resonate it with a fix inductor.

$$L_1 = \frac{1}{\omega^2 C_1} \tag{A.4}$$

Summarizing, the PI-matched allows to derive all the parameters by only R_1 and R_s. The same considerations can be also extended to the other PI-matched network and show below for simplicity:

$$R_2 = \frac{R_{hy}}{1 + Q_2^2} \tag{A.5}$$

$$Q_2 = R_{hy} C_{hy} \omega \tag{A.6}$$

$$C_2 = C_{hy} * (1 + \frac{1}{Q_2^2}) \tag{A.7}$$

$$L_2 = \frac{1}{\omega^2 C_2} \tag{A.8}$$

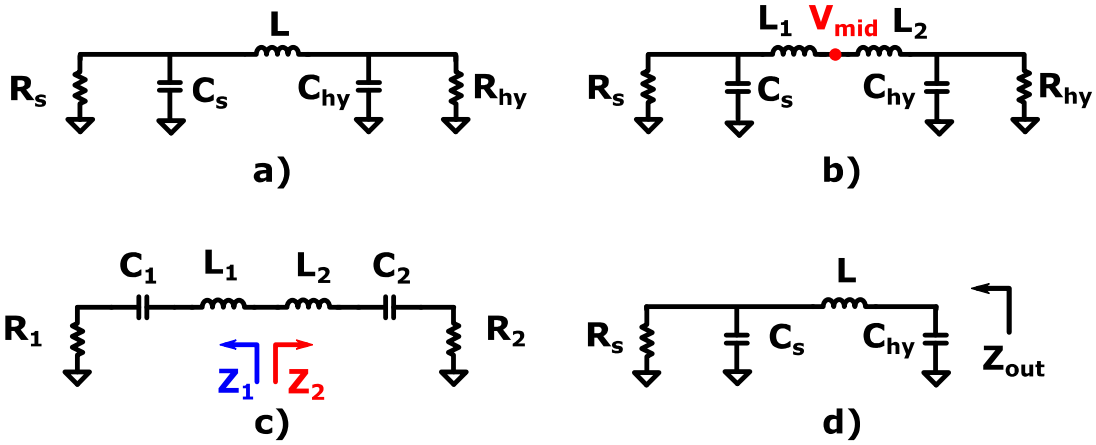


Fig.A.1: The CLC network. The figures show the required steps to design properly the CLC network for a wanted: operating frequency, quality factor and impedance.

Now, if the condition that $Z_1 = \mathrm{R}_1 = \mathrm{R}_2 = Z_2$ is forced in both sub-networks, Fig.A.1c, the circuit is now matched at $\mathrm{V}_{\mathrm{mid}}$. Therefore, the impedance seen in $\mathrm{Z}_{\mathrm{out}}$ is exactly equal to R_{hy}, Fig. A.1d. In practice, R_{hy} can be considered as the impedance to realize with the CLC network. With the previous steps is possible to realize the proper impedance from a generic CLC network. Being the same impedance R_{hy} realized with different values of $\mathrm{R}_1 = \mathrm{R}_2$, the redundancy is demonstrated.

$$\mathrm{Q} = \mathrm{Q}_1 + \mathrm{Q}_2 \tag{A.9}$$

$$\mathrm{L} = \mathrm{L}_1 + \mathrm{L}_2 \tag{A.10}$$

The last two equations indicate the overall quality factor and the required inductor L.

Appendix B

In Fig. B.1 is shown a standard three stages feedforward compensated OTA. The FF stage by-passes the second and third stage. To have comparable architectures, the connection between the first and the FF stages is the same of the topology in Fig. B.2. In this section, the local feedback compensation technique will demonstrate its superiority in terms of high frequency loop gain and lower power consumption.

Considering, the architecture in Fig. B.1 we can derive its transfer function between the first stage and the OTA's virtual ground.

$$V_x = \left(V_f g_{mff} + \frac{V_1 g_{m2} g_{m3} R_2}{sR_2C_2 + 1}\right) \frac{\frac{R_3}{sR_3C_3 + 1}\left(R_Z + \frac{R_S}{sR_SC_S + 1}\right)}{\frac{R_3}{sR_3C_3 + 1} + \frac{R_f}{sR_fC_f + 1} + R_Z + \frac{R_S}{sR_SC_S + 1}} \qquad \text{(B.1)}$$

V_f is the FF stage input, V_1 is the first stage output or second stage input, R_S is the down-converted impedance by mixing effect and R_Z is a small resistance added in the loop to develop a high frequency zero. The transconductance gains g_m, the capacitances C and the resistors R are relative of each block and the subscript represents the stage itself. For the sake of simplicity, the load of any stage is described though a standard RC circuit.

As already explain in chapter 2, the pole of the last stage is equal to the zero develops by R_fC_f. Moreover, at the same frequency, it is developed another pole R_SC_S due to driving impedance load. Therefore, we can establish an equality in equation (B.1)

$$R_3C_3 = R_fC_f = R_sC_s \cong 40\text{MHz} \qquad \text{(B.2)}$$

The equation (B.1) can now be simplified in:

$$V_x = \left(V_f g_{mff} + \frac{V_1 g_{m2} g_{m3} R_2}{sR_2C_2 + 1}\right) \frac{\frac{R_3}{sR_sC_s + 1}\left(R_Z + \frac{R_s}{sR_sC_s + 1}\right)}{R_Z + \frac{R_s + R_3 + R_f}{sR_sC_s + 1}} \qquad \text{(B.3)}$$

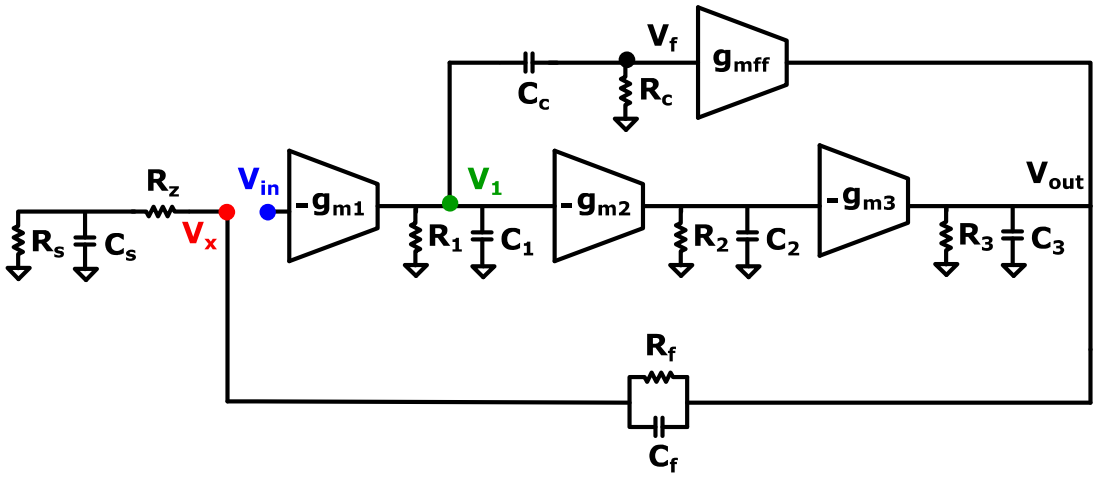


Fig.B.1: A single-ended version of a three stages feedforward compensated OTA.

$$V_x \cong \frac{R_s + R_Z}{R_Z + R_s + R_f + R_3}\left(V_f g_{mff} + \frac{V_1 g_{m2} g_{m3} R_2}{sR_2C_2 + 1}\right)\frac{R_3}{sR_sC_s + 1} * \\ * \frac{sR_z//R_sC_s + 1}{s\frac{R_sR_Z}{R_3 + R_s + R_Z + R_f}C_S + 1} \tag{B.4}$$

The last pole in (B.4) is at very high frequency and is negligible for this application. The previous equation can be rewritten as:

$$V_x \cong \frac{R_s + R_Z}{R_Z + R_s + R_f + R_3}\left(V_f g_{mff} + \frac{V_1 g_{m2} g_{m3} R_2}{sR_2C_2 + 1}\right)\frac{R_3(sR_zC_s + 1)}{sR_sC_s + 1} \tag{B.5}$$

The transfer function between V_f and V_1 is equal to:

$$V_f = V_1 \frac{sR_CC_C}{sR_CC_C + 1} \tag{B.6}$$

Now we force this condition:

$$R_CC_c \approx R_2C_2 \tag{B.7}$$

The equation (B.5) becomes:

$$V_x \cong \frac{(R_s + R_Z)\, g_{m2} g_{m3} R_2 R_3 V_1}{R_Z + R_s + R_f + R_3} \frac{(sR_zC_s + 1)(\frac{sC_cR_cg_{mff}}{g_{m2}g_{m3}R_2} + 1)}{(sR_sC_s + 1)(sR_2C_2 + 1)} \tag{B.8}$$

V_1 is the gain of the first stage and is equal to:

$$V_1 \approx -\frac{g_{m1}R_1(sR_cC_c + 1)}{sR_1(C_1 + C_C) + 1}V_{in} \tag{B.9}$$

Considering that the zero introduced by R_cC_c is used to cancel the pole of the second stage, the equation (B.8) becomes:

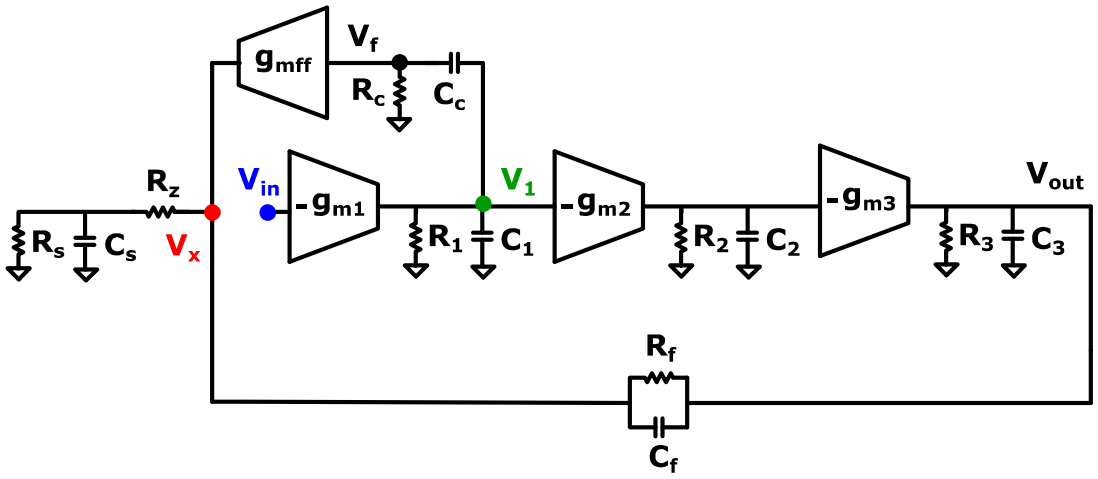


Fig.B.2: A single-ended version of a three stages local feedback compensated OTA

$$\frac{V_x}{V_{in}} \cong \frac{(R_s + R_Z)\,A_0}{R_Z + R_s + R_f + R_3} \frac{(sR_zC_s + 1)\left(\frac{sC_cR_cg_{mff}}{g_{m2}g_{m3}R_2} + 1\right)}{(sR_sC_s + 1)(sR_1(C_1 + C_C) + 1)} = G_{loop} \qquad \text{(B.10)}$$

The equation (B.10) represents the loop gain of a conventional feedforward compensated OTA. A_0 is the open-loop low frequency gain and is equal to $-g_{m1}g_{m2}g_{m3}R_1R_2R_3$. The equation in (B.10) shows two low frequency poles at 40MHz by design, and two zeros at high frequencies. One is introduced by resistor R_z with the large capacitor C_s, while the last one by the FF stage itself. The FF's zero is inversely proportional in frequency to its transconductance gain g_{mff}.

Considering, the architecture in Fig. B.2 we can repeat the same procedure to derive its loop gain.

$$\frac{V_x}{V_{in}} = \frac{(R_S + R_Z)A_0}{R_3 + R_S + R_Z + R_f} \frac{(sR_zC_S + 1)\left(s\frac{C_cR_Cg_{mff}}{g_{m2}g_{m3}R_2}\frac{R_f + R_3}{R_3} + 1\right)}{(sR_SC_S + 1)(sR_1(C_1 + C_C) + 1)} = G_{loop} \qquad \text{(B.11)}$$

With $R_3C_3 = R_fC_f$ equality is possible to derive a more intuitive equation:

$$\frac{V_x}{V_{in}} = \frac{(R_S + R_Z)A_0}{R_3 + R_S + R_Z + R_f} \frac{(sR_zC_S + 1)\left(s\frac{C_cR_Cg_{mff}}{g_{m2}g_{m3}R_2}\frac{C_f + C_3}{C_f} + 1\right)}{(sR_SC_S + 1)(sR_1(C_1 + C_C) + 1)} = G_{loop} \qquad \text{(B.12)}$$

The equation B.12 represents the loop gain of a local feedback compensated OTA. It shows an important difference than the equation B.10. The zero

introduces by FF stage is multiply by an extra coefficient always larger than 1. This means that to develop the same zero in frequency, the local feedback requires less g_{mff} or, in other words, less power consumption.

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