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Department of Electrical, Computer and Biomedical Engineering

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High Frequency DC-DC Buck Converter for Automotive Post-Regulated Applications

Supervisors:
Prof. Edoardo Bonizzoni
Ing. Cristan Garbossa

Ph.D Coordinator:
Prof. Piero Malcovati

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Filippo Boera

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"Arrivederci"
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Introduction

The current trends in the automotive market are pushing toward an ever increasing integration of electronic components in a car. Modern cars need to be safer and smarter, hence there is the need of a lot of sensors, radars, microcontrollers etc. Consequentially, the power supply circuits that are needed to power up all these devices starting from the 12-V battery of a car are also facing an intense thrust to integration. More integration of the power supply circuits means that the production costs and area of the components are significantly reduced, but leads to less flexibility of the circuits and less robustness to high temperatures. The traditional approach was to directly convert the battery voltage to each desired lower voltage using either Low Dropout Regulators (LDOs) or switching DC-DC converters (also called Switching Mode Power Supply, SMPS), depending on the application. Nowadays a post-regulated approach is preferred: one converter downshifts the battery voltage to an intermediate value, typically in the range of 4∼8 V, and that intermediate voltage can either directly supply some circuits, or be the input of multiple successive regulators, that will each power up the circuits that require lower supply voltages. While complicating the design, this approach is preferred due to a higher efficiency, and the possibility of a more robust thermal isolation of the circuits.

Switching DC-DC converters are usually very expensive and bulky, and this is mostly due to the presence of the inductor, which can often cost more than the chip itself, both in terms of money and area consumption. The typical switching frequency of a DC-DC converter is a few MHz. By increasing the switching frequency, a much lower inductance value can be used without degrading the current ripple. Having a lower value of inductance means that the physical dimension of the inductor is smaller, resulting in an advantage in chip cost and area.

When dealing with power converters, efficiency is obviously another key parameter, especially in the field of automotive where a high efficiency is beneficial for both environmental and economical reasons. The main topic of this

PhD research is the study and of this research is the study and the design of a DC-DC buck converter with specifications aligned with the post-regulated domain, switching at 50/100 MHz. This work has been possible thanks to the collaboration between the University of Pavia and Infineon Technologies Italy, with help from both the Pavia and Padova sites.

The second topic of this thesis is the design of a Hybrid Single-Inductor Bipolar-Output DC–DC Converter with Floating Negative Output for AMOLED Displays. As AMOLED Displays have become one of the standard technologies for mobile and TV screens, the research for more compact and efficient solutions for the supplies of the pixels is thriving. As AMOLED displays need two supply voltages (one positive and one negative) to turn on, two separate DC-DC converters are typically used to provide the necessary voltages from the battery. A Single-Inductor solution can generate both voltages with only one inductor, hence saving a lot of money and area on the chip. This part of the work has been conducted thanks to the collaboration between the University of Pavia and the University of Macau.

Chapter 1

High Frequency DC-DC Converters In Post-Reg Environment

This chapter gives an overview of what is intended with Post-Regulated DC-DC converter, and the typical specifications in this domain. Then, a basic review of the theory of switching DC-DC converters is given for both the power stage and the control loop, focused on the topics that are more influenced (positively or negatively) by going to high switching frequency.

1.1   Post-Regulated Approach

Nowadays two are the major trends that are pushing the automotive power supply market: integration and transition to Pre/Post regulation architecture. The push for more integration is well-known and common to most applications in electronics. A higher level of integration of electronic components translates in a lower cost and a lower area usage. However, this comes with a couple of downsides: firstly the circuits become less flexible to different uses, and secondly the thermal design becomes more challenging, as it is possible to have different circuits which are integrated in the same package but have different thermal requirements. The second big trend is the transition from direct conversion the Pre/Post regulated approach. As mentioned in the introduction, the traditional approach for supplying all the electronic parts of a car is direct conversion: each block has its own dedicated DC-DC converter, which can be switching or linear depending on the application, that scales down the battery voltage to the desired one. In the Pre/Post regulated approach, the initial
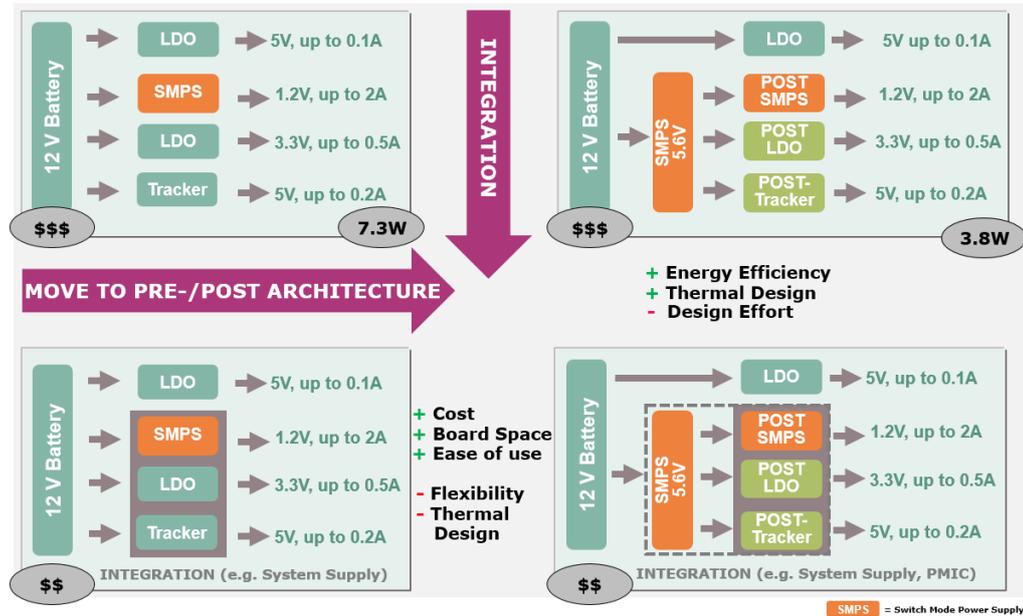
Figure 1.1: Trends in the automotive market (image courtesy of Infineon Technologies).

battery voltage is first scaled by what is called a pre-regulator to an intermediate voltage, and that voltage is the supply of successive regulators, called post-regulators, that will provide all the different supplies needed by the circuits. While complicating the design, the shift towards Pre/Post architecture provides two critical advantages. Firstly, the energy efficiency of the system is increased, and secondly it simplifies the thermal design, since the circuits at the different voltage domains are separated, simplifying the thermal isolation between them. A summary of the two described trends with the advantages and disadvantages of each trend is presented in Fig. 1.1. As it is shown in the figure, in an integrated Pre/Post architecture (in the bottom-right corner of the picture), the DC-DC converters in the post-regulated domain (inside the gray box) are supplied by the pre-regulator that converts the battery voltage from 12 to 5.6 V. The intermediate voltage then supplies the post-regulators which, in turn, generate the desired supplies for all the other circuits like RADARs, LIDARs, CPUs etc. The DC-DC converter proposed in this work is a switching DC-DC in the post-regulated domain. Therefore, its input voltage should range between 2.5 to around 5 V, its output voltage should be around 1-2 V with a maximum output current of 2 A.

(a)

(b)

(c)
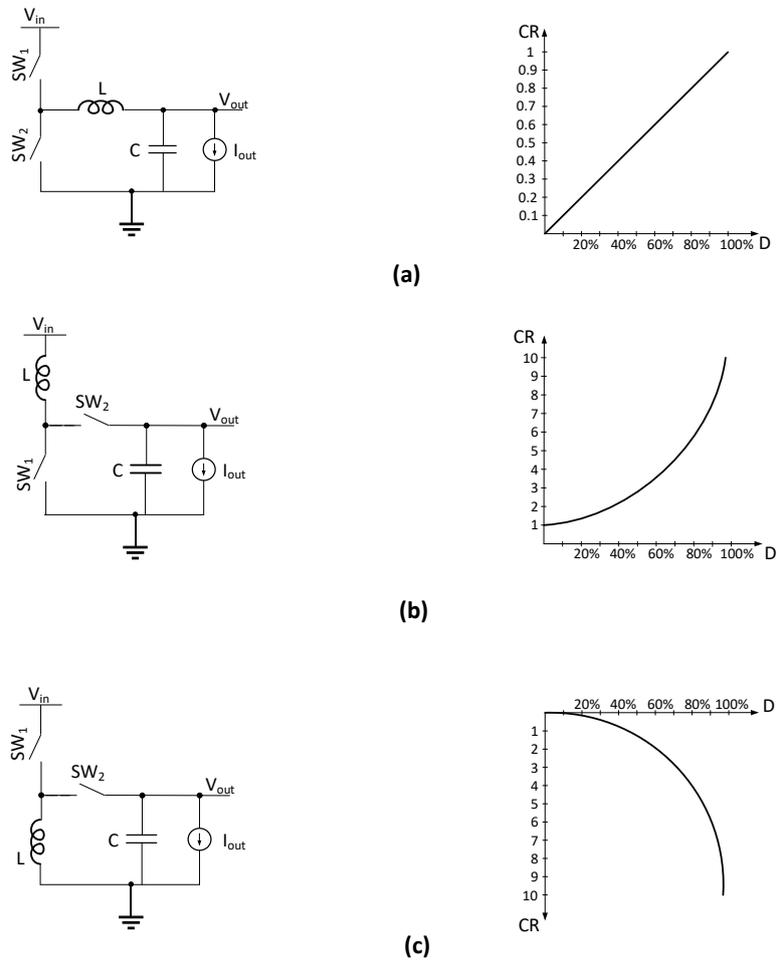
Figure 1.2: Schematics and conversion ratios of: (a) buck converter, (b) boost converter, (c) buck-boost converter.

1.2 High Frequency DC-DC Converters

1.2.1 DC-DC Introduction

Switching Mode DC-DC Converters (from now on simply referred as "DC-DC converters") are circuits that, given an input DC voltage, can convert that voltage to a different DC output through the charging and discharging of an inductor and a capacitor. Depending on the topology, the number of
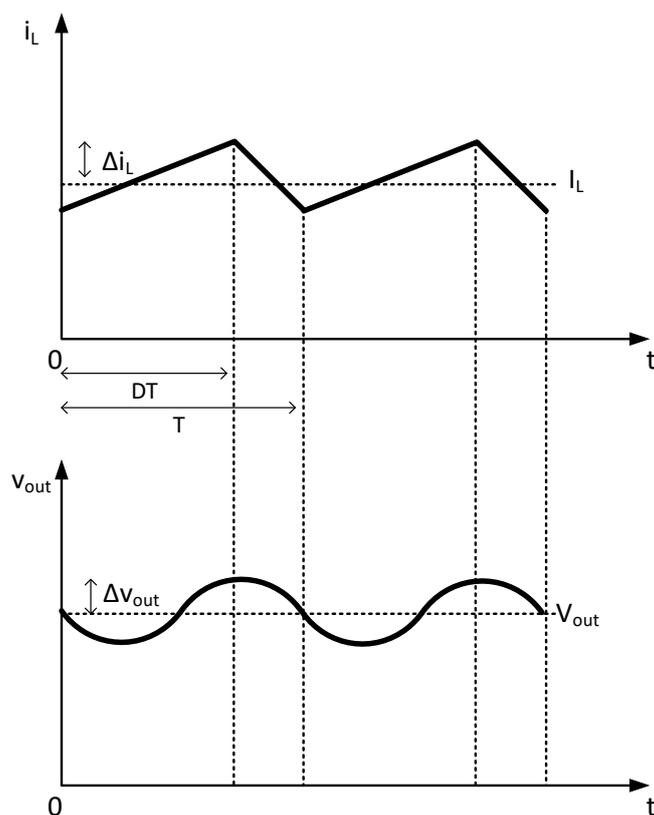
Figure 1.3: Output voltage and current of a buck converter.

components needed changes and the output voltage can be higher or lower than the input, with the same or opposite polarity. Fig. 1.2 shows the three most common topologies of DC-DC converters on the left side. The three converters shown are: the buck converter (a), the boost converter (b) and the buck-boost converter(c). The following analysis will focus on the buck converter, which is the topology proposed in this work. In Fig.1.2 (a), the two switches SW_1 and SW_2 are controlled by two opposite square waves that alternatively open and close them to charge and discharge the intermediate node. When SW_1 is open and SW_2 is closed, the intermediate node is shorted to V_{in} and the current through the inductor will increase, and when SW_1 is closed and SW_2 is open,

the intermediate node will be shorted to ground and the current through the inductor will decrease. The LC network at the output is filtering the square wave between ground V_{in} on the intermediate node, hence is extracting the average output voltage V_{out}. The output voltage can be calculated by applying the voltage balance principle to the inductor and the charge balance principle to the capacitor [1], and is equal to:

$$V_{out} = DV_{in} \tag{1.1}$$

Where V_{out} and V_{in} are the output and input voltages, respectively, and D is the duty cycle of the switches. Since D is inherently between 0 and 1, The output voltage of a buck converter is always lower than its input voltage. The Conversion Ratio (CR) of a DC-DC converter is defined as V_{out}/V_{in}. The graphs of the CR of the buck, boost and buck-boost converter versus the duty cycle D are drawn in the right side of Fig. 1.2.

With analogous procedure, the relationship between the input and output currents, I_{in} and I_{out}, is:

$$I_{out} = \frac{1}{D} \cdot I_{in} \tag{1.2}$$

It is worth noticing that in a buck converter, the DC output current I_{out} coincides with the inductor current I_L.

Given the switching nature of the circuit, the actual waveforms for the inductor current and capacitor voltage will not be continuous, but will have some ripple.

Fig. 1.3 shows sketches of the output voltage and inductor current of a generic buck converter. The ripple on the inductor current is equal to:

$$\Delta_{i_l} = \frac{V_{out}(1 - D)}{I_{out} \cdot f_s \cdot L} \tag{1.3}$$

Where f_s is the switching frequency. From the equation it can be seen that the current ripple is inversely proportional to both the inductance value and the switching frequency. Therefore it is theoretically possible to increase the switching frequency and at the same time reduce the inductance to achieve the same ripple. The same reasoning can be done for the voltage ripple on the output and the value of the capacitance. DC-DC converters are very expensive and bulky, and this is usually because of the presence of the inductor, which by itself occupies more area and can cost more than the entire chip. Reducing the value of the inductance opens the possibility for the integration of the inductor, which could possibly be integrated either on chip or in package, thus saving a lot of area and cost to the manufacturer.
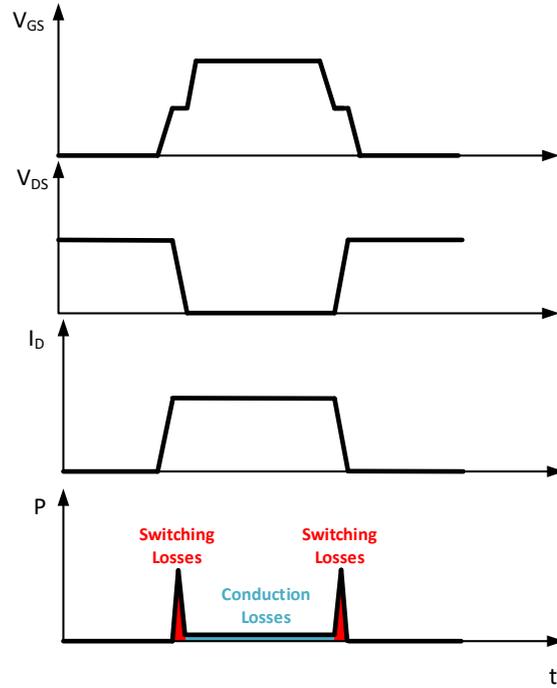
Figure 1.4: Simplified diagrams of conduction and switching losses in a MOS transistor.

1.2.2   Efficiency and Power Losses

When dealing with power converters, efficiency is a key parameter, as higher efficiency translates in less power wasted, and, in the specific case of automotive applications, in less CO_2 emissions. Given the worldwide push to reduce CO_2 emissions in cars (among other products), it is obvious that car manufacturers require electronic components with high efficiency.

Efficiency is defined as:

$$\eta = avg \left(\frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \right) \cdot 100 \tag{1.4}$$

By substituting V_{out} with $D \cdot V_{in}$ and I_{in} with $D \cdot I_{out}$, every term of eq. 1.4 would simplify to unity, leading to an efficiency equal to 100% . This theoretical value of efficiency shows the main advantage of switching DC-DC converters

over linear regulators, that have intrinsic losses even in ideal scenarios. Obviously, this would be true only if every component was ideal, but in reality the transistors acting as switches as well as the inductor and capacitor all have their parasitic resistances and capacitances that put a limit to the maximum efficiency achievable. In particular, considering MOS transistors, three are the main types of losses that decrease the efficiency of the converter: conduction losses, switching losses, and driving losses.

Conduction losses are due to the on-resistance of the transistor and are equal to:

$$P_{cond} = R_{DSON} \cdot I_D^2 \tag{1.5}$$

Where R_{DSON} is the drain-source resistance of the transistor when it is in it its on-state, and I_D is its drain current (RMS value). Conduction losses cause a non-zero voltage drop across the drain-source terminal of the transistors, requiring a higher duty cycle to achieve the same output voltage, hence lowering the efficiency. It is clear from 1.5 that conduction losses are dominant at high currents, and that they can be minimized by lowering R_{DSON}, which usually means maximizing the width of the transistors. It is worth mentioning that the inductor's Equivalent Series Resistance (ESR) causes an increase in conduction losses as well, as it is in series with the R_{DSON} of the switches.

Switching (or dynamic) losses are caused by the finite turn-on and turn-off times of the transistors. Supposing that the MOSFET is initially in its OFF state, its gate-source voltage V_{GS} is low, its drain-source voltage V_{DS} is high and no drain current flows. When a V_{GS} is applied the drain current I_D starts to flow, but the V_{DS} does not commute before the V_{GS} reaches the Miller Plateau [1]. during this time, V_{DS} and the I_D are simultaneously different from zero, causing the consumed power $P = V \cdot I$ to be also different from zero. The same princilple applies during the turn-off of the transistor, and the total switching power loss equal to:

$$P_{sw} = (W_{ON} + W_{OFF}) \cdot f_s \tag{1.6}$$

Where W_{ON} and W_{OFF} are the turn-on and turn-off energy, respectively. From 1.6 it is clear that increasing the switching frequency f_s has a negative impact on the switching losses. Fig. 1.4 visualizes these two contributions to the power loss, along with the relevant (simplified) waveforms of the MOSFET. In the picture, the total the conduction power loss during the on-state of the MOSFET is in blue and the switching power losses are in red.

The last contribution to the degradation of the efficiency comes from the driving losses. With driving losses is intended the power that is needed to turn

on the transistor. Driving losses are defined with the equation:

$$P_{drv} = \frac{1}{2} \cdot C_G \cdot V^2 \cdot f_s \tag{1.7}$$

where C_G is the gate capacitance. Minimizing the width of the transistor reduces the driving losses, but, as mentioned before, conduction losses are increased with decreasing width. The optimal sizing of the power MOSFETs is calculated keeping all these loss contributions into account.

Another important cause of efficiency loss, and potential cause of device failure, comes from the cross-conduction currents. For example, looking at the buck converter in Fig. 1.2 (a), it can happen that SW_1 (high side) and SW_2 (low side) are both closed at the same time. This is again due to the finite turn-on and turn-off times of the MOSFETs used for the switching. When both switches are closed, a high current flows directly from V_{in} to ground, and this current is all current lost that incides on the efficiency and, if its value is too high, can potentially damage the devices. To avoid cross-conduction, a dead-time circuit has to be added to the control of the switches.

1.3 Control Loops

A DC-DC converter can not work with just one fixed duty cycle: variations in the battery voltage (line transients), load current (load transients) and other external disturbances can compromise the DC conversion. Typical examples in the automotive field are the battery cold crank, which is a drop in the battery voltage caused by the cranking of the engine at cold temperatures, and the load dump, which is a quick release of the load that causes the output voltage to increase. In cases like these, the duty cycle needs to be quickly adjusted in order to maintain the output voltage as constant as possible even when these variations occur. A control feedback loop must be added to the power stage to ensure line and load transient regulation.

1.3.1 Most Common Topologies

Fig. 1.5 shows the three basic topologies used for the control loops of DC-DC converters, applied to a boost power stage. In the Voltage Control Mode (VCM) loop, Fig. 1.5(a), the output voltage V_{out} is first scaled down by the two resistors, R_1 and R_2, and then subtracted from a fixed reference voltage (also referred to as set point), V_{ref}, by means of an error amplifier. The output of the error amplifier, V_{err}, is then compared with a sawtooth waveform signal. The result at the output of the voltage comparator is a pulse-width
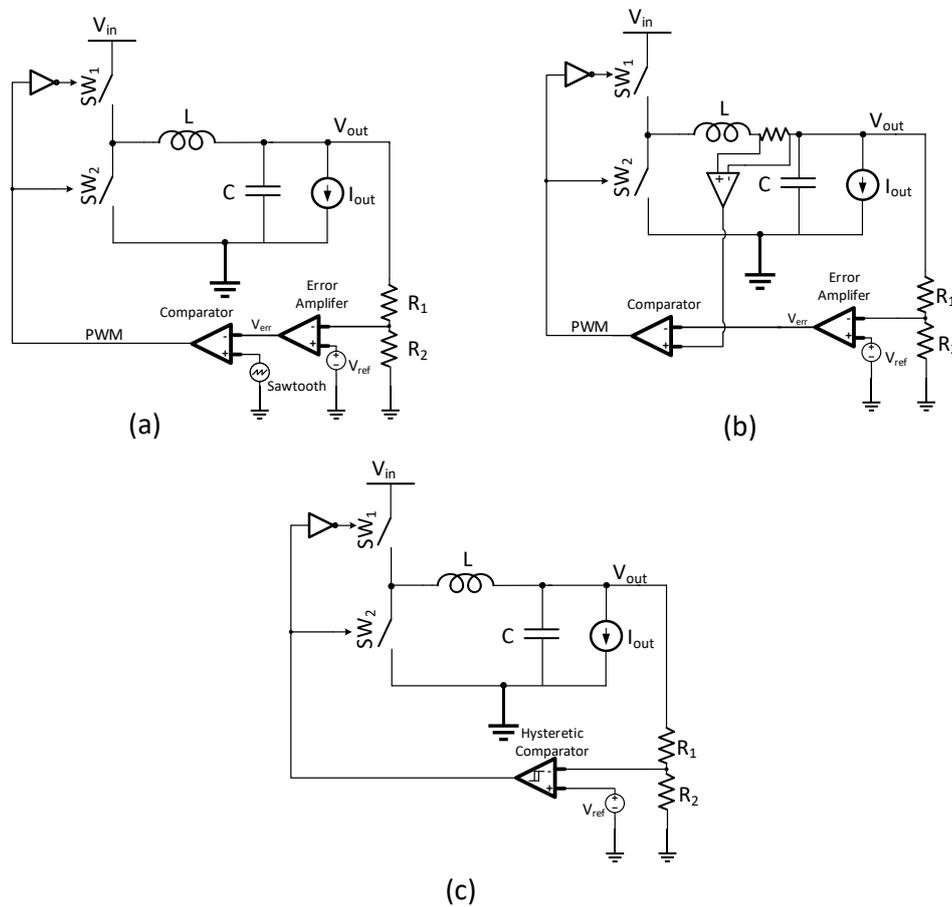
Figure 1.5: Schematic diagrams of a) VCM, b) CCM, c) HCM applied to a buck converter.

modulated (PWM) waveform, i.e. a square wave with varying duty cycle, depending on the error signal, V_{err}. This PWM wave dynamically controls the duty cycle of the switches. Suppose that V_{out} is decreasing from the desired value. The error amplifier subtracts the scaled down output from the reference, making V_{err} increasing. This results in a higher duty cycle when it is compared with the sawtooth. Higher duty cycle means an increase in V_{out}: the process continues until the output voltage reaches back the desired value. It is important to underline that the sawtooth generator has a frequency equal to

the switching frequency of the converter: therefore, the VCM technique works at a fixed frequency. The Current Controlled Mode loop (CCM), Fig.1.5(b), is obtained by replacing the sawtooth signal with the sensed inductor current signal, [2]. It can achieve faster responses with respect to what achieved by VCM as it implements two feedback loops, but suffers from sub-harmonic resonance and thus needs a compensation ramp to be added to the sensed inductor current, [3]. Hysteretic Control Mode (HCM) loop, Fig. 1.5(c), is the fastest of the three techniques. The scaled-down output voltage is directly the input to a comparator with some hysteresis. The output of the comparator is the square wave that directly controls the switches. HCM can achieve excellent dynamic characteristics since typically does not need feedback loop compensation circuits, [2]. Notice that HCM does not work at a fixed frequency, so a design challenge is not to let the HCM increases the switching frequency too much. It also requires the ripple to be high in order to properly complete the sensing operation, so either the capacitor must have a high ESR or the ripple needs some gain or enhancement techniques, [4]. Other variable frequency control techniques include constant-on-time or constant-off-time control, [5].

In automotive applications, due to the typically very strict noise requirements, fixed frequency controls are usually preferred over the variable ones: the switching activity of a DC-DC converter is introducing noise in the system at the switching frequency, and this noise can interfere with the other devices. If the switching frequency is fixed, so is the frequency of the injected noise, otherwise it is harder to predict the noise frequency, resulting in even more strict requirements of the noise mask. Shifting the switching frequency from the typical 1-2 MHz to higher values has the added advantage of shifting the switching noise frequency towards values that do not interfere with other circuits. The obvious trade-off is the complication in the design of the control loop: since a high frequency loop requires extremely fast blocks, such as a high bandwidth Error Amplifier and a comparator with minimum delay.

1.3.2 Stability and Frequency Compensation

The circuits shown in the previous paragraph are not enough to build a stable control loop. Fig. 3.16 (a) shows the Bode plot of the gain of the power stage of a buck converter in open loop. The inductor an capacitor resonance causes a double pole at the resonant frequency F_{LC}, which is the reason for a gain decrease with - 40 dB -over-decade slope, and a 180°phase shift. From the graph, it is evident that the buck converter by itself is inherently unstable, as the gain crosses the zero dB axes with 0° of phase margin. At a higher frequency, an additional zero is present caused by the ESR of the capacitor.
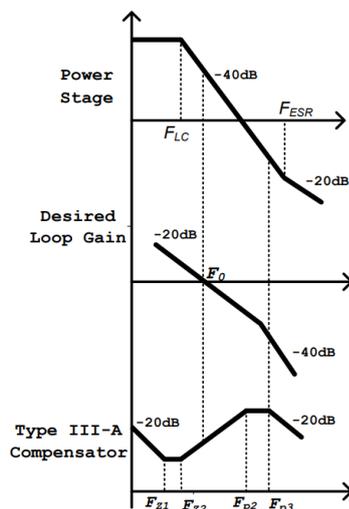
Figure 1.6: Bode plots of a)Power Stage b)Loop Gain c) Compensator [6].

To achieve the desired loop gain that is shown in Fig. 3.16 (b), it is necessary to compensate the effect of the poles and zero of the power stage, and to do so, an RC compensation network is added to the Error Amplifier in the loop. Depending on the cases, the number of desired poles and zeroes in the compensator changes, and so does the number of resistors and capacitors needed. Based on how many poles and zeroes are needed, the compensators are divided in three categories called type I, II and III [6]. The case shown in Fig. 3.16 (c) is a Type III compensator. This compensator implements two zeroes close to F_{LC} to cancel the effect of the double pole, one pole in the origin to have the slope of -20 dB-per-decade and two poles at higher frequencies to cancel the effect of the ESR zero. The F_0 of the loop is typically set to one tenth of the switching frequency, to ensure that the switching noise will be attenuated, being at a frequency at least one decade after the zero-crossing. Another advantage of going to higher frequencies is that since the switching frequency is higher, the bandwidth of the loop can be higher too, allowing for faster transient responses. The details of the calculations for the compensation network in this work will be shown later on.

Chapter 2

Stacked Power Stage Circuit

The first step in the design of a DC-DC converter is the design of the power stage in open loop: starting from the correct selection of the MOSFETs available in the technology that can sustain the required levels of voltage and current in the post-regulated domain, to the correct sizing in order to have a sufficient efficiency. In this chapter a summary of previous art of high frequency power stages is provided, then details on the choice and design of the power stage are given, closing with some simulation results.

2.1 Circuit Description

2.1.1 Previous Art

The most common configuration for an integrated buck DC-DC converter power stage uses a PMOS as high-side switch, and an NMOS as low-side switch, both driven with a tapered chain of inverters. This structure is simple, well known, and has a high efficiency, therefore it is widely used, [7], [8]. However, the simple buck power stage has an intrinsic limitation: the maximum input voltage that it can sustain is equal to the maximum drain-to-source voltage (V_{DS}) of the transistor allowed by the technology. If the application requires an input voltage which is higher than the maximum V_{DS}, there are two possible solutions: either use transistors from a different technology that allows a higher voltage, or stack multiple "low voltage" transistors. By stacking two PMOS and two NMOS transistors the maximum V_{in} rises to $2V_{DS}$, assuming that the two transistors are equal in terms of maximum V_{DS}. A number of stacked structures or high frequency buck converters has been studied in literature. The research in [9] shows an example of this technique: by stacking
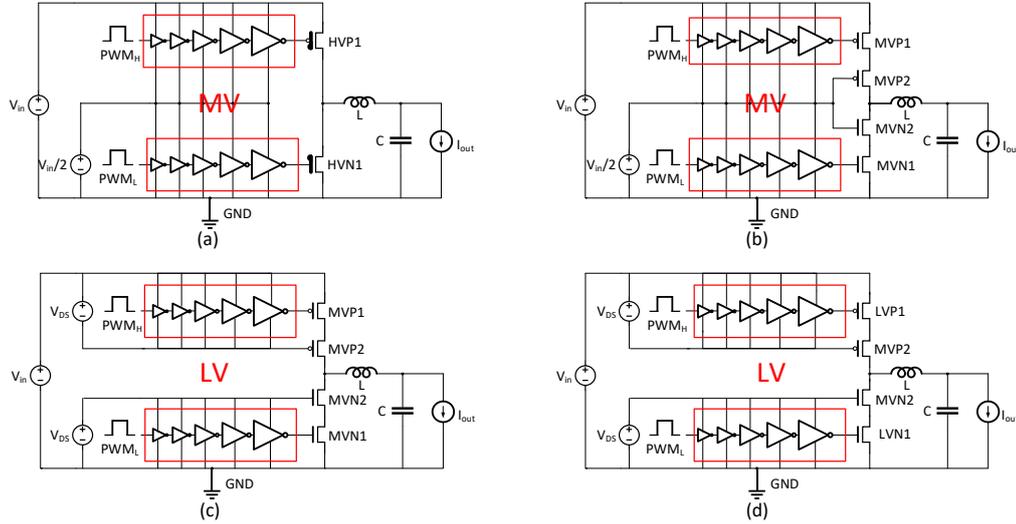
Figure 2.1: Four proposed schematics: (a) HV, (b) MV, (c) MV with LV driving, (d) Hybrid LV+MV.

two 180-nm transistors higher input voltages are allowed, and a high efficiency (88%) is still reached with I_{load} = 250 mA. The work presented in [10] brings this configuration even further stacking three low voltage transistors (40-nm with maximum V_{DS} around 1 V) to sustain 3.3 V of input voltage with very high efficiency (97 %) when the load current is 150 mA. The circuit in [11] uses a 45-nm technology to achieve a peak efficiency of 87.8% with a very high switching frequency equal to 240 MHz and I_{load} = 250 mA. However, the particular dead time architecture proposed requires both positive and negative inductor current to properly work. All these solutions achieve high efficiencies with high switching frequency, but with output currents in the range of only few hundreds of mA. For automotive post-regulated applications, the output current is typically much larger, up to 1∼2 A which is another challenging specification for the design. This chapter studies different configurations and technologies for a power stage switching at 100 MHz with an output current equal to 1 A and V_{in} up to more than 4 V.

2.1.2 Technology

The technology for high voltage automotive applications available for this work features several MOS transistors, each with different minimum sizes, maximum

V$_{DS}$ sustainable, threshold voltage, and capacitance. The transistors involved in this study are three: a "high voltage" (HV) MOS with minimum channel length of approximately 1 μm, a "medium voltage" (MV) MOS with minimum channel length of approximately 400 nm, and a "low voltage" (LV) MOS with minimum channel length of approximately 120 nm. The maximum V$_{DS}$ sustainable is, obviously, higher for the HV MOS, intermediate for the MV MOS and lower for the LV MOS. The purpose of this study is to verify which device and which topology works best as a power stage. The correct choice of transistor types and dimensions for the drivers also counts for an optimal efficiency.

2.1.3 Power MOSFETs and Drivers Design

Fig. 2.1 shows the four schematics designed and compared in this chapter. The circuit in Fig. 2.1 (a) uses the HV MOSFETs as power stage and the MV MOS in the driver. The chains are supplied at V$_{in}/2$, since the MV MOS-FETs cannot sustain the full range of V$_{in}$. The HV MOSFETs can sustain any V$_{in}$ in the desired range, but the length and the large gate capacitance of the HV MOSFETs cause an increase of both switching and conduction losses, decreasing the overall power efficiency. The use of HV transistors can be avoided by building the power stage with two MV MOSFETs stacked, as shown in Fig. 2.1(b). This circuit can still sustain any V$_{in}$ in the desired range, and the MV devices are more performing at high frequencies, thanks to their reduced dimension and capacitance. Without changing the MV power stage, if the low-side and high-side chains are designed with LV transistors instead of MV, as shown in Fig. 2.1(c), another slight improvement in the efficiency could be obtained. Notice that, unlike the previous two circuits, in the circuit in Fig. 2.1(c) the low supply of the high-side chain and the high supply of the low-side chain cannot be both set as V$_{in}/2$, but have to be set to a lower value to avoid the breakdown of the LV drivers. The fourth and last circuit is shown in Fig. 2.1(d). For this circuit, a hybrid solution for the power stage has been studied, cascading a LV and a MV transistor. LV MOSFETs are used for switching, while MV are used as cascode. Given the reduced channel length of the LV MOS which makes them more suited for high frequency switching, the efficiency is expected to rise, while the MV cascode protects the LV MOS, ensuring high voltage operation. The drawback of this solution is the maximum sustainable V$_{in}$, now limited to 4 V (V$_{ds}$(LV) + V$_{ds}$(MV)). To minimize the losses, in all the designs, the channel length of the MOSFETs has been kept to the minimum value. Since the maximum load current required is 2 A, the channel widths of the power stages have been optimized for $I_{out} = 1$ A (half
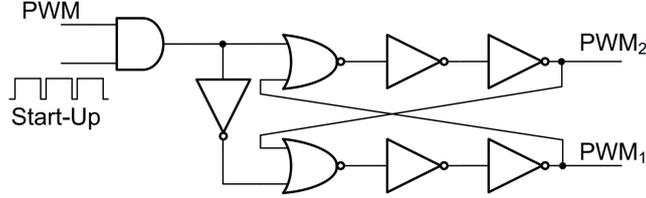
Figure 2.2: Dead-time and Start-up.

the maximum value, assuming that the converters will rarely have to work at maximum load condition). Regarding the drivers, tapered chains of five inverters are used in all schematics. the widths of the inverters in the drivers have been calculated with the taper formula:

$$W_{n-1} = W_n \frac{(b+1)^{n-1}}{a^n} \tag{2.1}$$

In (2.1), a is the taper factor, b is the W_P/W_N ratio, n is the number of each inverter. As shown in Fig. 2.1, for all the power stages, chains of five inverters have been used for high and low side driving.

2.2 Simulation Results

The considered four schematics have been simulated to compare their efficiency. For all the schematics in Fig. 2.1 the value of the inductance is 60 nH and the load capacitance is equal to 10 nF. Parasitic ESRs of the inductor and capacitor are included in the schematics, equal for all the four configurations.The power efficiency has been simulated for I_{out} ranging from 0 to 2 A, which is the common range in these applications. For this preliminary stage, an ideal voltage mode control [1] (VCM) loop has been designed, to keep the output voltage of all the four schematics fixed at 1.8 V for the efficiency evaluation, while V_{in} is 3.6 V for this comparison. A traditional dead-time generation circuit of around 300 ps plus a start-up (shown in Fig.2.2) has been added to the loop to avoid cross-conduction currents in the power stages.

Fig. 2.3 shows the resulting simulated power efficiency of the four schematics. As anticipated in the previous section, the lowest efficiency is obtained with the HV power stage (blue curve), that reaches a peak value of 72%. The efficiency improvement is significant with the two-stacked MV power stage (orange curve), peaking at 79%. Changing the low-side and high-side chains from MV to LV provides another slight boost in the efficiency (gray curve): from
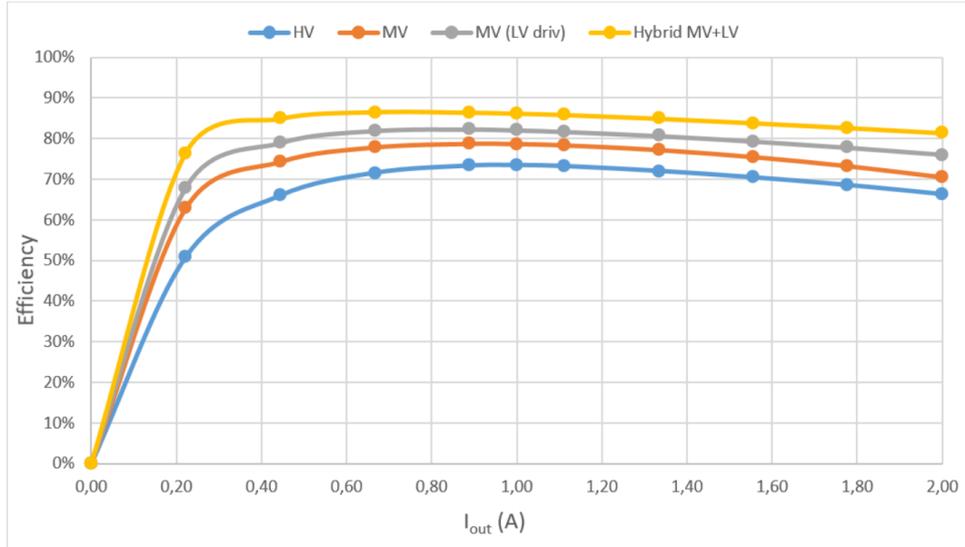
Figure 2.3: Simulated power stages efficiency as a function of the load current.

79% to 82%. The highest efficiency is achieved with the hybrid LV+MV power stage (yellow curve) that reaches a peak efficiency of 86%. Fig. 2.4 shows the drain voltages of the switching transistors in the MV power stage configuration (MVP1 and MVN1 in Fig. 2.1(c)): thanks to the stacked configuration, the V_{DS} of the transistors stays within the breakdown limit. Also in the hybrid configuration, the V_{DS} of the LV switching transistors is below the maximum limit, thanks to the stacked MV MOSFETs (Fig. 2.5).

Table 2.1 summarizes the results comparing the simulated peak efficiencies and the maximum input voltages. A rough estimation of the area consumption of each power stage is calculated and added to the table in percentage terms, showing that the hybrid configuration (used as reference for the percentages calculation) is not only the best in terms of peak efficiency, but also in area consumption, while the two MV solutions are the bulkiest. Notice that this is just a rough estimation to have an idea of area comparison between the four circuits. Among the four solutions, the hybrid power stage has been chosen for further development, thanks to the high efficiency improvement provided by the LV+MV configuration.

A comparison of the proposed hybrid LV+MV solution and the previously discussed state of the art circuits is summarized in Table 2.2, showing that the proposed solution is still competitive in terms of efficiency, while implementing longer transistors and operating with much higher output currents, with the
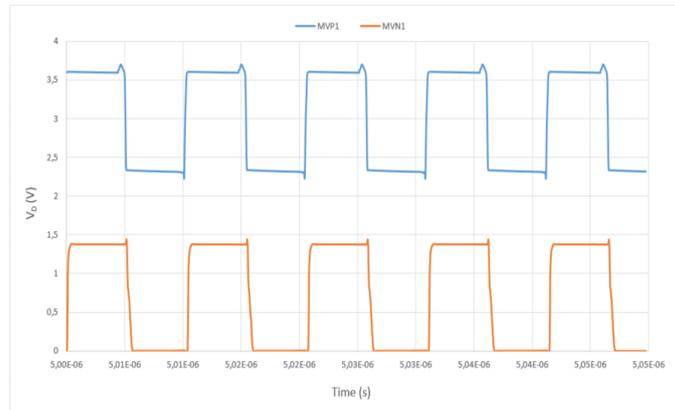
Figure 2.4: Simulated drain voltages (V_D) of the MV power stage.

additional advantage of a slightly higher maximum input voltage.

Since 100 MHz is a very high switching frequency for a buck converter with these specifications, a good compromise between efficiency, area, and possible time-to-market could be to lower the switching frequency to some tens of MHz. Doing so, the efficiency would rise, and the area of the power stage would decrease, at the expense of a larger inductor, but it would still be smaller than the ones needed in the conventional 1-2 MHz converters. Fig. 2.6 shows the simulated power efficiency of the four power stages as a function of the switching frequency. The load current, for all circuits, is set to 1 A. From Fig. 2.6, it is clear that the frequency range with the highest efficiency
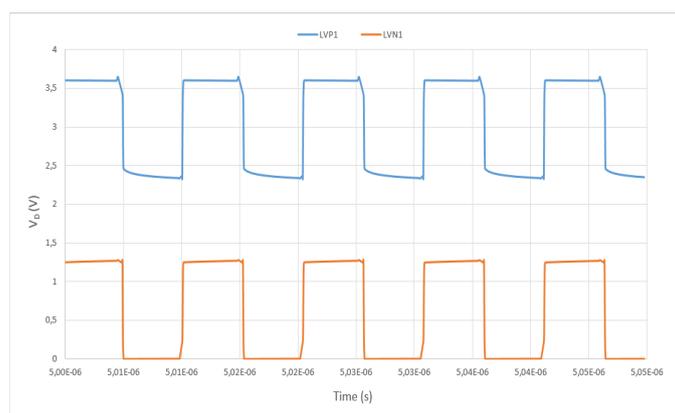
Figure 2.5: Simulated drain voltages (V_D) of the hybrid power stage.

	HV	MV	MV(LV driv)	Hybrid LV+MV
Technology [μm]	1	0.4	0.4+0.12	0.12+0.4
Peak Efficiency	72%	79%	81%	86%
Area Estimation	118%	239%	205%	100%

Table 2.1: Performance summary and comparison of the proposed power stages.

	[9]	[10]	[11]	Hybrid
Technology [μm]	0.18	0.04	0.045	0.12+0.4
Max. V_{in} [V]	3.6	3.6	$\sim$3.6	4
Peak Efficiency	87.8%	91%(meas.)	87.8%	86%
Switching Frequency [MHz]	97	100	240	100
Load current [mA]	250	150	150	1000

Table 2.2: Performance comparison with previous art.

is in the range 30-60 MHz, reaching 89.7% for the LV+MV schematic, which proves to be better than the other three in all the frequency sweep. Above 60 MHz, the switching losses increase too much, degrading the efficiency. On the other side, conduction losses are the cause for the efficiency drop at lower frequencies. Notice that the sizes of the transistors were optimized to maximize the efficiency in the 100 MHz condition, so the power efficiency is expected rise even further by re-optimizing the widths of both the power stages and the inverter chains for lower frequencies.

2.3 Internal Bias Voltages Generation

The previous simulations were conducted using ideal voltage generators for the two internal rails both supplying the high and low side drivers, and biasing the stacked transistors. When using ideal generators, which are able to source and sink an infinite amount of current instantly, those two voltages are perfectly regulated and constant in time. In reality, when the voltage generation is not ideal, the high switching frequency and high current in the power MOSFETs cause periodic variations in the two voltage rails. These variations both cause a drop in the efficiency, and risk to damage the transistors in the drivers, if
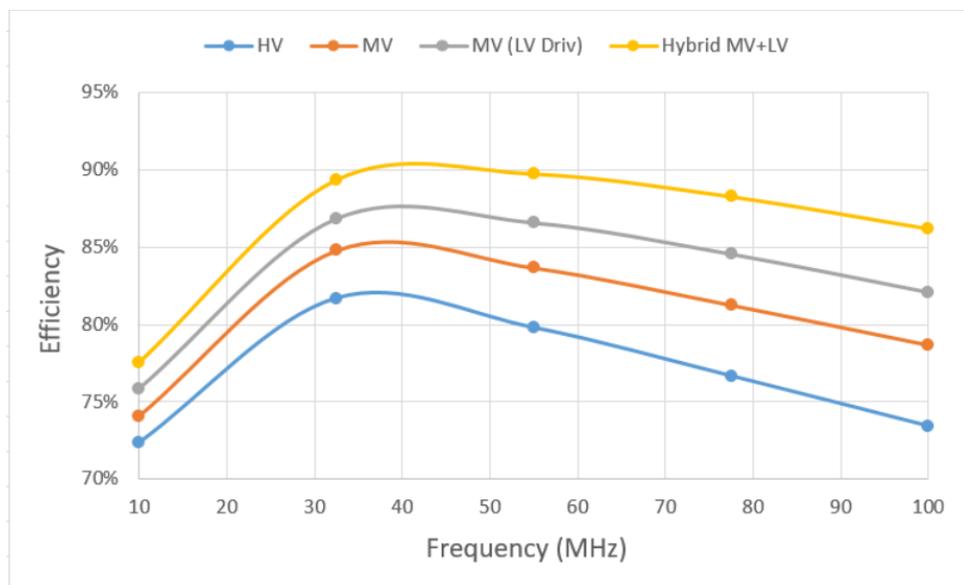
Figure 2.6: Simulated power stages efficiency as a function of the switching frequency.

their maximum V_{DS} is exceeded. The real voltage generator circuit is shown in Fig. 2.7. The two voltages are obtained with a stack of two diodes per rail (two PMOS D_1, D_2 for the high side and NMOS D_3, D_4 for the low side) with the bias resistor R in the middle. In order to smooth the mentioned jumps in the voltage rails, capacitors C_1 and C_2 need to be added, and their capacitance should be as high as possible. In this design, 300 pF of capacitance for each side have been integrated.

2.4 Parasitic Bonding Inductance

Another unwanted effect that severely threatens the functioning and performance of the power stage is the effect of the parasitic inductance of the bondings on the supply and ground voltages. The inductive effect of the bonding causes the supply and ground voltages to ring. This ringing can cause the supply-to-ground differential voltage $V_{in} - V_{ss}$ to reach values as high as 7.5 V. This voltage difference falls on the V_{DS} of the stacked transistors in the power stage, as well as on the drivers, risking to compromise the functionality of the system. To attenuate the ringing, two possible solutions are possible: increase the number of bondwires put in parallel on the same pin to reduce
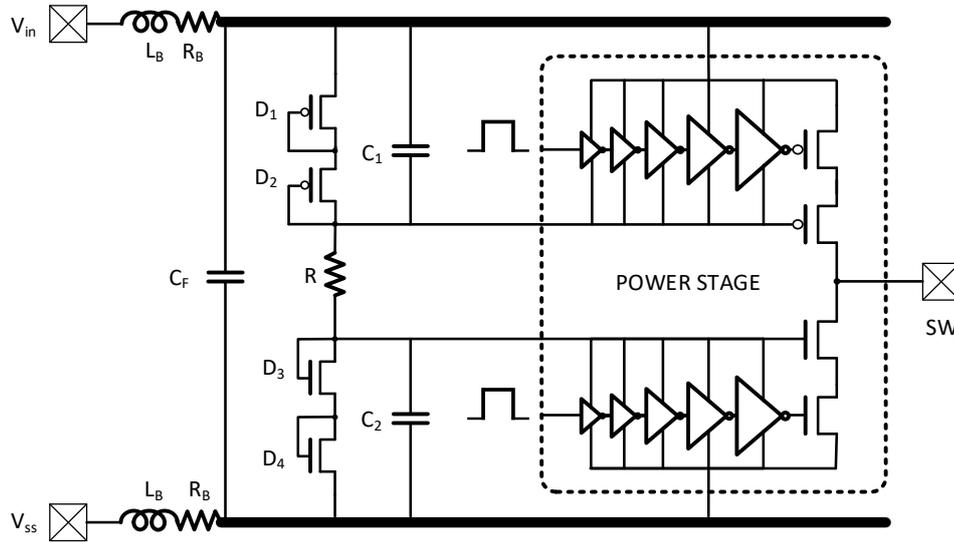
Figure 2.7: Internal bias generation circuit.

the equivalent parasitic inductance, and integrate high capacitance between the supply voltage and the power ground to filter the spikes. Fig. 2.7 adds the parasitic bonding inductance an resistance L_B and R_B to the schematic of the power stage, and Fig. 2.8 shows the effect of a filter capacitance of 500 pF on $V_{in} - V_{ss}$ and on the switching voltage. This simulation assumed 500 pH of parasitic bonding inductance on both pins, a value that was estimated considering triple bondings on V_{in} and V_{ss} and an average length of the bondwires of 1 mm ($25\mu m$ diameter gold bondwires). The simulations show that such a high value of capacitance is needed to keep the voltage in a reasonable range and prevent the breakdown of the power stage. It is worth mentioning that this issue could be resolved at the root by using a bondless package, which would most likely be the case for a potential product, but, for the sake of this research, the package choice is limited to bonded packages. The simulated efficiency with real voltage generators and considering the parasitic bonding inductance is shown in Fig. 2.9.
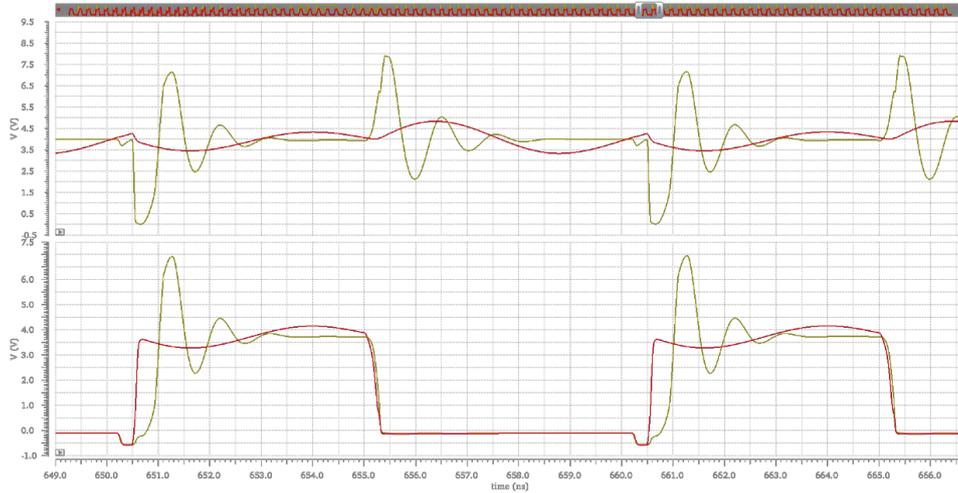
Figure 2.8: Inductance effect on $V_{in} - V_{ss}$ and the switching node: without filter capacitance (yellow), with 500 pF of filter capacitance (red).
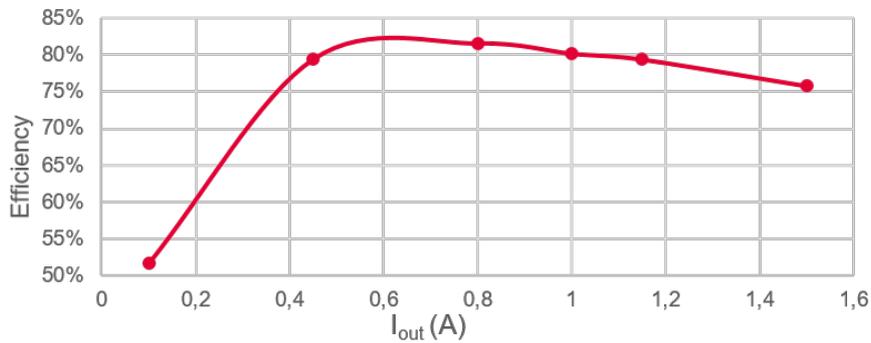
Figure 2.9: Simulated power efficiency with parasitics and real voltage generators.

2.5 Power Stage Layout

For this project, two slightly different versions of the power stage are proposed. The two versions differ only in their layout, and are identical on the schematic level. Both power stages are implemented in the chip. Fig. 2.10 shows the layout blocks of the two power stages. The power on top has more dense fingers, while the one on the bottom has less density of fingers but more bulk contacts. The circuit for the internal voltages generation has to be duplicated
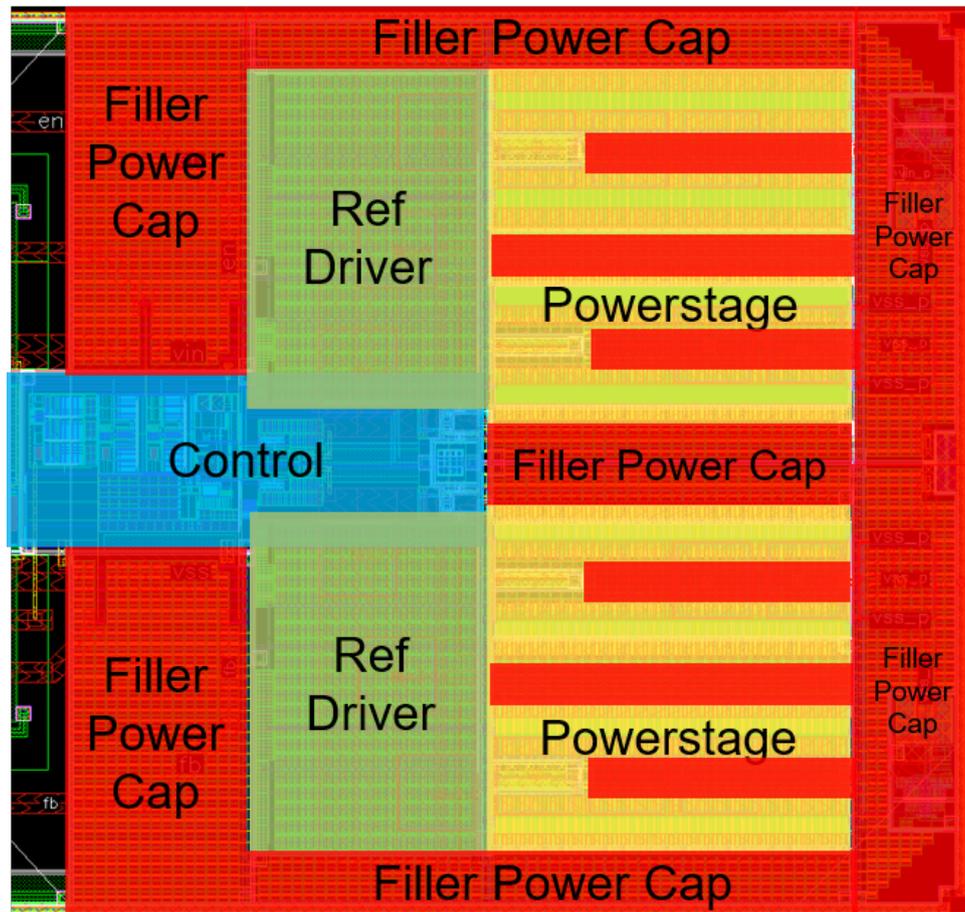
Figure 2.10: Layout of the two power stages.

for both powers, the two are indicated as "Ref Driver" in the figure. To reduce the current density, a wide layer of copper metal is needed on both powers, enlarging the area required for the power stage. Although the chip area was not a strict constraint in this project, in order to avoid wasting too much area, the empty layers below the copper metal were filled with capacitors connected between the power supply and power ground, to filter the inductive effect of the bondings described before. More capacitors have been added on the edges of the power stage (indicated as "Filler Cap" in Fig. 2.10) , to reach the desired value of at least 500 pF for each power stage. For the same reason, three pad openings are also placed on all power supply, power ground and
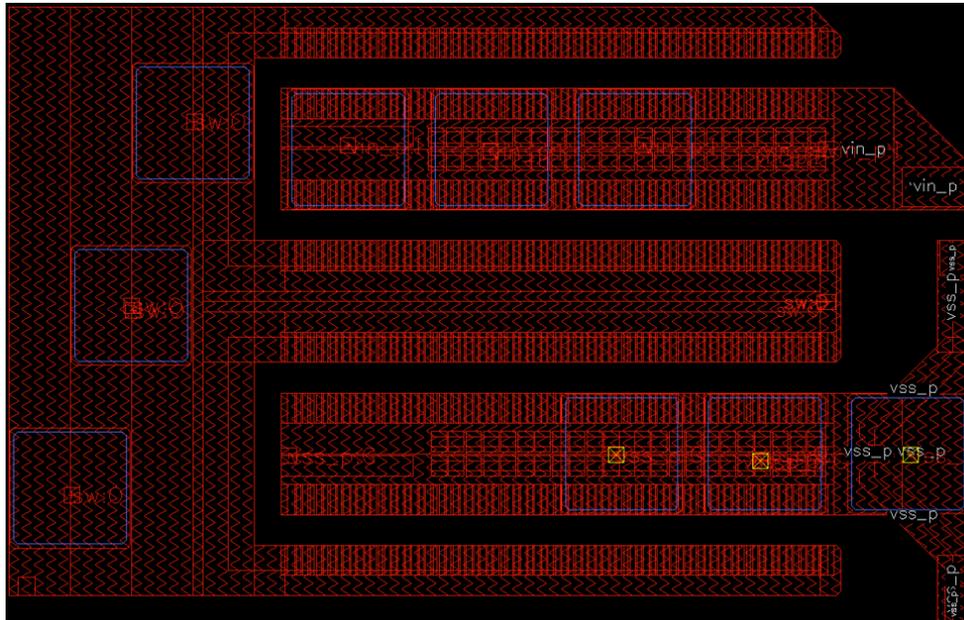
Figure 2.11: Copper layer detail for one power stage.

switching nodes to allow triple bonding on all of them (Fig. 2.11). In the next chapter, the control loop, indicated in Fig. 2.10 as "Control" is explained, and a complete concept block diagram of the chip comprehending the two power stages and control loop is provided.

Chapter 3

Control Loop Design

In this chapter, the control loops studied and designed for the discussed power stage are explained. After a brief review of the state of the art regarding high frequency control loops. two different control strategies are presented and compared with SIMPLIS simulations. After that, transistor level design is discussed.

3.1   Previous Art

As mentioned in previous sections, a lot of challenges come from the design of control loops at high frequencies. In literature, there are some examples of the design of high frequency loops. For example, [12] presents a very interesting multi-phase buck switching at 100 MHz and using the bondwire inductance as the main inductor. For that converter, a simple VCM control was chosen, discarding the hysteretic and current control for the extra challenges coming from the need for frequency synchronization (HCM) or a high bandwidth current sensor (current control).The work in [13] proposes a Constant-On-Time controlled buck at 10 MHz with dynamic biasing of the comparator to improve the efficiency. [8] introduces an innovative Voltage-to-Pulse converter for a buck switching at 60/120 MHz, and [14] proposes a Delay Locked Loop (DLL) to synchronize the frequency of a hysteretic-controlled buck switching from 25 to 70 MHz. Finally, [15] proposes the use of a One Cycle (OC) Controller applied to a DC-DC converter for RF applications.

For this project, two different control strategies have been designed and implemented on chip. Each of the two controls combines the functioning of two loops, and each control works at fixed frequency. The first control implements a One Cycle loop combined with an output VCM loop. The choice of the
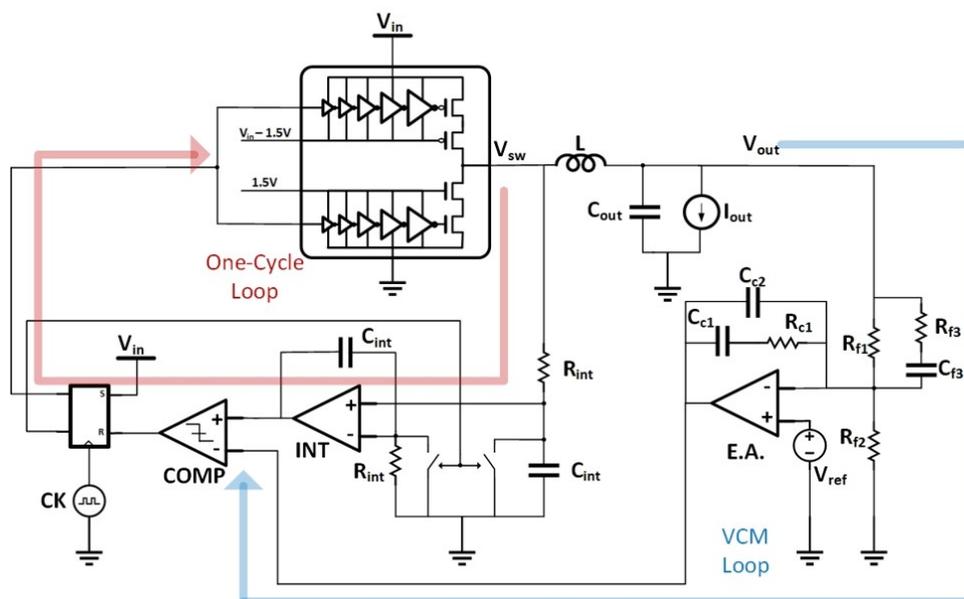
Figure 3.1: Schematic of the One Cycle + VCM loop.

One Cycle loop was made because of the interesting topology and potential advantages that can bring to the circuit. So far, very few examples of this kind of control loop at 100 MHz are found in literature, none of which appears to have reached the fabrication stage. The second control is implementing a more traditional Feed Forward (FF) loop, paired with the same VCM output loop of the first control. The choice of having two control strategies on the same chip was made in order to compare the performances of the two solutions, and to have both a more innovative and a more traditional solution on the same chip. The functioning of each of the control loops is explained next.

3.2   One Cycle Control

The circuit in Fig.3.1 shows a schematic representation of the hybrid stacked power stage described in the previous chapter, with the addition of a One Cycle control loop (following the red path) and the VCM output loop (following the blue path). The One Cycle loop integrates the voltage at the switching node V_{SW}, generating a ramp signal V_{INT}. In Fig.3.1 is shown a general, non-inverting integrator scheme, the actual design will be discussed later on. The ramp signal is then compared with a reference voltage. This reference
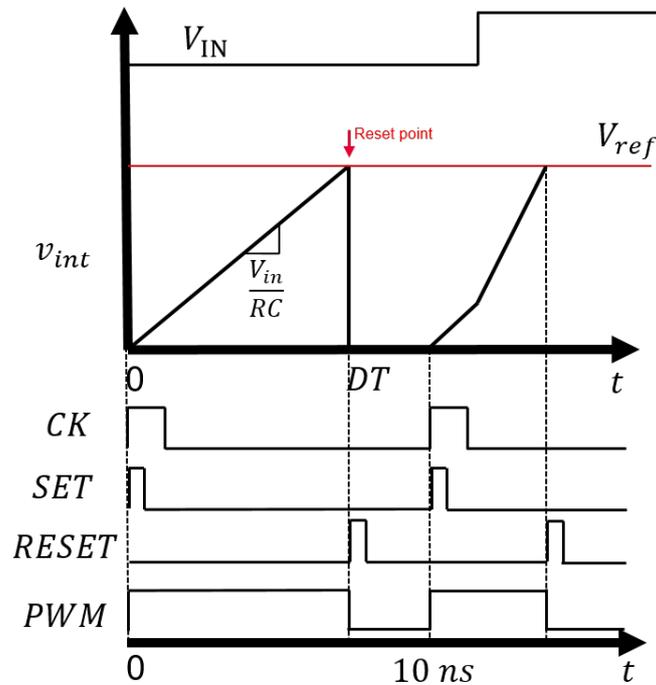
Figure 3.2: Working principle of a One Cycle loop.

voltage V_{ref} can be fixed or variable. When the integrated signal becomes greater than the reference, the comparator is triggered and sends a pulse to the set/reset (SR) flip-flop. The SR flip-flop is receiving a SET pulse on every clock cycle, while its RESET pulse is given by the output of the comparator, so the output of the flip-flop will be a PWM signal controlling the power stage. The inverted PWM signal will control two switches that will reset the integrator inputs [16]. Since the Flip-Flop is clocked at a fixed frequency (100 MHz in this case), the whole loop acts as a fixed-frequency control. Fig.3.2 shows the working principle of the One Cycle control that was just described. If, for example, the input voltage rises, the integration slope will be steeper, so it will reach the reference voltage (i.e. the reset point) faster, resulting in a lower duty cycle and regulating the output voltage. The opposite reasoning can be made for a drop in the input voltage, causing the slope to decrease its slope hence rising the duty cycle. Since the change in the integration slope is instantaneous, the regulation should be immediate in an ideal environment, resulting in a virtually perfect line transient response.

To obtain the output voltage V_{out} it must be reminded that it equals the average value of the switching voltage v_{sw}, and that V_{sw} is equal, ideally, to V_{IN} for the time time that the high side is on (D). The relationship then becomes:

$$V_{out} = avg(v_{sw}) = \frac{1}{T} \int_0^{DT} v_{in} \, dx \qquad (3.1)$$

Assuming for now the reference to be a constant voltage and considering the RC slope of the integration, the value of V_{sw} can be set through the following equation:

$$\left(\frac{1}{k}\right)\frac{V_{in}}{RC}DT = V_{ref}\left(\frac{1}{k}\right) \qquad (3.2)$$

Where k is a scaling factor. Another advantage of this loop is that, since the integration is taking place on the switching node, so after the switches, the non-idealities of the power MOSFETs are taken into account in the integration process and the duty cycle is regulated accordingly. As an example: the value of R_{on} on the high side changes the value of V_{sw}, which will not be exactly equal to V_{IN}, but lower. This will result in a different slope of the integration, and a different value of the duty cycle to correct this loss.

3.3 Output Loop

With only this circuit, no information is fed to the loop directly from the output, so information like the ESR of the inductor are not considered in the regulation process, and this may result in poor load transient response. To improve this aspect, a second loop is added: the reference voltage V_{ref} is not fixed anymore, but is provided by an error amplifier computing the difference between a fixed reference voltage and the output voltage, just as in a traditional Voltage Control Moed loop [1]. Fig.3.1 (blue path) shows the error amplifier with the fixed reference voltage (typically a bandgap reference) and the compensation network made by the resistors and capacitors. A change in the output voltage will result in a change of V_{ref} in Equation 3.2, hence the reset pulse will come sooner or later according to the output variation. For this design, a Type-3 compensation was chosen [6]. The design of the opamp and the compensation network is described in later sections of this chapter.
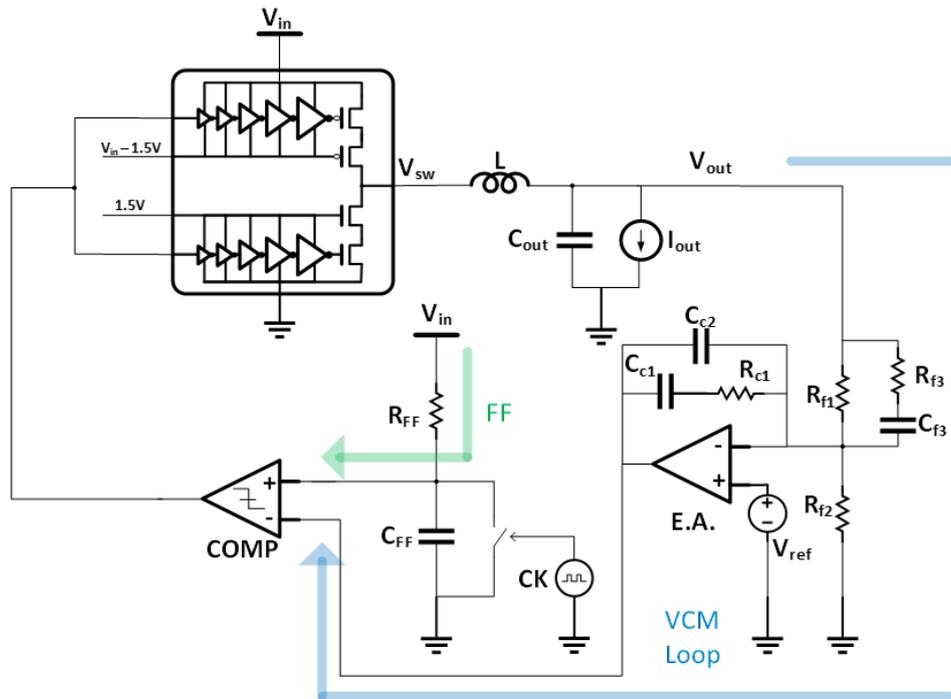
Figure 3.3: Schematic of the Feed Forward + VCM loop.

3.4   Feed Forward

As mentioned in Section 3.1, a second control strategy was designed for this project, and is shown in 3.3. This control loop consists in a Voltage Mode with Feed Forward. The working principle is the same as the standard VCM described in 1.3, but the generation of the sawtooth is handled differently: a pulse generator switching at a fixed frequency (again, 100 MHz in this case) with low duty cycle controls a switch that charges and discharges the capacitor C_{FF} through the resistor R_{FF}. What this loop is doing is basically integrating the input voltage in a similar way to the One Cycle loop previously described.The main difference is that in this case, the PWM wave comes directly from the output of the comparator, and the voltage coming from the error amplifier is not deciding a reset point, but an average value. When a change in the input voltage occurs, the peak and slope of the generated sawtooth wave will change accordingly, changing the output of the comparator and modulating the duty cycle of the PWM wave. As in the previous case, load changes are handled by
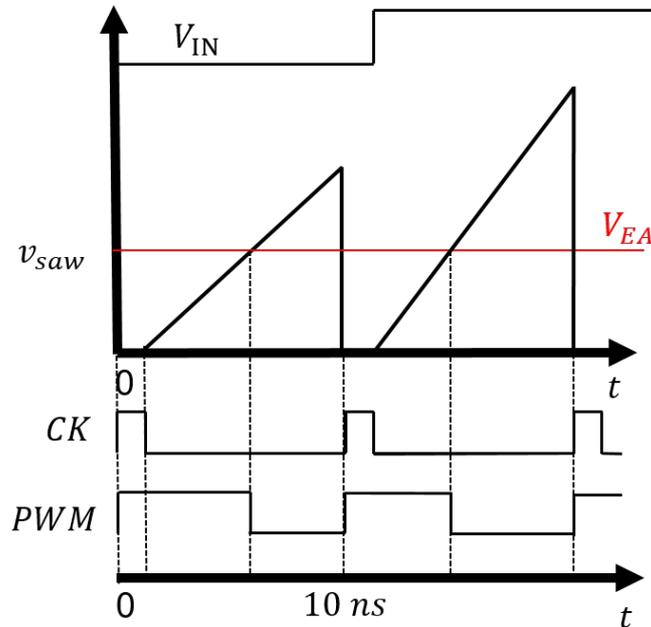
Figure 3.4: Working principle of the Feed Forward loop

the error amplifier connected to the output that changes the reference of the comparator. Fig.3.4 visualizes the working principle. Another key difference with the first control is that in this case the integration process is happening before the switches, so performance should be more affected by non-idealities of the MOSFETs. Both One Cycle and Feed Forward loops are integrated in this project, and the same error amplifier and compensation network of the VCM loop is shared between the two.

3.5 SIMPLIS Simulations

The two control loops described in the previous sections were firstly modeled and simulated on SIMPLIS to verify the functionality. In order to have a correct sizing of the compensation network that will be used in both control loops, the AC characteristics of the power stage in open loop must be investigated first. Fig. 3.5 shows the SIMPLIS model of the stacked power stage in open loop. In this model, the on-resistances and the gate capacitances of the MOSFETs are included as parameters of the transistor models. As seen in the
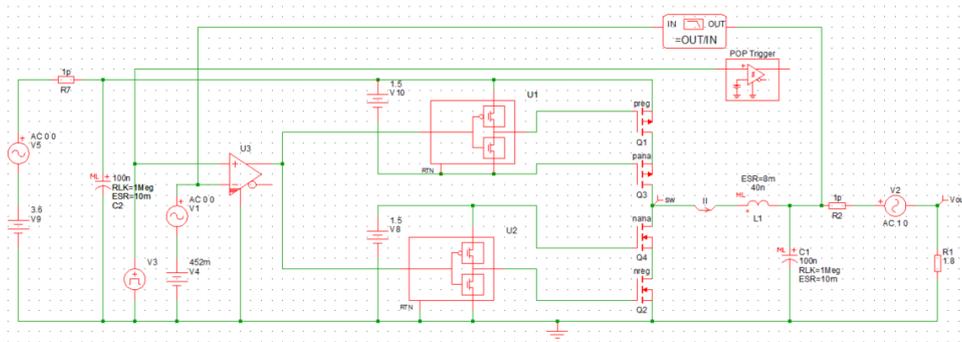
Figure 3.5: SIMPLIS model of the stacked power stage.
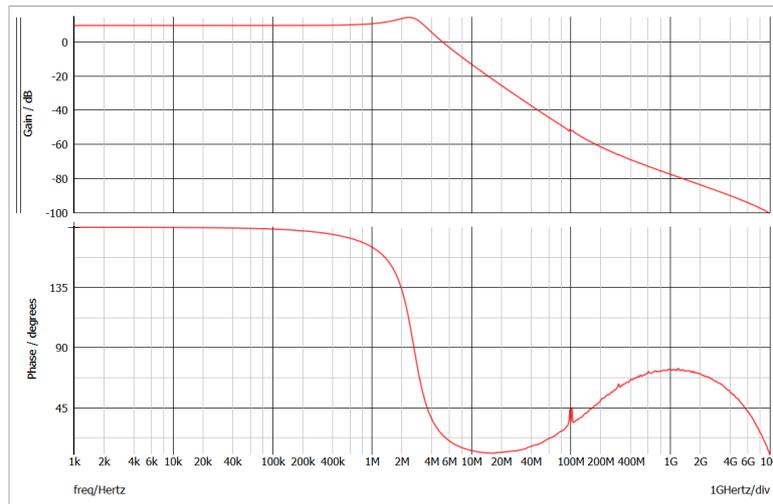
Figure 3.6: Magnitude and phase of the open-loop power stage.

figure, the output inductor was decreased to 40 nH and the output capacitor was increased to 100 nF. This changes have been done to increase the load transient response of the circuit. The AC characteristic of the power stage was simulated and the bode plot of magnitude and phase is shown in 3.6. From this simulation, it can be verified that the LC frequency is:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} = 2,52MHz \tag{3.3}$$

And the frequency of the zero caused by the ESR of the output capacitor is:

$\mathbf{R}_{f1}$	1.5 kΩ
$\mathbf{R}_{f2}$	750 Ω
$\mathbf{R}_{f3}$	25 Ω
$\mathbf{R}_{c1}$	2.5 kΩ
$\mathbf{C}_{c1}$	41 pF
$\mathbf{C}_{c2}$	1.2 pF
$\mathbf{C}_{f3}$	40 pF

Table 3.1: Compensator Parameters.

$$f_{ESR} = \frac{1}{2\pi R_C C} = 159MHz \tag{3.4}$$

With these values,the compensator poles and zeroes can be calculated as [6]:

$$f_{Z2} = f_{LC} = 2,52MHz \tag{3.5}$$

$$f_{Z1} = 0,75f_{Z2} = 1,9MHz \tag{3.6}$$

$$f_{P1} = 0 \tag{3.7}$$

$$f_{P2} = f_{ESR} = 159MHz \tag{3.8}$$

$$f_{P2} = \frac{f_s}{2} = 50MHz \tag{3.9}$$

From the poles and zeroes, the values of the resistors and capacitors in the compensation network can be set. Referring to either Fig. 3.1 or Fig.3.3, the resistor and capacitor values are summarized in Tab. 3.1.

The values in Tab. 3.1are calculated supposing an output voltage V_{out} equal to 1.8 V, a reference voltage V_{ref} equal to 600 mV and setting the cutoff frequency of the closed loop f_0 around 10 MHz (one-tenth of the switching frequency as said in Section 1.3). Fig. 3.7 shows the simulated magnitude and phase of the described compensator.

The One Cycle loop shown in Fig. 3.1 is then added to the SIMPLIS model in Fig. 3.5. Fig. 3.8 shows the AC characteristic of the closed loop. As expected
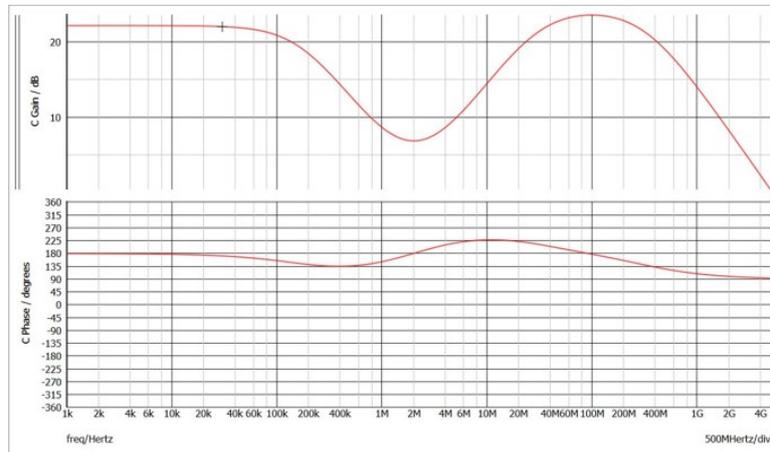
Figure 3.7: Magnitude and phase of the compensator.
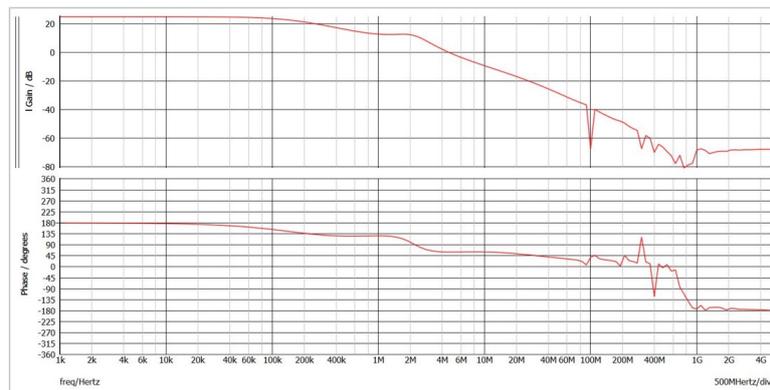
Figure 3.8: Magnitude and phase of the closed loop.

the cutoff frequency of the loop is around 10 MHz, with a phase margin of 64°. The same is done for the Feed Forward loop in Fig. 3.3 and the two circuits are fine-tuned to have the same bandwidth.

The two solutions are simulated and compared. Firstly, AC simulations for the output impedances of the two loops are presented in Fig. 3.9. Both loops show a peak output impedance of 180 mΩ at around 8 MHz, but the One Cycle loop shows a lower DC output impedance with respect to the Feed Forward loop. Secondly, transients simulations were performed to compare line and load jump responses in the outputs of the two circuits. For these simulations a load step was given first, ranging from 0.5 A to 1.5 A and vice
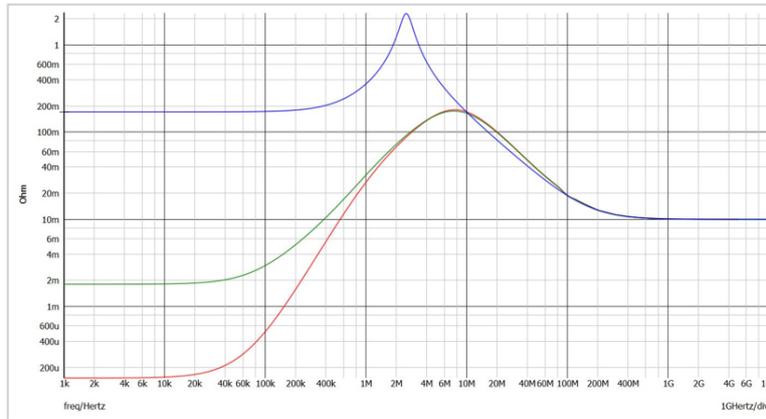
Figure 3.9: Output impedance. Red: OC+VCM, green: FF+VCM, blue: power stage.
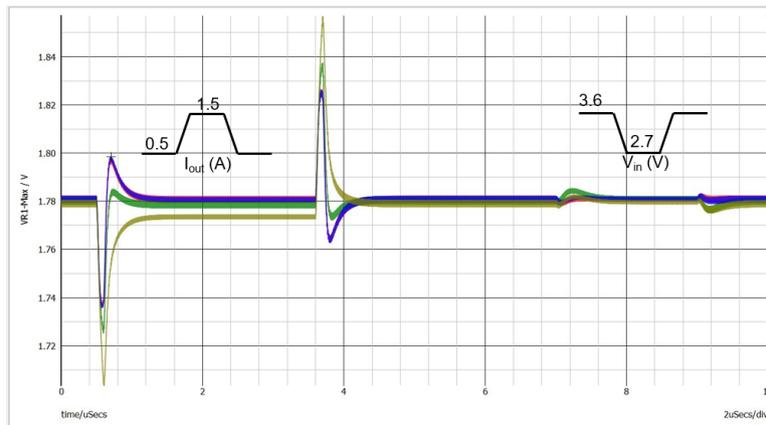
Figure 3.10: Transient Responses. Red: OC+VCM, green: FF+VCM, blue: OC+VCM(10xRon), yellow: FF+VCM (10xRon).

versa with 100 ns of rise and fall times. After the load step, a line step was applied, from 3.6 V to 2.7 V and vice versa, again with rise and fall times equal to 100 ns. The circuits were first simulated in their nominal conditions. then simulated again with exaggerated parasitics (i.e. gate capacitance and on resistance), and the outputs are shown in Fig. 3.10. In nominal conditions, the One Cycle loop (red) performs slightly better than the Feed Forward loop (green). The difference in performance is more evident when multiplying the on resistances of the MOSFETs by 10 times. In the case of One Cycle (blue),

	DC Out Imp (Ω)	Peak Out Imp (Ω)	Loop f_0 (Hz)	PM (°)	Worst Load Trans (V)	Worst Line Trans (V)
Power	160m	2 @ 2 MHz	-	-	-	-
FF	1.8m	180m @ 8 MHz	10 M	57	55m	5m
OC	160u	180m @ 8 MHz	10 M	64	44m	2m

Table 3.2: SIMPLIS Performance comparison.
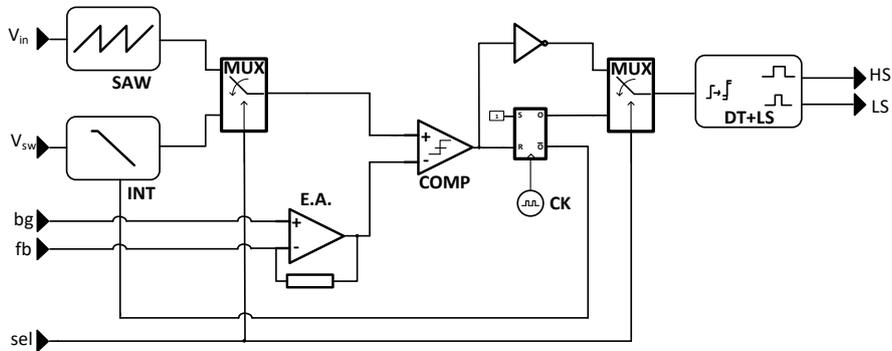
Figure 3.11: Block diagram of the two loops.

the two curves are exactly superimposed, while the Feed Forward (yellow) shows a more critical loss in performance. This is due to the fact that the One Cycle loop is integrating the voltage at the switching node, so after the power MOSFETs, compensating for the ohmic losses. No critical difference was observed when increasing the parasitic capacitances. Table 3.2 summarizes the results that were just discussed.

3.6 Cadence®Virtuoso Design

In this section the transistor level design of the control loops is described, with details on the main blocks.

3.6.1 Concept

As mentioned, both control loops have been implemented at transistor level using Cadence®Virtuoso. Integrating both loops is relatively simple, as they share different blocks. To do so, only two additional analog multiplexers are

Figure 3.12: Schematic of the error amplifier

required in the loop. Fig. 3.11 shows the block diagram of the two combined loops. The two multiplexers (MUX) are both controlled by the loop selection signal "sel" coming from the outside. The first one decides the positive input of the comparator (COMP) between the integrator (INT) output for the One Cycle loop and the sawtooth (SAW) wave for the Feed Forward loop, while the second multiplexer chooses which output goes to the dead-time and level shifter (DT + LS) block: the output of the SR Flip-Flop for the One Cycle or directly the inverted output of the comparator for the Feed Forward. From the DT+LS block, the two output signals controlling the High Side (HS) and Low Side (LS) are generated. As seen in the picture, the same Error Amplifier (E.A.) is shared between the loops, taking as inputs the feedback signal (fb) and the bandgap reference (bg).

3.6.2 Error Amplifier

For the design of the error amplifier, the main target is to have a bandwidth as high as possible. Since the targeted f_0 of the loop is 10 MHz, the error amplifier should have a - 3 dB cutoff frequency of at least 10 MHz, to avoid the addition of unwanted poles in the loop that may cause instability. To target such high bandwidth, the most simple architecture was chosen: Fig. 3.12 shows the schematic of the error amplifier. The input stage is a simple NMOS differential pair, while the output is a source follower. With this structure it is impossible to achieve high gain. However, moving to more complex archi-

Figure 3.13: Bode plots of the error amplifier.

tectures would inevitably affect the bandwidth. Fig. 3.13 shows the Bode plot of the simulated EA. The DC gain is 32 dB with a bandwidth of 10 MHz and a phase margin of 48°. The circuit is biased with a current of 35 μA and overall consumes 240 μA. the high current consumption is again necessary for maximizing the bandwidth, but it's negligible if compared with the current consumption of the power stage.

3.6.3 Feed Forward Sawtooth

To generate the sawtooth wave for the Feed Forward, a very simple pulse generator, shown in Fig. 3.14 is used. The 50% duty cycle clock at the input passes through an AND gate that has an inverted and delayed replica of the same clock signal as its second input. The result is a train of short pulses, with their width equal to the delay introduced in the path of the second input of the AND. These pulses turn off the NMOS, discharging the capacitor C_{FF} and generating the desired sawtooth wave from the input voltage V_{in}.

3.6.4 Integrator

For the integrator in the One Cycle loop different architectures were simulated. A Type II current conveyor circuit like the one proposed in [15] was designed and simulated, but then discarded due to the high current required. Instead, a much simpler RC circuit with a switch resetting the capacitor is used, exactly like the one used in the Feed Forward loop, with the difference that the switch is controlled not by a fixed train of short pulses, but by the inverse of the PWM wave that controls the power stage. Fig. 3.15 shows the difference in the performance of the integration between the current conveyor and the RC. With a similar integration slope, the simple RC circuit reacts faster, and consumes
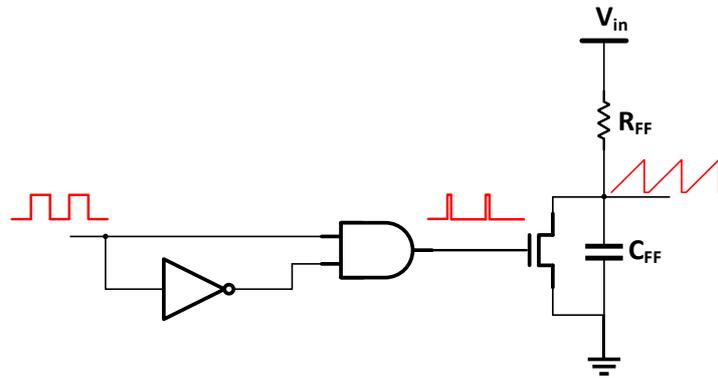
Figure 3.14: Feed Forward sawtooth generator.
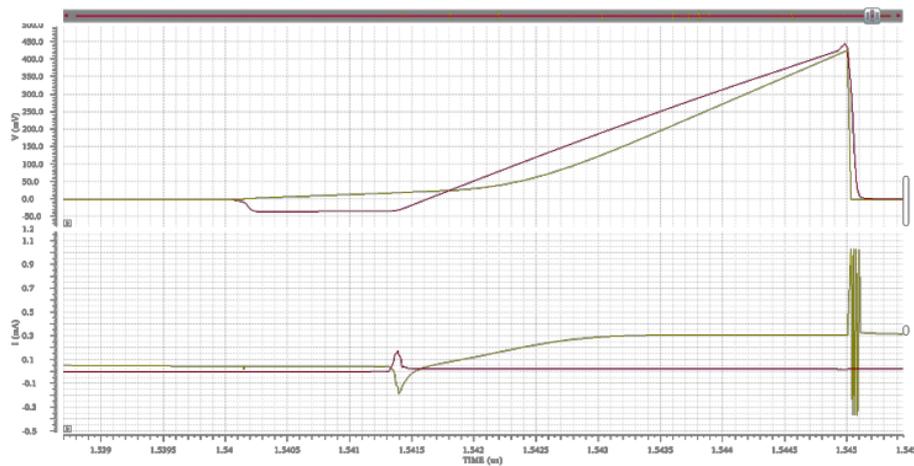
Figure 3.15: Current consumption of Current Conveyor (yellow) vs RC integrator (red).

roughly one-tenth of the current consumed by the current conveyor.

3.6.5 Comparator

For the case of the comparator design, propagation delay is the most critical parameter to optimize, as it critical for the One Cycle loop to have minimum possible delay between the integrated waveform touching the reference voltage and the actual reset of the integrator. Similarly to the error amplifier, to
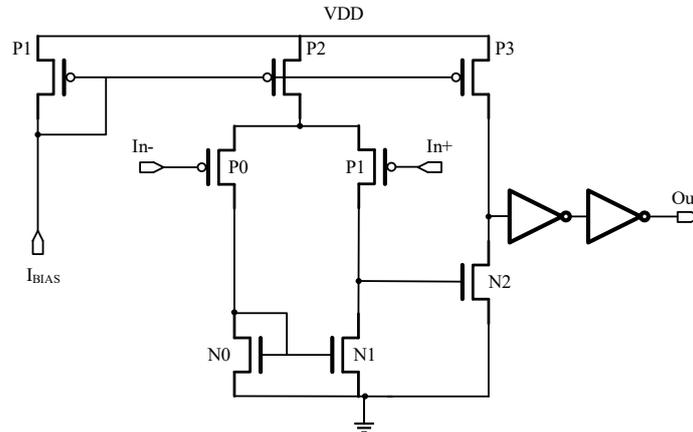
Figure 3.16: Schematic of the comparator.

achieve minimum delay, the most simple structure with a differential pair, output stage and two output inverters for retification has been used, with transistors having minimum channel length. The schematic is shown in Fig. 3.16. A PMOS input pair was chosen to allow higher voltage range at the input. The resulting propagation delay is around 1 ns.

3.6.6 Trimming of the Capacitor in the two Loops

The RC nets used for both loops are simple, functional and easy to implement. However, due to the high variation of the capacitance value in different temperature and process corners, the integration slope may change substantially at different temperatures. Such high slope variation can cause variations in the loop that may compromise the correct functionality of the system. Between the two, the One Cycle loop is the most sensitive to this variation: for example, the integration slope can become so slow that the reset pulse skips one clock cycle and the circuit find an unwanted stability condition at half the switching frequency. Fig. 3.17 shows the One Cycle loop in case of the unwanted 50 MHz operation. On the other hand, a too fast integration slope can lead to instability of the circuit.

To mitigate this issue, a rudimental trimming of the capacitors has been designed. Having only one available pin on the package and no digital infrastructure, the simple ADC in Fig.3.18 has been designed. Each of the two comparators is comparing a different partition of the voltage on the pin with
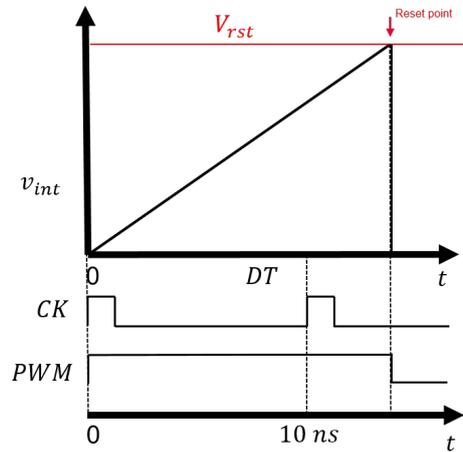
Figure 3.17: Working principle of a One Cycle loop when in half-frequency operation.
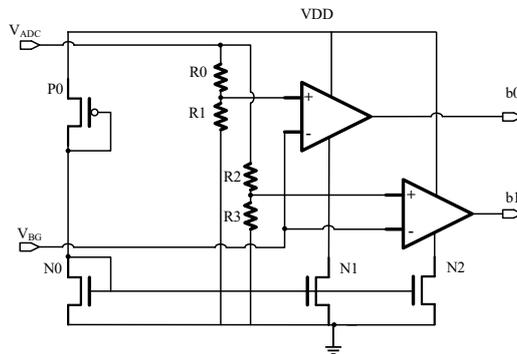
Figure 3.18: Schematic of the ADC.

the bandgap reference, allowing two 'bits' at the output, with three possible configuratons from an analog voltage on the pin. The two digital signals can then add or subtract capacitance from the integrator or the sawtooth generator, correcting the change in the integration slope at different temperature. The trimming was limited due to the research nature of the work. Obviously, for a possible product, a more precise trimming and a more complex digital infrastructure would be available, improving the circuit performance at different temperature and process corners.

3.7   Concept of the Full Chip

Finally, Fig. 3.19 shows the full block diagram of the chip. Besides the blocks already discussed, i.e. the two power stages with their respective internal bias generators and the two controls included in "LOOP", the "CEFU" block comprehends all the supply and bias circuit, like the bandgap, two 1.5 V regulators (one dedicated to the analog circuits, one dedicated to the digital), one "$V_{in} - 1.5V$" generator, the bias current generator, and a clock that can work at 100, 50 or 25 MHz. The two multiplexers are needed to select both the power stage and the loop that is being used through the "sel_loop" pin and an ADC which is just a 3-bit version of the one previously described.
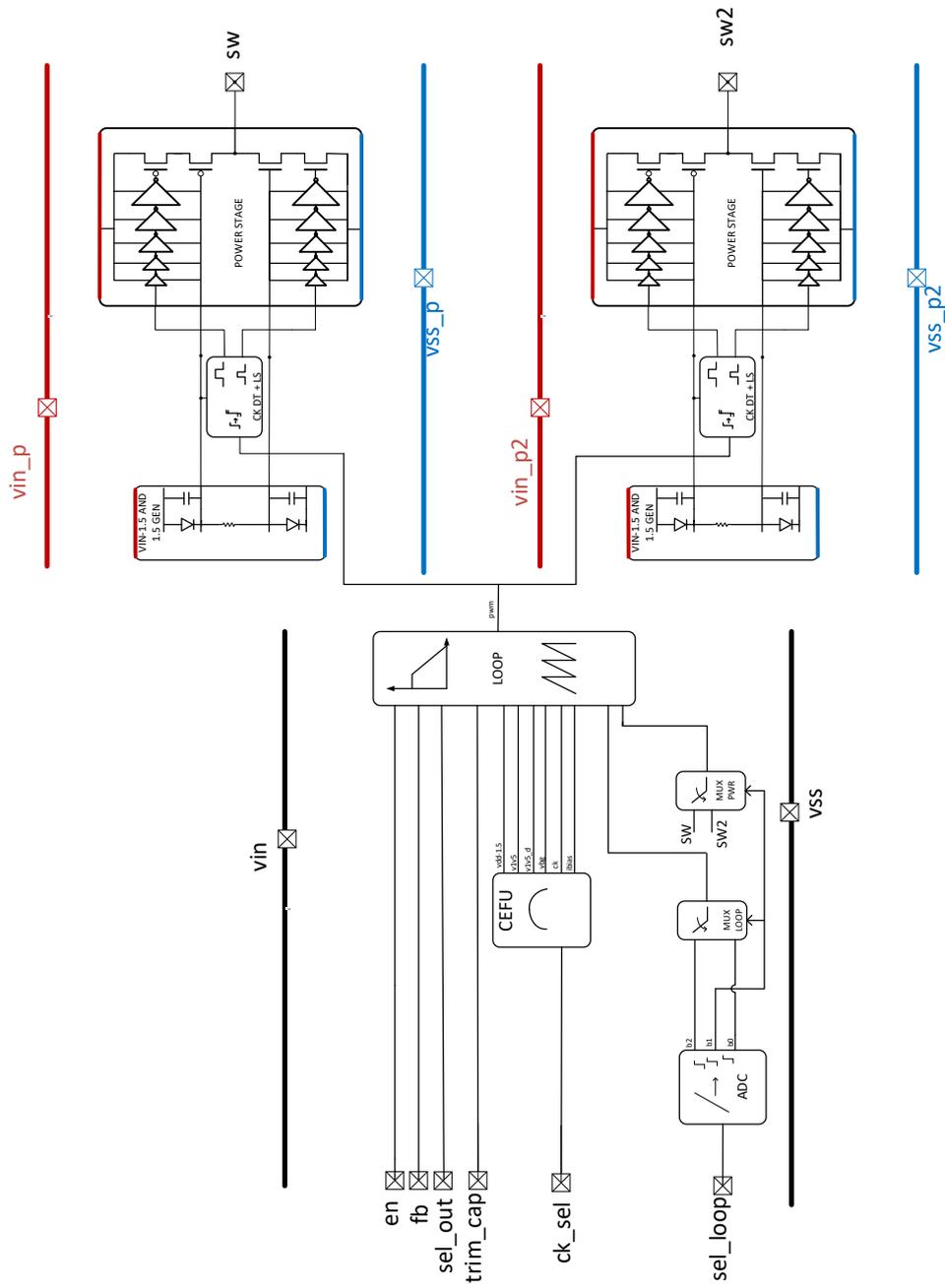
Figure 3.19: Full block diagram of the chip.

Chapter 4

Measurements

This chapter gives a description of how the chip was bonded and assembled, then an overview of the most critical points in the Printed Circuit Board (PCB) design is given, closing with the measurement results.

4.1 Bonding and Packaging

The available package for this project is a plastic 14-pins dual-in-line. Fig. 4.1 shows the bonding diagram of the circuit, while Tab. 4.1 shows the pinout of the chip. Pins 1-3 and 12-14 are dedicated to the two power stages, pins 7 and 8 are the signal supply and ground, pin 11 is the feedback pin, pin 4 is for the enable signal, and pins 5-9 are for selection and trimming functions. As it can be seen from the figure, each of the six power pins has been triple-bonded to reduce the effects of the parasitic equivalent bond inductance described in Chapter 2. For the same reasons, the die has been bonded with an offset of 300 μm to the right. The resulting average lengths of the bondwires on vin_p(2) and vss_p(2) are, respectively, around 1.4 mm and 997 μm, with resulting equivalent parasitic inductances around 287 pH and 490 pH. The length of the bonds on the two sw pins is minimized as well, to reduce the parasitic resistance of the bondings that adds in series to the output inductor's series resistance, increasing the conduction losses. The feedback pin also benefits from decreased bonding length, as parasitic resistance and inductance may influence the stability or the dynamic performances of the loop. The trade-off is an increased length of the bondings on the signal supply and ground signals (vin and vss), while all the other signals are static, so no significant issue is expected from the bondings.

Figure 4.1: Bonding diagram of the chip.

Pin	Name	Function	Pin	Name	Function
1	vss_p	power ground	**14**	vss_p2	power ground (second power)
2	vin_p	power supply	**13**	vin_p2	power supply (second power)
3	sw	switching node	**12**	sw2	switching node (second power)
4	en	enable	**11**	fb	feedback
5	sel_out	output selection	**10**	trim_cap	loop capacitance trimming
6	ck_sel	clock frequency selection	**9**	sel_loop	power stage and loop selection
7	vin	signal supply	**8**	vss	signal ground

Table 4.1: Pinout of the chip.

4.2 PCB Design

Given the high switching frequency of the circuit, particular care has to be put in the PCB design as well. Parasitic inductances, capacitances and resistances from the board could have the same negative impact on the performance as the parasitics of the bondings previously discussed. Fig. 4.2 shows the designed board. Fig. 4.2 (a) shows the top layer of the board. The design for the two power paths is symmetrical on the y axis, with the power supplies VIN_P

Figure 4.2: Designed board layout: (a) top layer, (b) bottom layer.

and VIN_P2 placed as close as possible to their respective pins, with arrays of four capacitors (C_P and C_P2) to filter out the noise and the inductive effects from the PCB traces. The ground is placed close to the power ground pins of he chip, and the ground plane is spread all over the board on top and bottom layers, with a large number of vias to minimize the total parasitic inductance. The switching nodes are connected to the two custom footprint for the selected air-core inductors (L and L2) and their respective array of 3 output capacitors (C_out and C_out2), which are placed as close as possible to the input capaicitors to minimize the current loop from the input to the output. A standard inductor footprint has been placed in case other types of inductors need to be tried. Two connections for each output are placed, (one banana and one coaxial each) for more versatility and to allow force/sense measurements. The two outputs are then connected to the feedback pin through the solder jumper S_fb, that will select which of the two outputs is connected to the voltage loop. An RC filter for the noise is added to the feedback path. On the bottom layer, Fig. 4.2 (b) all the enable, selection and trimming inputs are placed (sel_loop, trim_cap, en, sel_out, ck_sel). Being those static signals, it is fine to place them on the bottom layer, further from the chip. A noise-filtering capacitor is placed on each input. On the bottom layer is also placed the signal supply vin. Placing vin on the bottom layer is not ideal, but given the pinout of the circuit, the priority is given to the minimization of the feedback path, and the array of capacitors between vin and signal-ground placed on the top

Feed Forward		One Cycle	
Load Current (mA)	Output Voltage (V)	Load Current (mA)	Output Voltage (V)
164	1.35	192	1.54
340	1.21	420	1.5
430	1.28	490	1.52
610	1	610	1.45

Table 4.2: Load regulation.

layer should filter out the inductive effects of the PCB track and via.

4.3   Measurements

The chip has been measured in both Infineon sites of Pavia and Padova. Unfortunately, most of the measurements in Padova are still undergoing, so mainly some preliminary results from Pavia are presented. All the measurements described next refer to the power stage 1.

4.3.1   Load Regulation and Efficiency

In the first set of measurements, the input voltages vin_p and vin are given through a continuous power supply, the load current is given through power resistors or SMU, and the enable signal is given as a DC voltage, letting the converter run indefinitely. Tab. 4.2 summarizes the results of some load regulation measurements done at 50 MHz. The first noticed issue was a significant reduction in the load regulation with respect to the expected. The cause of this drop in the load regulation is still under investigation, but it is suspected to be is due to some parasitic resistance effect either in the PCB traces or in the setup. This effect is probably worsened by the fact that the heating caused by the long-running time of the converter is degrading the R_{on} of the transistors in the power stage. Heavy coupling between input voltage and output voltage is also observed. These measurements were done with an input voltage of 4 V. The output voltage is measured with a multimeter and the output current with a current probe. The values of the output currents don't exactly match in the two loops due to the fact that passive resistors were used for the output in this setup. The measurements suggest that the supposed parasitic resistance effect is having a stronger impact when using the Feed Forward loop, with respect to the One Cycle. In these measurements, both the output current and the

Measure	P1:ampl(C1)	P2:freq(C1)	P3:rise(C1)	P4:fall(C1)	P5:duty(C1)	P6:ampl(C2)	P7:mean(C2)	P8:min(C3)
value	3.808 V	51.531 MHz	928 ps	664 ps	41.032 %	114 mV	1.523 V	-52 mV
mean	2.963 V	51.8866 MHz	< 3.081 ns	< 2.005 ns	36.640 %	169.0 mV	1.0916 V	-37.8 mV
min	83 mV	51.117 MHz	< 99 ps	< 124 ps	21.409 %	61 mV	-59 mV	-537 mV
max	5.442 V	52.692 MHz	< 97.228 ns	< 98.132 ns	41.677 %	954 mV	1.633 V	3.88 V
sdev	1.572 V	161.2 kHz	< 7.614 ns	< 6.467 ns	3.481 %	190.9 mV	607.5 mV	176.3 mV
num	20.897e+3	67.473e+3	93.235e+3	93.801e+3	67.473e+3	20.828e+3	20.828e+3	51.130e+3
status	✔	✔	✔	✔	✔	⊓		

Figure 4.3: Detail of the switching node (yellow) and output voltage(pink).

frequency are set lower than expected, because going to higher currents makes both loop loose the regulation, and going to100 MHz in this setup makes the Feed Forward Loop lose the regulation with even lower currents, so a comparison is not useful in this case. Looking at a detail of the switching node in Fig. 4.3 (measured with an active probe) it can be seen that the rising and falling times are much slower than the values expected, which were not more than 100 ps. This might again be related to some unknown parasitic effects on the setup. The waveforms in Fig. 4.3 are captured in the One Cycle case, with around 300 mA of output current, but the results apply also in the Feed Forward case. In these conditions, the peak efficiency is reached with an input voltage of 3.6 V and an output current of 150 mA. The graph of the efficiency vs output current is shown in Fig 5.23, peaking at 83% for the One Cycle loop, and 80% in the Feed Forward loop. The fact that the efficiency peak is fount at a much lower output current value than the expected one is a further suggestion that a parasitic resistor effect is degrading the effective R_{on} of the power stage, hence increasing the conduction losses with higher load currents. First measurements in Padova shows that moving the output capacitors from their current position and placing them along the feedback PCB trace has a positive effect on the load regulation.

4.3.2 Transient Measurements

For the transient measurements, the enable signal is a pulse of 180 μs with 1 ns of both rise and fall times. In order to allow line transient measurements, the input voltage is now provided in the following way: a function generator in fed as input to a power amplifier which, in turn, supplies the circuit. The
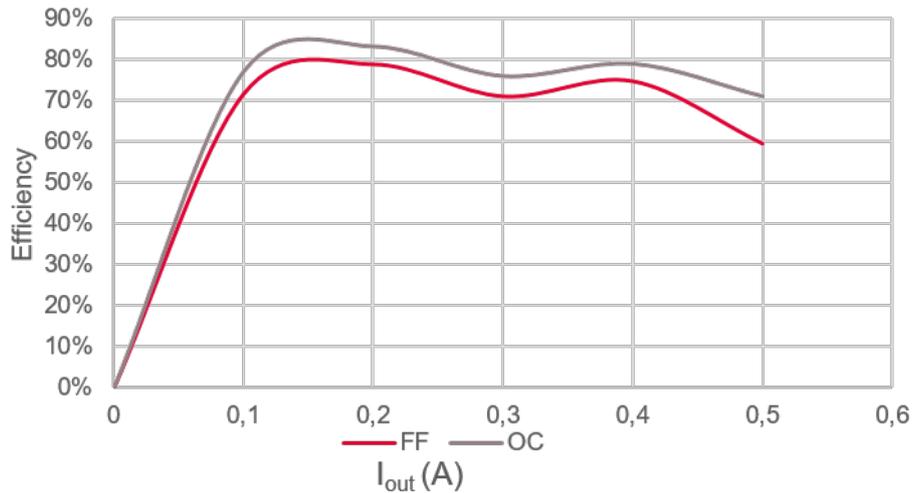
Figure 4.4: Measured efficiency at 50 MHz.

main issue with this setup is that the power amplifier needs a big electrolytic capacitor to reduce the ringing, and this limits the rise and fall transients of the DC-DC input voltage to ∼2 μs. The resulting DC-DC input voltage is a pulse ranging from ∼4.1 V to ∼4.8 V with a width of 50 μs and a delayed of 50 μs with respect to the triggering of the enable. The output current is again set with resistors. With this setup, both 100 and 50 MHz are presented. From now on, all the waveforms shown on Channel 1 are the input voltage (measured before the filtering capacitors), on Channel 2 the output voltage (measured with a BCD connected to the oscilloscope), on Channel 3 the switching voltage (measured with an active probe), on Channel 4 the output current (measured with the current probe). Fig. 4.5 shows an overall of the line transient response in the case of the One Cycle loop working at 50 MHz, while Fig. 4.6 shows the details of the waveforms when the input voltage is high (a) or low (b). From the figures it can be seen that the converter is correctly modulating its duty cycle in the different input voltage conditions, but similar issues than the ones observed in the previous measurements occur: the circuit exhibits a worst line regulation than expected, probably due to the same parasitic resistance described before. The measurements show some glitches during the transients, caused by the poor performance of the input error amplifier in the setup. The same measures are presented in the case of the Feed Forward in

	[8]	**[13]**	**[14]**	**[17]**	**This Work**
Technology [μm]	0.18	0.18	0.6	0.13	0.12+0.4
V$_{in}$ [V]	2.8	3.3	5	1.2	4
Out. Inductance [nH]	36	330	220	3-8	40
Out. Capacitance [nF]	4700	1600	4.7	1.87	100
Frequency [MHz]	60/100	10	32	100	50/100
Peak Efficiency	93%/88%	-	83%	82.4%	83%/80%(exp)
Load current [mA]	1000	1200	500	1200	1000
Load step	500 mA/4μs	1.15 A/ns	0.5A/20ns	140 mA/μs	1 A/100 ns
Load transient	250 mV/V	56 mV max	190 mV max	80 mV max	40 mV max (exp)
Line transient	6 mV/V	-	-	-	180 mV (exp <5 mV)

Table 4.3: Performance comparison.

Fig. 4.7 and Fig. 4.8. In this case, glitches on the output are more frequent, as the circuit is directly integrating the input voltage. Between the two, the One Cycle has a slightly better line regulation (200 mV of difference on the One Cycle vs. 300 mV on the Feed Forward), but a direct comparison of the line transient response is impossible due to the glitches. Finally a 100 MHz transient is shown for the case of the One Cycle loop in Fig. 4.9 and Fig. 4.10 and of the Feed Forward loop in Fig. 4.11 and Fig. 4.12, showing that both loops are functional also at 100 MHz. All these measurements have been done with a 3.6 Ω resistor as output load. Tab. 4.3 compares the result of this work with other high frequency DC-DC in found in literature, although some values are sill reported as "expected".

4.3.3 Future Measurements and Setup Improvements

As mentioned, more accurate measurements are being conducted in the Infineon Padova site. First results indicate a slight improvement in the load regulation by changing the input and output capacitors with more preforming components, and by moving the output capacitors alongside the feedback path, but still does not solve the issue and a heavy coupling between input and output is stll present. More trials are scheduled in the near future: to reduce in/out coupling, a new high performance inductor is going to be tried. Eventually, to solve the load regulation issue, a new board will be designed, with four layers to allow shorter traces, hence reducing the parasitic paths.
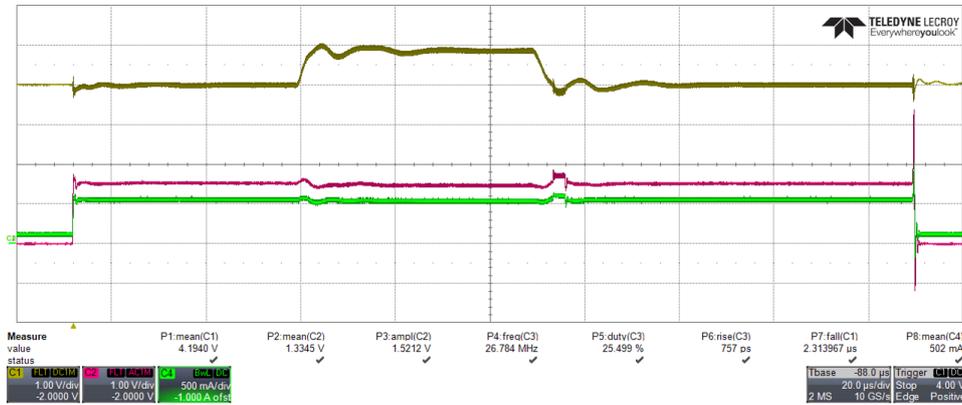
Figure 4.5: Overall line transient response. One Cycle, 50 MHz.
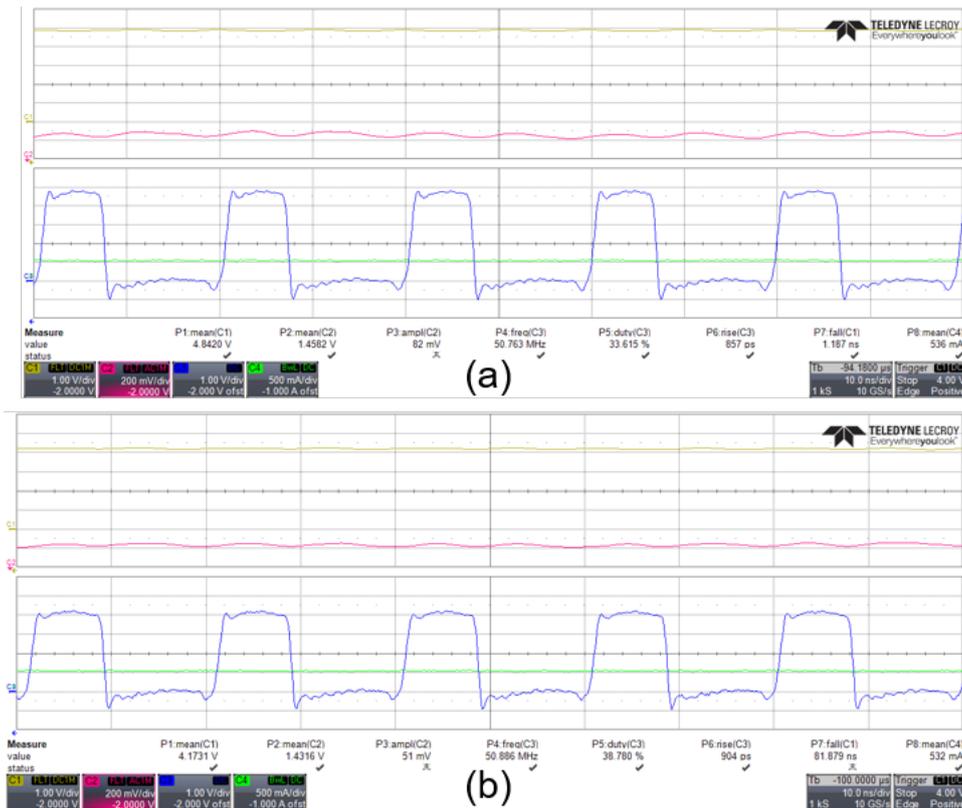
Figure 4.6: Details of the waveforms when input is high (a) or low (b). One Cycle, 50 MHz.
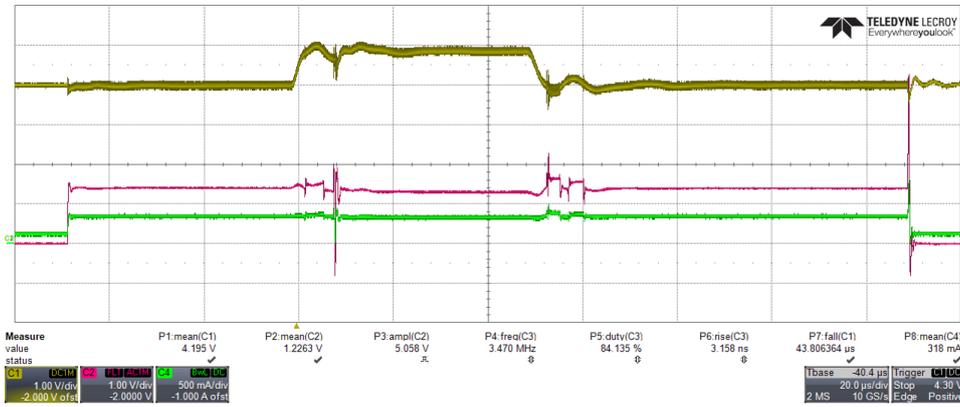
Figure 4.7: Overall line transient response. Feed Forward, 50 MHz.
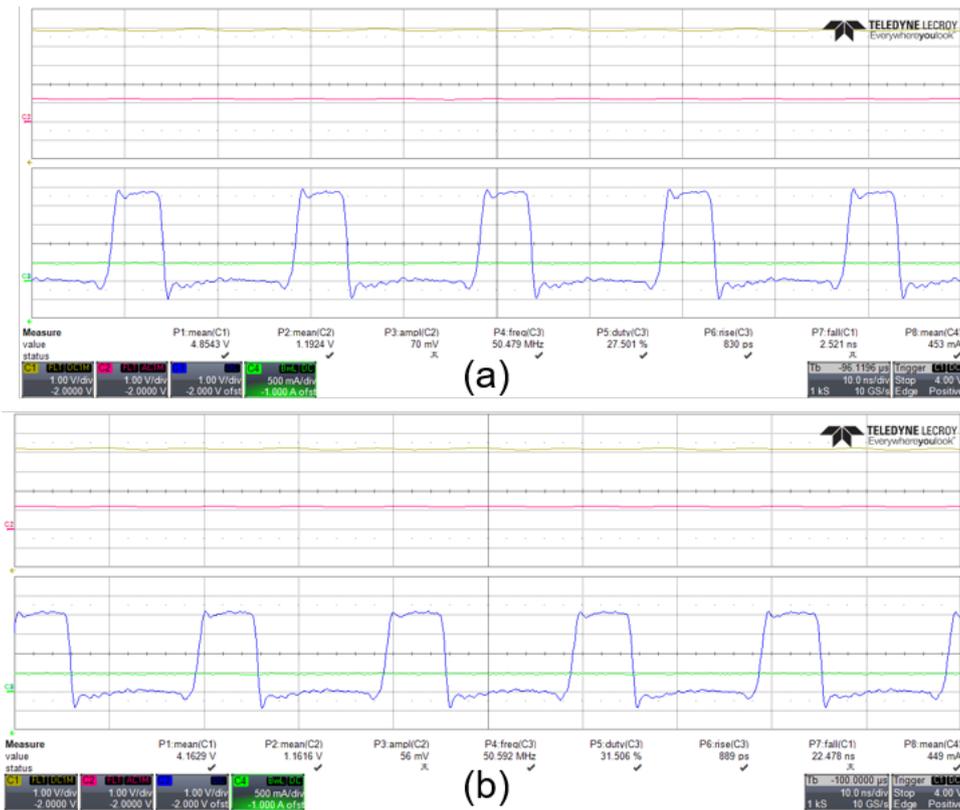
Figure 4.8: Details of the waveforms when input is high (a) or low (b). Feed Forward, 50 MHz.
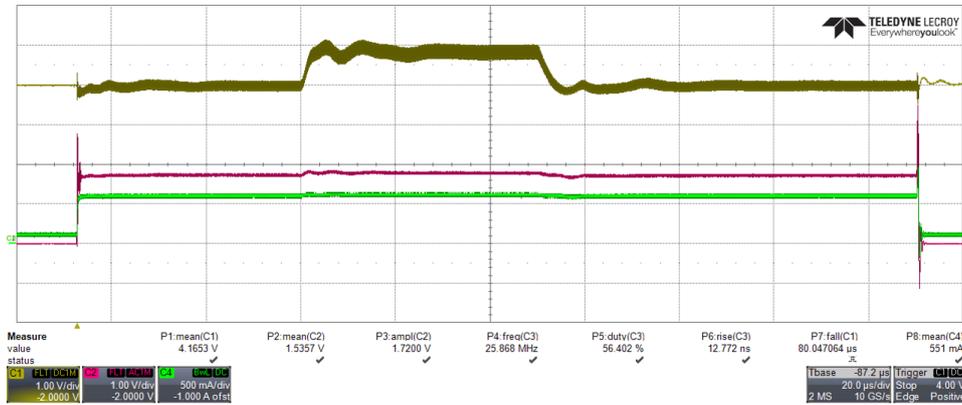
Figure 4.9: Overall line transient response. One Cycle, 100 MHz.
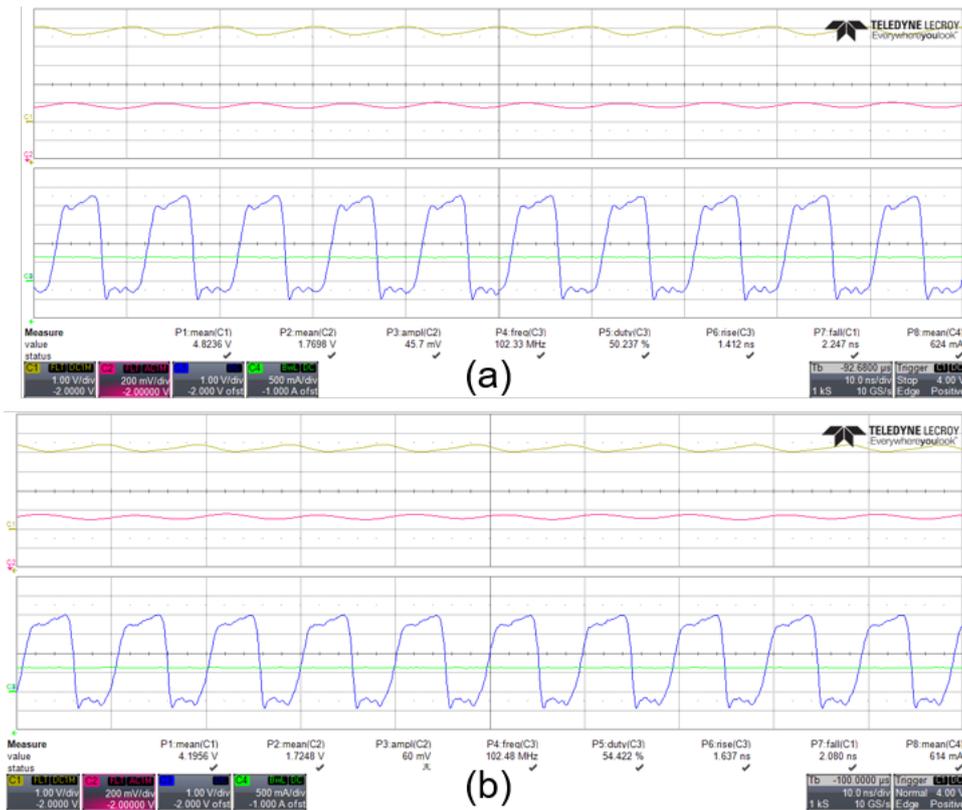
Figure 4.10: Details of the waveforms when input is high (a) or low (b). One Cycle, 100 MHz.
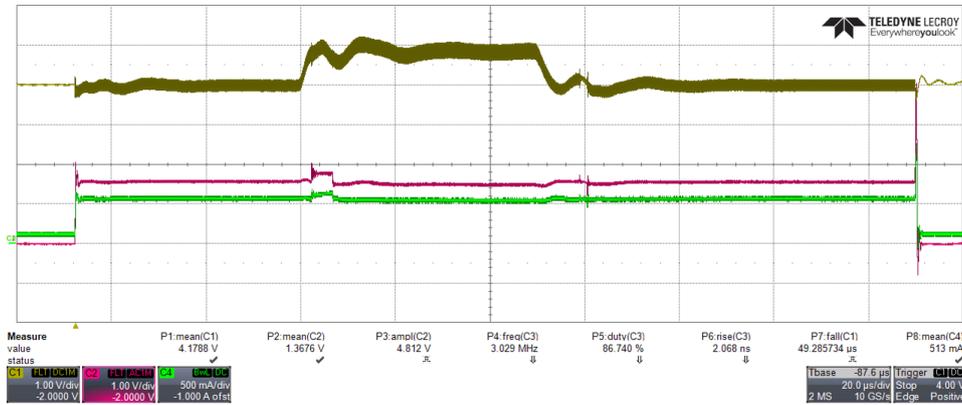
Figure 4.11: Overall line transient response. Feed Forward, 100 MHz.
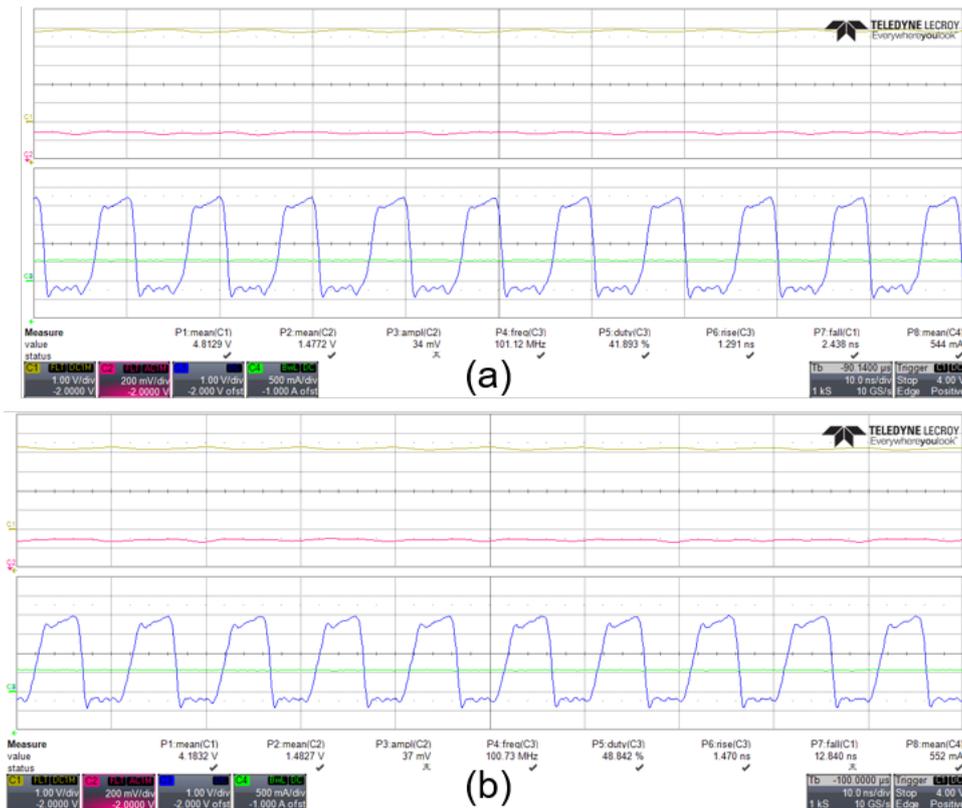
Figure 4.12: Details of the waveforms when input is high (a) or low (b). Feed Forward, 100 MHz.

Chapter 5

Secondary Activity: SIBO DC-DC for AMOLED

The second research topic of this PhD work is focused on Single-Inductor Bipolar-Outputs (SIBO) DC-DC Converter for Active Matrix Organic Light Emitting Diode (AMOLED) displays. This part of the research was conducted thanks to the collaboration between the University of Pavia and the University of Macau. This chapter briefly introduces AMOLED displays and how they are driven, then gives a short introduction to Single-Inductor-Multiple-Outputs DC-DC converters. After that, the designed circuit is described.

5.1   Introduction to AMOLED Displays

During the last decade, Active Matrix Organic Light Emitting Diode (AMOLED) displays have been increasingly replacing the traditional Liquid Crystal Displays (LCDs). While at first only in portable devices, AMOLED displays can now be found also in larger size devices, like tablets and televisions. Most of the advantages of AMOLED displays come from the use of thin layers of an organic (i.e. carbon-based) material that have the property of producing luminescence if stimulated by an electrical current. Since the luminescence comes from the organic material itself, no backlight panel is needed, while LCDs use a Light Emitting Diode (LED) backlight panel to provide light to the pixels.
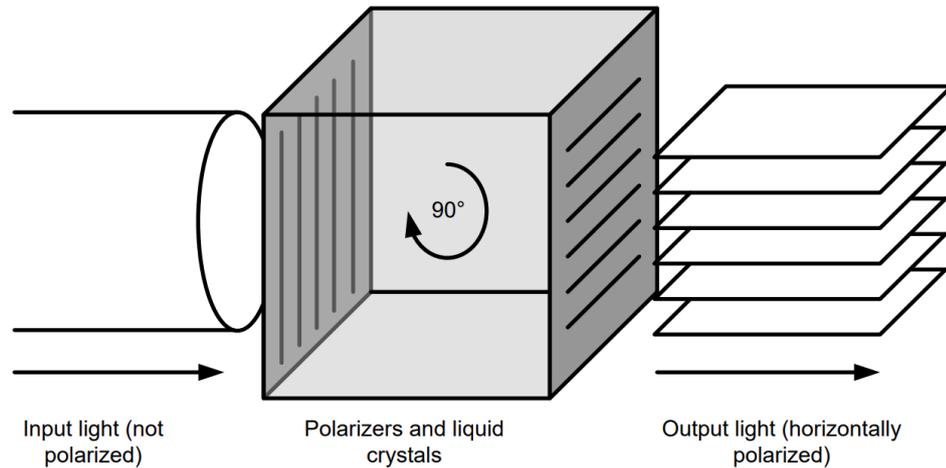
Figure 5.1: Concept of an LCD pixel.

5.1.1   LCD

In an LCD pixel, the light comes unpolarized from the LED source. The light goes through a first, vertical, polarizer. After the first polarizer, the vertically polarized light passes through a layer of liquid crystals. Liquid crystals have the property of rotating the polarization of the incident light as a function of the electric voltage applied to the layer. This voltage is provided to the liquid crystal layer by two transparent electrodes. After the liquid crystal layer, another polarizer is present. The second polarizer is orthogonal to the previous one. As an example, if the voltage applied to the liquid crystals is such that the rotation of the polarization of the incident light is zero, the vertically polarized input light will arrive at the horizontal polarizer without changing its polarization. Since the polarization of the light and the polarizer are orthogonal, no light will pass through the horizontal polarizer, and the pixel will appear black. By changing the voltage on the liquid crystal layer, the polarization will rotate when the light is passing through: a higher rotation angle will result in more light at the output. In the extreme case of a 90° rotation, all the vertically polarized light will be horizontal after the liquid crystals, so the output light of the pixel will be maximized. Fig. 5.1 shows a simplified conceptual diagram of an LCD pixel, in the case of a rotation angle of 90°.
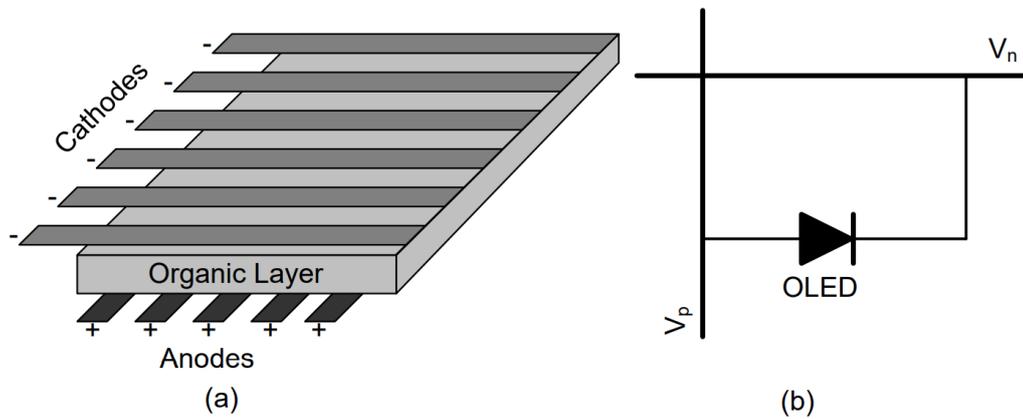
Figure 5.2: Simplified schematics of a) a PMOLED panel and b) a PMOLED pixel.

5.1.2 AMOLED

The absence of a backlight panel is a key advantage in the AMOLED technology, as it leads to an obvious reduction in the dimensions and weight of the display, and to a lower power consumption (when a pixel is black no light is emitted, while in the LCDs the backlight panel is always on). Due to the reduced thickness and weight, flexible AMOLED displays are realizable, [18], which led to the production of curved or even foldable displays in recent smartphones. Other advantages of AMOLED displays are: better contrast ratio, faster refresh rates, and wider viewing angle, [19]. The major disadvantage is that the AMOLED displays' lifetime is shorter than the LCDs' one, but this is becoming more and more irrelevant since the AMOLED displays' lifetime is constantly being increased, and it can reach hundreds of thousands hours of use nowadays. The OLED pixel is the elementary element that makes a display. In an OLED pixel, the organic layer is placed between two electrodes that work as anode and cathode, providing the current required to turn on the pixel when a proper voltage is applied. The single pixel is commonly modeled as a diode and, in order to build a full screen, a number of pixels are arranged in a matrix. A distinction has to be specified between Passive Matrix OLED (PMOLED) and AMOLED. Fig.5.2(a) shows a conceptual diagram of a PMOLED panel. As shown in the figure, multiple electrodes are placed orthogonally on the top and bottom of the organic layer, thereby defining the rows and columns of the matrix. Each interception of the matrix is a pixel. Fig.5.2(b) shows the simplified schematic diagram of a single pixel of a PMOLED display. The pixel
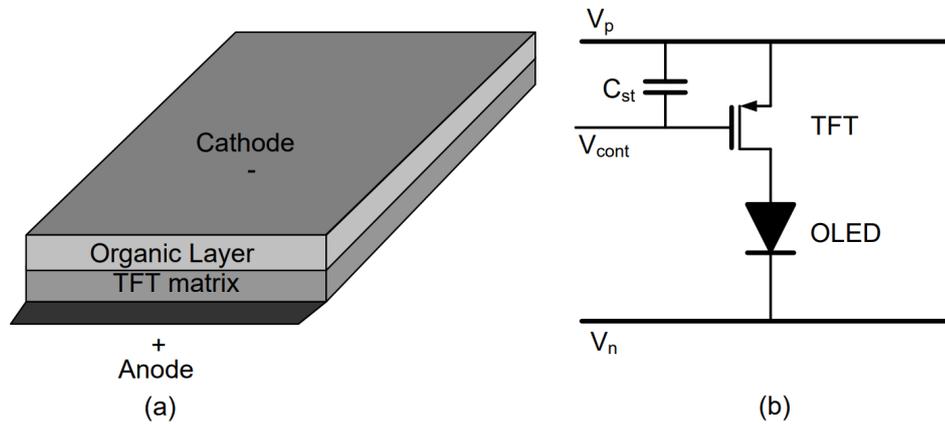
Figure 5.3: Simplified schematics of a) an AMOLED panel and b) an AMOLED pixel.

consists of a diode and two supply lines: one positive (V_p) and one negative (V_n). In order to draw a full image on the screen, the pixels of the matrix have to be turned on sequentially, [20]. The main problem in the PMOLED technology is that, when line N is turned on, line (N − 1) is turned off, and the pixels on that line do not have a way to store their charge, so they will be turned off. An active matrix addressing scheme is used in AMOLED displays: the electrodes supply all the pixels at the same time, and the on/off state of each pixel is controlled by a matrix of thin-field transistors (TFTs). Fig.5.3(a) shows the conceptual representation of an AMOLED panel. Fig.5.3(b) shows the simplified schematic diagram of an AMOLED pixel: V_p and V_n are the positive and negative supply lines, and the voltage V_{cont} at the gate of the TFT controls the on/off state of the pixel. A storage capacitor C_{st} is included in order to maintain the state of the pixel when the line is turned off, [21]. Although PMOLED displays are cheaper to produce, the lack of a storage element in the pixel leads to the overall need of more brightness than AMOLEDs to achieve the same quality of the image. More brightness means that an higher voltage needs to be applied, and this can degrade the lifetime of the screen. Another issue of PMOLED displays is the refresh rate, which is limited when compared to the AMOLED case. These are the main reasons why AMOLED technology is the only dominant OLED technology for all the high-resolution displays (smartphones, smartwatches, tablets, TVs), while the use of PMOLED is limited to smaller, low-resolution displays (smartbands for example), [22]. As mentioned,

each pixel of an AMOLED display needs three different voltages to be turned on, depending on the particular display considered: $\sim +5$ V for the positive supply (V_p), $\sim -4/-6$ V for the negative supply (V_n), and typically $+7$ V at the gate of the TFT to turn on a particular pixel. The typical Li-Ion battery of a smartphone provides a single voltage ranging from 2.4 V to 4.9 V. In order to generate the three supply voltages in AMOLED displays, the conventional solution is to employ three separate DC-DC converters are used. The use of three separate DC-DC converters implies that three inductors and at least three filter capacitors need to be implemented. As discussed in the previous sections, inductors are, again, the most critical components to integrate in the system, due to theyr cost and size. This issue becomes even more relevant when dealing with portable devices, where having three separate inductors only to power up the display becomes costly. A solution that reduces the number of inductors will result in benefits for chip cost and area.

5.2   Single-Inductor-Multiple-Output DC-DC

Single-Inductor-Multiple-Output (SIMO) DC-DC converters are a particular category of switching DC-DC converters that can provide two or more output voltages using only one inductor. The different outputs are obtained by multiplexing the inductor current between the different output loads. An example of a dual-output boost converter is shown in Fig. 5.4 (a). The multiplexing operation is done by the two independently controlled switches, SW_2 and SW_3. The energizing cycle can be done in two different ways. The different energy flows are shown in Fig. 5.5, assuming the presence of only two loads. The first way is to have multiple energizing cycles per switching period, as in Fig. 5.5(a): the switching period T gets divided into more subperiods. Each subperiod experiences a charge/discharge cycle. It is obvious that in order to achieve different outputs the different charge/discharge cycles must be different. In the figure: D_1 is the first charge of the inductor, D_2 the discharge into the first load, D_3 is the second charge, and D_4 the discharge into the second load. The second way to drive multiple outputs is to charge the inductor enough to feed all the outputs, then discharge sequentially into each of the output loads, as shown in Fig. 5.5(b). D_1 is the charging duty cycle, D_2 the discharge into the first output, D_3 the discharge into the second output. The concept is here shown for two outputs but can be extended to have N outputs. SIMO converters can suffer from cross regulation problems: the discharge of the inductor current into one output may not be not properly completed when it is time to either recharge or discharge into the next load. This will cause the second output to
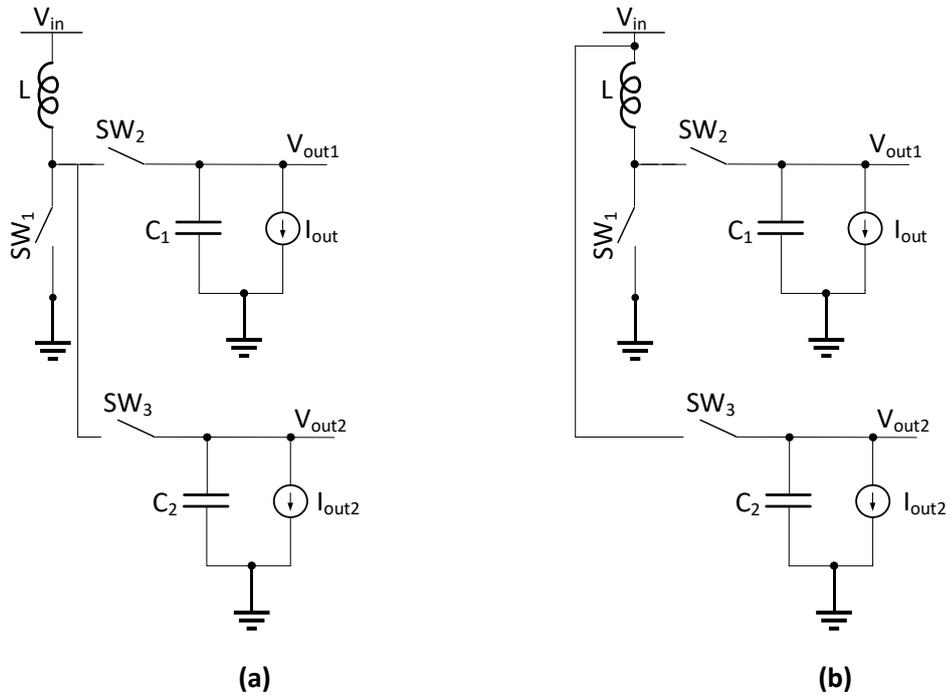
Figure 5.4: Schematics of SIMO boost converters with: a) unipolar outputs and b) bipolar outputs.

have a value different from the desired one. So, for instance, a voltage variation in the first output may cause a variation in the charge/discharge cycle, changing the value of the second output too. This problem can be mitigated by using the converter in DCM or Pseudo-CCM, [23]. Notice that if, instead of connecting both the outputs to the same inductor terminal, the second output switch is connected to the complementary terminal of the inductor, the output voltage on the second output will be negative. DC-DC SIMO converters of this kind are usually called Single Inductor Bipolar Outputs (SIBO) converters. Fig. 5.4 (b) shows an example of a boost SIBO converter. When V_{out2} needs to be charged, SW_1 and SW_3 are open, while SW_2 and SW_4 are closed. The inductor current, which can not change its direction, is actually discharging the second load, bringing its voltage to a negative value.
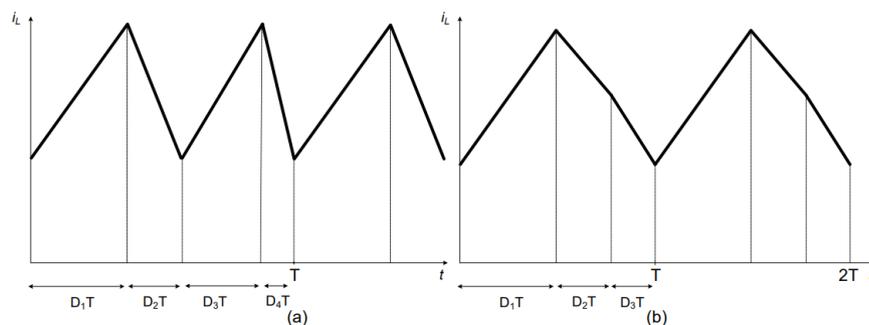
Figure 5.5: Inductor current in SIMO DC-DC converters: a) multiple energizing cycles per switching period, b) one energizing cycle per switching period.
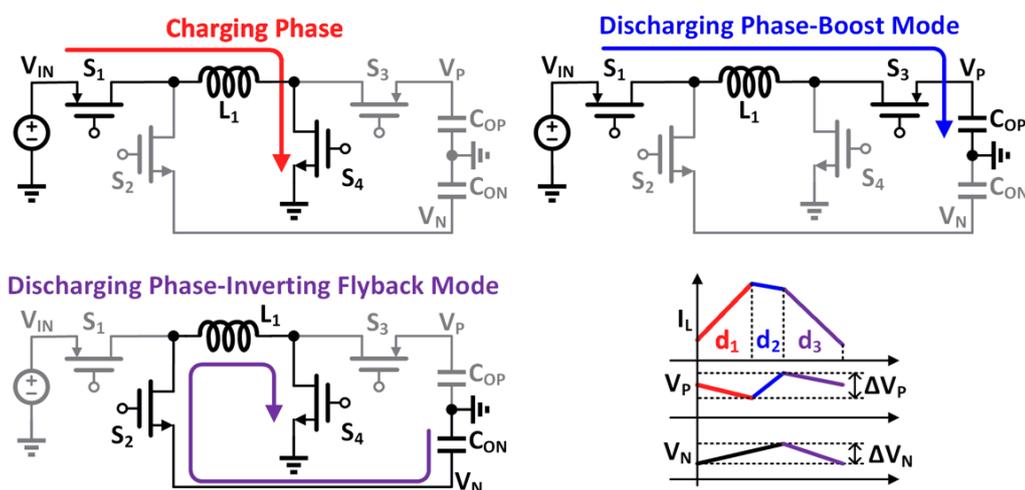
Figure 5.6: Conventional SIBO converter with a three-phase operation scheme and its relevant waveforms.

5.3 Previous Art

[24] and [25] are two conventional solutions that integrate on a single chip two separate dc–dc converters, one boost converter and one inverting flyback converter, to provide the bipolar supply rails. As expected, conventional solutions benefits from the short time-to-market but the two power inductors negatively affect the chip cost and area. Several SIBO converters emerged in recent years [26–33] to shrink the device size and lower the cost. In [26–30],

the SIBO converters operate with three phases, as shown in Fig. 5.6. V_P is charged with boost mode, and V_N is charged with inverting flyback mode, respectively. Compared to the SIBO converter operated with two phases and charging V_P and V_N simultaneously with inverting flyback mode [31], the inductor current ripple can be reduced and the efficiency can be improved. Similar to the ordered power distributive control (OPDC) in single-inductor multiple-output (SIMO) converters [34,35], the SIBO converter shown in Fig. 5.6 uses a comparator to regulate V_P with a higher priority, while uses a PI controller to regulate V_N. OPDC has the advantages of a fast transient response and no cross-regulation for V_P, both of which are quite favorable for the AMOLED displays. However, this control scheme results in a positive voltage ripple larger than the negative one, which is not the best for AMOLED displays. In [32], a current-mode pulse-width modulation (PWM) controller regulates the positive output. Thus, improving the line and load regulations of this SIBO converter. However, the transient response severely degrades, and the measured undershoot/overshoot can be as large as 292 mV/430 mV when a load transient happens. Finally, the regulation of the negative output in [32] requires a temporary phase that decreases or increases the energy delivered to the positive output, causing a cross-regulation issue.

5.4 Circuit Description

To overcome the drawbacks from prior arts, the proposed solution is a hybrid SIBO converter with floating negative output and shunt regulators [33] to keep the positive voltage fixed. In the design, the shunt regulators only deal with a tiny portion of the total ripples and consume low power, reducing the output positive ripple and improving the transient response. In the proposed topology, most of the output variations are pushed towards the floating negative output. Having low ripple and low line transients on the positive output is a key specification when driving AMOLED displays, as the positive voltage is responsible for controlling the TFT gate, so the turn on/off of the pixel. Sudden variations on the positive voltage, which can be caused for example by external disturbances like an incoming call, can cause image flickering on the screen if not properly addressed. The proposed SIBO converter may be suited to supply AMOLED displays up to 7 inches (such as smartphones or small tablet screens), as it can provide more than 200 mA of current to the output when its input voltage is higher than 3 V.

Figure 5.7: System architecture of the proposed hybrid SIBO converter with floating negative output.

5.4.1 Working Principle

Fig. 5.7 shows the proposed hybrid SIBO converter's system architecture with floating negative output and shunt regulators. It includes four power transistors, S_1–S_4, one off-chip Schottky diode, D_1, one power inductor, L_1, one flying capacitor C_{FLY}, one output capacitor, C_O, and one filtering capacitor, C_{OP}, for the positive output, V_P. As shown in Fig. 5.7, all the power transistors, buffers, and control circuits are integrated on the chip. Unlike previous works [24–31], only the positive output V_P has an output capacitor C_{OP} serving as an anchor while the nodes V_N, V_{X1}, and V_{X2} are floating. As V_N is floating, the three-phase operation scheme, which means charging the two outputs separately, is not needed here. Therefore, a two-phase operation scheme is used, with the circuit being charged and discharged as if it had a single output. The main output capacitor C_O stabilizes the differential voltage V_P-V_N, and V_P is set with the anchor capacitor C_{OP} and with the shunt regulators. With these adjustments, V_N will be automatically regulated, and since V_P is fixed by the shunt regulators, all the variations will be pushed to V_N.

Fig. 5.8 shows the charging and discharging phases of the proposed SIBO converter. In the figure, R_L represents the AMOLED pixel array. V_{X1}, V_{X2},

Figure 5.8: (a) Charging phase and (b) discharging phase of the proposed SIBO converter. (c) SIBO converter with C_{PN} and (c) its waveforms.

and V_{X3} are the switching nodes. During the charging phase, Fig.5.8(a), the capacitor C_{FLY} is charged, thus the inductor is energized. In the discharging phase, Fig.5.8(b), all the circuit nodes, except V_P, are floating. If the parasitic capacitors are not considered, all the inductor current I_L will flow into C_O and establish $V_P - V_N$ directly, with no current flowing into or out of C_{OP}. Therefore, C_{OP} operates as an anchor capacitor defining the voltage of V_P. Ideally, there should be no voltage variation on V_P. Fig. 5.8(c) plots the relevant waveforms of the two phases, and the ideal equations for the ripples of V_P and V_N are:

$$\Delta V_P \approx 0 \tag{5.1}$$

$$\Delta V_N \approx \frac{d_1 \cdot T \cdot I_{OUT}}{C_0} \tag{5.2}$$

In practice, a parasitic capacitor C_{PN} is present on the node V_N, as highlighted in Fig. 5.9. This parasitic capaitor C_{PN} is in series with C_{OP}, and then in parallel with C_O, providing another current path. Therefore, the voltage variation on C_O is distributed to V_P and V_N , according to the C_{PN}/C_{OP} ratio. This issue can be easily solved by setting C_{OP} to be thousands of times
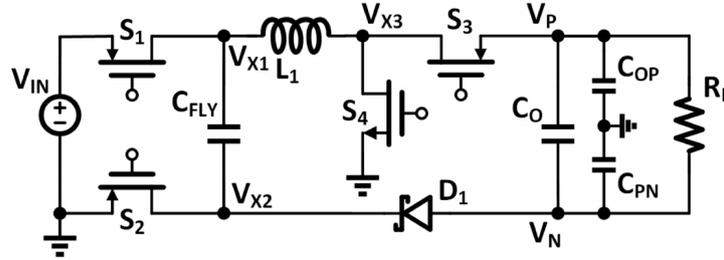
Figure 5.9: SIBO converter with C_{PN}.
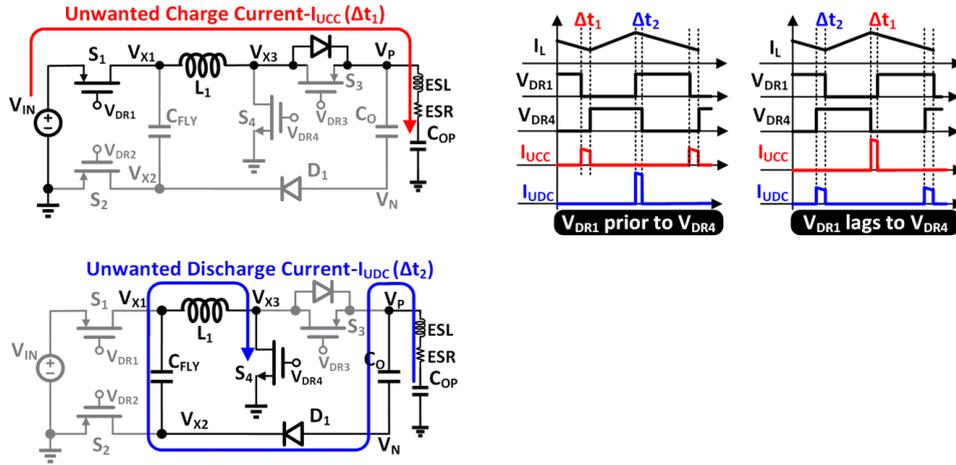
Figure 5.10: Circuit configurations when (a) unwanted charging current and (b) unwanted discharging current happens, and (c) relevant waveforms when V_{DR1} is prior to or lags to V_{DR4}.

larger than C_{PN}, making, therefore,V_P almost zero.

The flying capacitor C_{FLY} has also the functions of both reducing the inductor current ripple in this two-phase operation (which would otherwise be much larger than the three-phase case), and reducing the voltage stress across the power switching, allowing the use of a standard 5-V CMOS process, and increasing the power efficiency. Besides, a cross-coupled bootstrap-based level-shifter (CCBB-LS) and a dual-PMOS inverter buffer are implemented, in order to avoid the need for the deep N-well.

5.4.2 Unbalanced Charge Injection of C_{OP}

Besides the C_{PN}-caused V_P ripple mentioned before, there are three other mechanisms that may cause charge to unbalance on C_{OP}, resulting in V_P variations, and therefore require extra attention.

1) C_{OP} Charge Injection from Switch Timing Mismatch: during the transition between the two phases, it is impossible to turn ON/OFF S_1, and S_4 simultaneously, due to the control circuit and buffers' delay mismatches. The delay on S_2 is not relevant, as S_2 turns on slightly later, and turns off slightly earlier, than S_1 remaining off during the phase transitions. Therefore, the synchronization issue is limited to the timing of S_1 and S_4. Fig. 5.10 exhibits the unwanted charge or discharge currents to C_{OP}, when there are timing mismatches between S_1 and S_4. During Δt_1, S_1 is ON, and S_4 is OFF. The unwanted charge current I_{UCC} flows from V_{IN} into C_{OP} through the body diode of S_3, causing unexpected voltage variation on V_P. Similarly, the unwanted discharge current I_{UCDC} flows from the output to ground during Δt_2, with S_1 being OFF and S_4 being ON. When V_{DR1} is leading V_{DR4}, I_{UCC} appears during the transition from the discharging phase to the charging phase, and I_{UCDC} occurs during the charging to discharging phase transition. When V_{DR1} lags behind V_{DR4}, it is the other way around. As Δt_1 and Δt_2 are much smaller than the switching period, then $I_{UCC} \approx I_{VALLEY}$ and $I_{UCDC} \approx I_{PEAK}$, where I_{VALLEY} and I_{PEAK} are the valley and peak values of I_L , respectively. The C_{OP} charge injection caused by I_{UCC} and I_{UCDC} in each cycle, ΔQ_1, becomes:

$$\Delta Q_1 \approx \Delta t_1 I_{VALLEY} - \Delta t_2 I_{PEAK} \tag{5.3}$$

ΔQ_1 can be positive or negative, and accumulates over cycles, causing V_P voltage ripple and dc voltage shift. To minimize $|\Delta Q1|$, an additional synchronous control loop is implemented. This loop considers the S_1 gate-drive signal V_{DR1} as a reference, to generate the gate-drive signal for S_4. Then, in the steady state, V_{DR4} synchronizes with V_{DR1}. It will be explained in more details in the next section.

2) C_{OP} Charge Injection From the Parasitic Capacitors: besides the timing mismatches between S_1 and S_4, the parasitic capacitors at the switching nodes will also cause charge injection to C_{OP}. In Fig.5.11 the three considered switching nodes V_{X1}, V_{X2}, and V_{X3} are highlighted along with their respective parasitic capacitors: C_{P1}, C_{P2}, and C_{P3}. During the phase transition from charging phase to discharging phase, V_{X1} switches from V_{IN} to (V_{IN} +V_N - V_{D1}), V_{X2} switches from the ground to V_N - V_{D1}, and V_{X3} switches from the ground to V_P, respectively, where V_{D1} is the D_1 diode voltage drop. There will be a charge transfer between the parasitic capacitors and C_{OP} during these
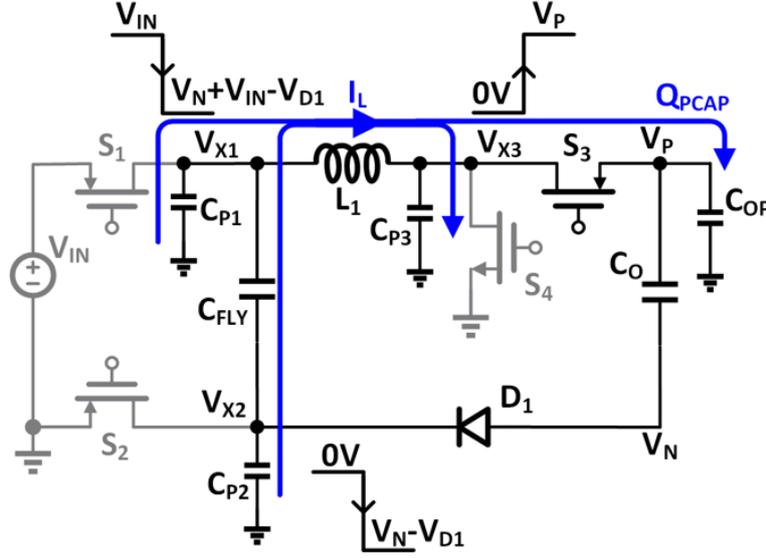
Figure 5.11: Charge injection of C_{OP} caused by the parasitic capacitors of the switching nodes.

phase transitions. The amount of injected charge ΔQ_2 on C_{OP} in each cycle is equal to the sum of the three contributions from each parasitic capacitor:

$$\Delta Q_2 = (C_{P1} + C_{P2})|V_N - V_{D1}| - C_{P3}V_P \tag{5.4}$$

In this design, $(C_{P1} + C_{P2})$ is estimated around 275 pF and C_{P3} are around 168 pF. With these values, ΔQ_2 is positive. Furthermore, the resulting ripple on V_P is $\Delta Q_2/C_{OP}$, which is lower than 0.5 mV, considering a C_{OP} of 1 μF. In the same way as ΔQ_1, ΔQ_2 also accumulates over cycles.

3) C_{OP} Charge Injection From the Gate-Drivers and Control: from Fig. 5.12, the third source of V_P variation derives from sourcing and sinking the gate-drive currents. Fig. 5.12 shows the details of the interested circuits and relative current. As shown in the figure, V_P is used to supply the control block and the gate-drive buffers of S_3 and S_4, by sourcing current I_1. Furthermore, V_P also sinks current I_2 from the gate-drive buffer of S_2. The total C_{OP} charge injection, ΔQ_3, caused by I_1 and I_2 in each cycle is:

$$\Delta Q_3 = \int_0^T (I_2 - I_1)\, dt \tag{5.5}$$

Since the total size of S_3 and S_4 is several times larger than S_2, and as the
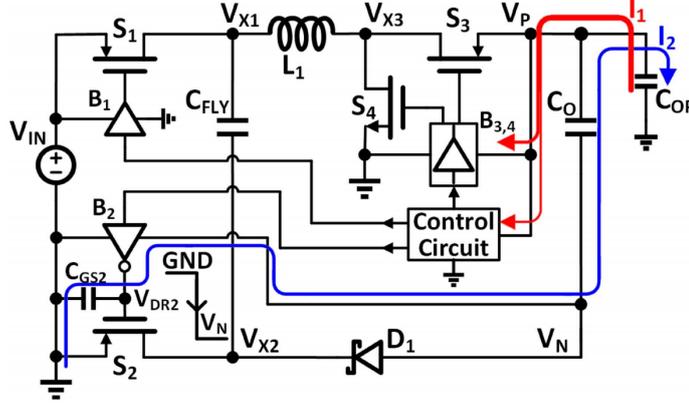
Figure 5.12: Charge injection of C_{OP} caused by the supply current of the control circuit and buffers.

current consumption of the control block is much smaller than the gate-drive currents, ΔQ_3 will result to be negative. Considering all the three contributions just described, the total C_{OP} charge injection in one cycle, ΔQ_T, is equal to:

$$\Delta Q_T = \Delta Q_1 + \Delta Q_2 + \Delta Q_3 \tag{5.6}$$

To minimize $|\Delta Q_1|$, an additional synchronous control loop is implemented. This loop considers the S_1 gate-drive signal V_{DR1} as a reference, to generate the gate-drive signal for S_4. Then, in the steady state, V_{DR4} synchronizes with V_{DR1}. The implementation of this control is discussed later on in more detail. As the synchronous driver minimizes ΔQ_1, ΔQ_T is mainly determined by ΔQ_2 and ΔQ_3, both of which are tightly related to the power transistor sizes. In this design, $|\Delta Q_3| > |\Delta Q_2|$, and therefore ΔQ_T is negative, suggesting that the supply V_P should need a small auxiliary shunt regulator, which will be discussed next.

5.4.3 Charge Compensation and Output Voltage Regulation

Fig. 5.13 presents the converter with the addition of a fast response shunt regulator, designed to compensate for the C_{OP} charge injection. As V_{IN} is provided by a Li-ion battery, it ranges from 2.7 to 4.5 V, hence is lower than V_P. Therefore, the shunt regulator cannot directly supply current to V_P from V_{IN}. For this reason, the voltage-controlled current source I_{SR} is connected to the left side of L_1, instead of being connected to V_P directly. In the SIBO converter
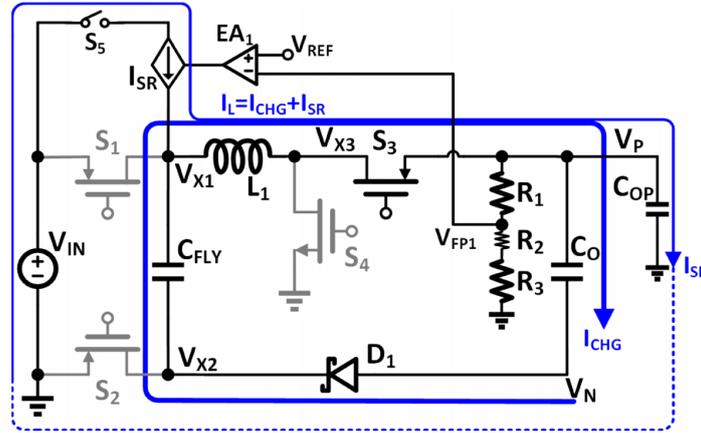
Figure 5.13: Proposed solution for the C_{OP} charge compensation and $V_P$voltage regulation.

discharging phase, the switch S_5 turns on, I_{SR} flows through L_1, S_3, C_{OP}, ground, and V_N, forming a closed loop. In the other current loop, I_{CHG} charges C_O and provides power to the load. The sum of I_{SR} and I_{CHG} equals the inductor current I_L. Here, it is worth to note that I_{SR} is only a small portion of I_L and will not affect the power delivered to the load. the additional switch S_5 is OFF during the charging phase, ensuring that I_{SR} is zero during that phase. To keep V_P steady at 5 V, the current source I_{SR} alone is not enough. As Fig. 5.7 shows, besides I_{SR}, there is a current sink I_{SK} connected to V_P preventing V_P of being overcharged, which is an event that occurs especially during the startup process. In Fig. 5.7 , the error amplifier EA_1 controls I_{SR}, targeting a V_P of 5.3 V. When V_P is overcharged, the current sink I_{SK} controlled by EA_2 will pull V_P back to 5.33 V quickly. It is worth mentioning that since V_P also provides currents to the controller and gate drivers, it will also be pulled down below 5.3 V slowly by those currents. A small resistor R_2 inserted between R_1 and R_3 that generates a 30-mV offset for EA_1 and EA_2 avoids I_{SR} and I_{SK} to conduct simultaneously. As the shunt regulators controls V_P, then, as mentioned, the voltage across C_O determines V_N . Therefore, regulating V_N means regulating the total output voltage, V_P- V_N. To this end, this circuit uses a typical voltage-mode type-II PWM controller.
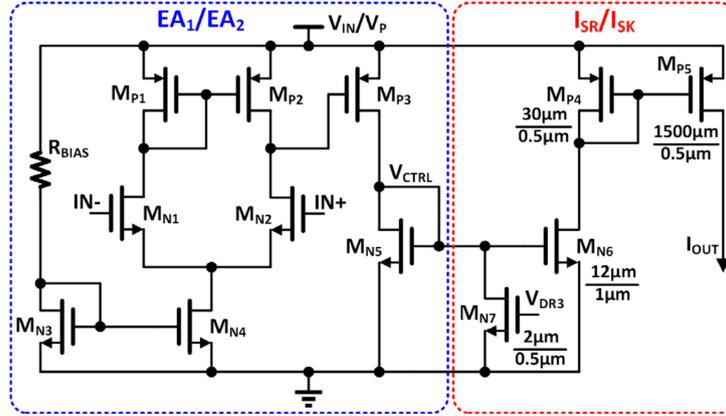
Figure 5.14: Schematic of EA_1 orEA_2 and a current mirror output stage driving I_{SR} or I_{SK}.
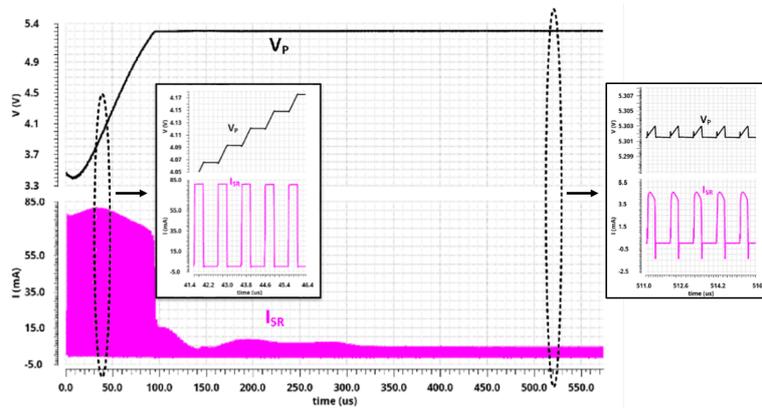
Figure 5.15: Simulated regulation process of V_P when $V_{IN} = 3.7$ V and $I_{LOAD} = 100$ mA.

5.5 Circuit Implementation

5.5.1 Shunt Regulators

Fig.5.14 illustrates the schematic of the error amplifiers, EA_1 and EA_2, and the current mirror output stage driving the current source/sink, I_{SR}, and I_{SK}, respectively. V_{IN} supplies EA_1 and I_{SR}, while V_P supplies EA_2 and I_{SK}. In this design, M_{N7} is a small-sized transistor that performs the function of S_5, cutting off the current mirror output stage, hence disabling I_{SR} during the
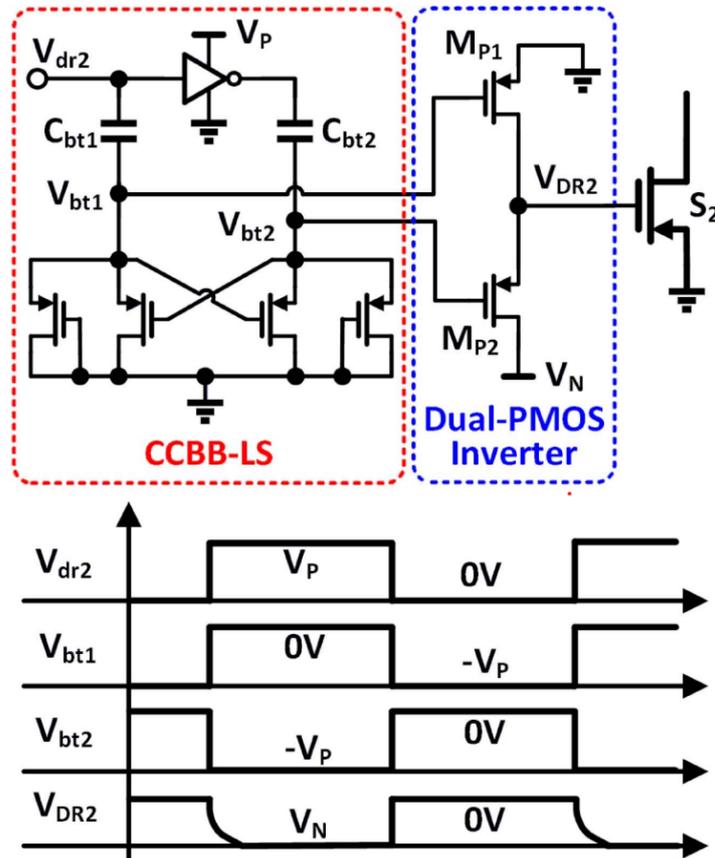
Figure 5.16: Schematic of the CCBB-LS and the dual-PMOS inverter buffer, and the voltage waveforms.

SIBO converter charging phase. M_{P5} in Fig. 5.14 is the output transistor, and a current ratio of 50:1 with M_{P4} is selected to provide a high enough compensation current in each cycle with an acceptable silicon area. Fig. 5.15 plots the simulated regulation process of V_P when $V_{IN} = 3.7$ V and $I_{LOAD} = 100$ mA. In the start-up, V_P is much smaller than the targeted 5.3 V, so I_{SR} is larger, increasing V_P rapidly. As V_P gets close to 5.3 V, I_{SR} drops quickly. When the shunt regulator reaches stability, V_P is fixed at 5.3 V and I_{SR} is small.

Figure 5.17: Block diagram of the synchronous driver for S_4.

5.5.2   CCBB-LS and Dual-PMOS Inverter Buffer

The control signal of the power PMOS S_2 must be a negative voltage for the turn on and zero for the turn off. A level shifter is needed to provide the correct control signal Fig. 5.16 presents the designed cross-coupled bootstrap-based level shifter (CCBB-LS) with a dual-PMOS inverter buffer B_2 at the output, in order to alleviate the device voltage stress and eliminate the need for DNWs. The CCBB-LS supplied by V_P generates differential driving signals, V_{bt1} and V_{bt2}, swinging from -V_P to 0 V. Besides, the gate-drive buffer with two P-type transistors, M_{P1} and M_{P2}, can drive the large power transistor S_2, reducing the required bootstrap capacitance ($C_{bt1} = C_{bt2} = 20$ pF are integrated on chip in this work). When V_{DR2} swings from 0 V to V_N , the V_{GS} of M_{P2} keeps decreasing, and the falling edge is relatively slow. Since S_2 is only used to charge C_{FLY}, which is a hard-charging process, the slow turn on does not affect the power efficiency. As mentioned, with this structure there is no need of using high-voltage (HV) devices nor DNWs.

5.5.3   Synchronous Driver for S_4

Fig. 5.17, shows the block diagram of the synchronous driver for S_4. It consists of two delay-locked loops (DLLs): the upper loop is for the turn on timing tuning and the lower loop is for the turn off timing tuning. During the operation,the turn on and turn off timing of S_1 and S_4 is detected by the ON/OFF-detection blocks. After detection, the signal is compared by the phase detectors (PDs). Then, the charge pumps (CPs) integrate and convert the phase

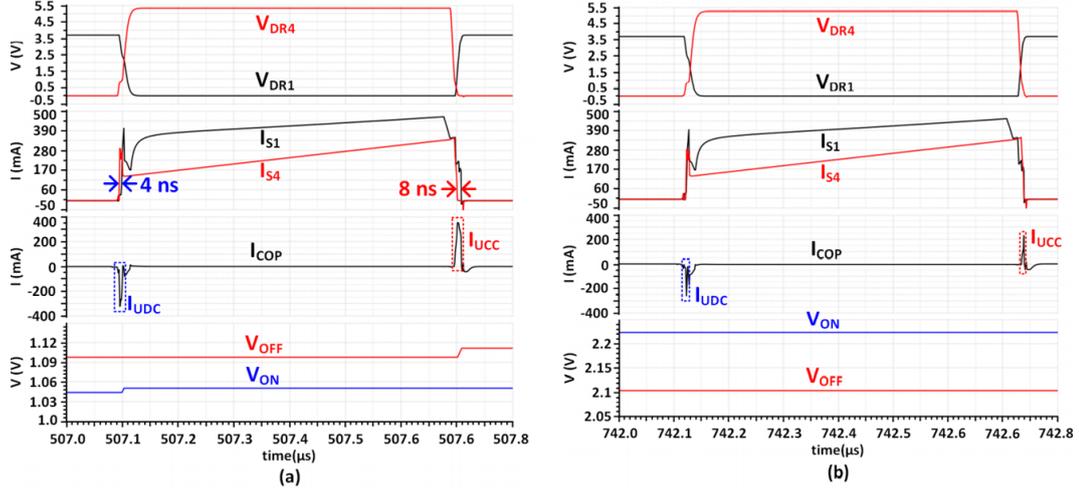**Figure 5.18:** Simulated waveforms of the synchronous driver (a) before the steady state and (b) in the steady state when $V_{IN} = 3.7$ V and $I_{LOAD} = 100$ mA.

differences to the analog control voltages, V_{ON} and V_{OFF}, and feed them to the voltage-controlled delay lines (VCDLs), to match the delays of the rising edge and falling edge of V_{dr4} accordingly, achieving a synchronized V_{DR4}. The synchronous driver and the buffer B_1 are supplied by V_{IN}, while the buffer B_4 is supplied by V_P. As $V_{IN} < V_P$, a level shifter is added to connect the synchronous driver and B_4. Fig. 5.18 (a) plots the simulated waveforms before the proposed gate drivers get synchronized, where I_{S1} and I_{S4} are the currents flowing through S_1 and S_4, respectively, and I_{COP} is the current flowing into C_{OP}. In the figure, by observing the rising/falling edges of I_{S1} and I_{S4}, the exact turn on/turn off timing of S_1 and S_4 can be determined. The rising edge of I_{S4} anticipates the rising edge of I_{S1} by 4 ns, and the falling edge of I_{S4} anticipates that of I_{S1} by 8 ns. As a result, the current I_{UCDC} is present when S_4 is turned on, and S_1 is off,while I_{UCC} is present when S_4 turns off, and S_1 is on. The control voltages for VCDL, V_{ON}, and V_{OFF} are then charged up by a small step to delay the rising and falling edges of V_{DR4}, respectively. When the synchronous gate driver of S_4 reaches stability, V_{DR1} and V_{DR4} are synchronized. As shown in Fig. 5.18 (b), the rising and falling edges of I_{S4} are almost coincident with the ones of I_{S1}. The narrow pulse of I_{UCDC} and I_{UCC} shows that V_{DR1} and V_{DR4} are not perfectly synchronized (due to some mismatch in the ON-/OFF-detection circuit). Nonetheless, the reduction in
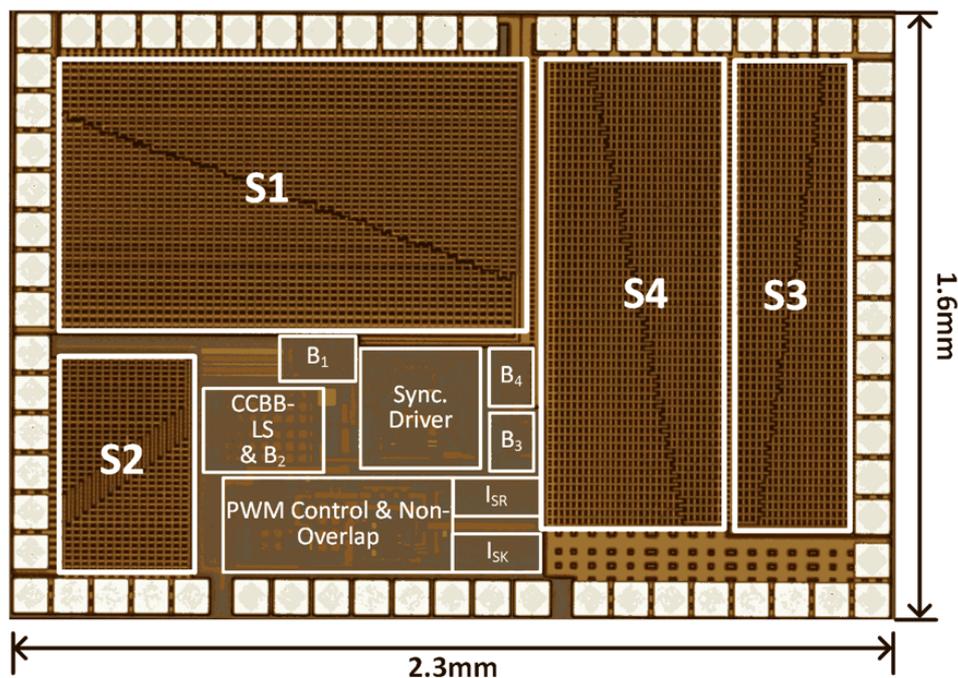
Figure 5.19: Chip micrograph of the proposed SIBO converter.

the current pulse with respect to what is seen in Fig.5.18(a), indicates that ΔQ_1 in 5.6 is being minimized.

5.6   Measurement Results

The proposed hybrid SIBO converter was fabricated in a 0.35-μm CMOS process with 5-V devices. Fig. 5.19 shows the chip micrograph of the SIBO converter. The total chip area is equal to 3.68 mm^2. The described shunt regulator only occupies 0.035 mm^2 of the total area. The circuit operates with a switching frequency equal to 1 MHz. The power inductor is equal to 10 μH, the flying capacitor is 4.7 μF, C_O is 10 μF, and a C_{OP} is 1 μF. The input voltage range for this SIBO converter ranges from 2.7 to 4.5 V. The targeted V_P and V_N are 5.3 and -4.7 V, respectively. Fig. 5.20 shows the measured waveforms with 3.7-V input and load currents of 30 mA (a) and 350 mA (b). The waveforms were measured with a voltage probe with a bandwidth of 20 MHz. Besides the small ringing glitches observed during the phase transition, probably caused by the probe loop inductance, the voltage ripples on V_P are always lower than
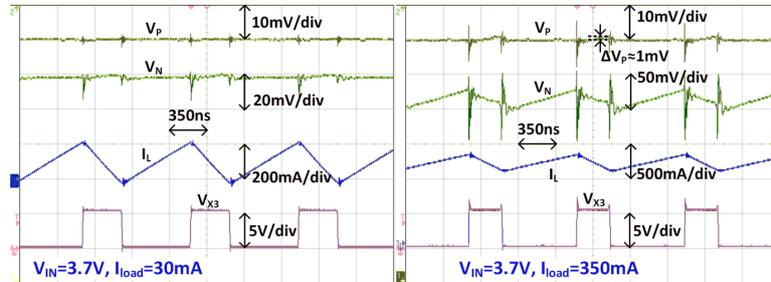
Figure 5.20: Measured waveforms of V_P, V_N, I_L, and V_{X1} when $V_{IN} = 3.7$ V, and $I_{LOAD} = 30$ mA and $I_{LOAD} = 350$ mA.
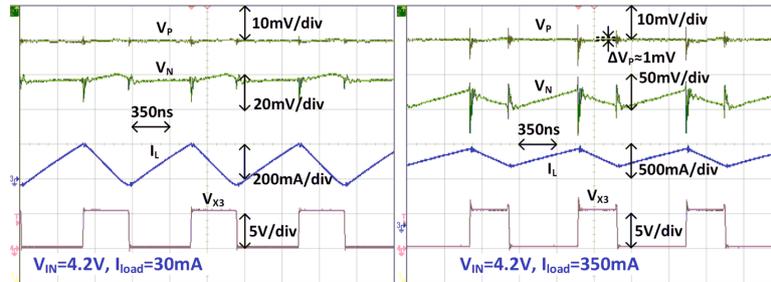

Figure 5.21: Measured waveforms of V_P, V_N, I_L, and V_{X1} when $V_{IN} = 4.2$ V, and $I_{LOAD} = 30$ mA and $I_{LOAD} = 350$ mA.

1 mV for all the load current range from 30 to 350 mA. The ripples on V_N are the expected overall output voltage ripple of the bipolar outputs related to the load current. The maximum observed ripple on V_N is equal to 30 mV in the heavy load condition. Fig. 5.21 displays the same measurements, but with a 4.2-V input voltage. Also in this case, the ripple on V_P is negligible, and the ripple on V_N is around 30 mV. Fig. 5.22 shows the measured load transient response when I_{LOAD} varies between 30 and 350 mA, with a slope of 250 mA/μs. Due to the floating negative output topology and the fast response shunt regulator, the undershoot voltage on V_P is only 3 mV, and the overshoot voltage is unnoticeable, as most of the output variations are migrated to V_N. Fig. 5.23 exhibits the measured power conversion efficiencies with different input voltages and load currents. The measured peak efficiency is 89.3% when the input voltage is 4.5 V, and the load current is 100 mA. In this condition, the output power is equal to 1.1 W. The measured efficiency remains above 80% even at the 30-mA light load condition, proving that the shunt regulators do not introduce significant conduction losses. Table 5.1 compares the pro-
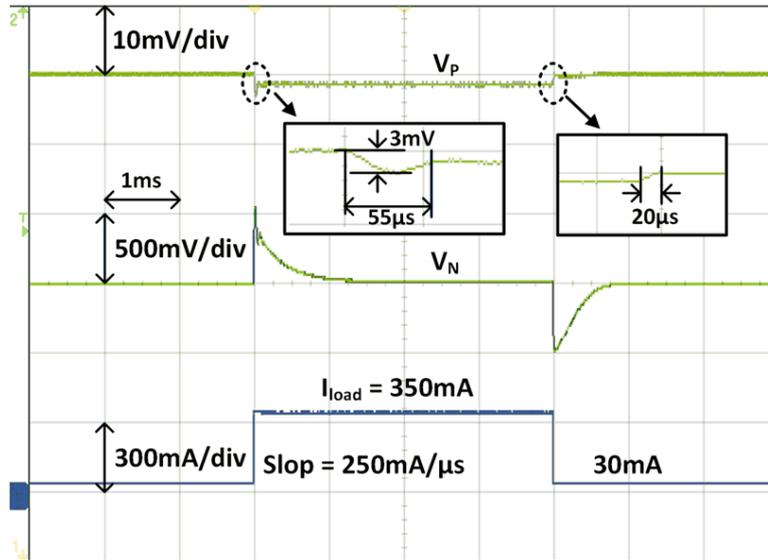
Figure 5.22: Measured load transient waveforms with $V_{IN} = 4.2$ V

posed SIBO converters with the prior works. By only using 5-V devices, this work achieves the highest output power with a small chip area. The resulting ripple on V_P is negligible and the total ripple on the bipolar outputs is the smallest, with smaller filtering capacitors.

Figure 5.23: Measured power conversion efficiencies as a function of the load current for different input voltages.

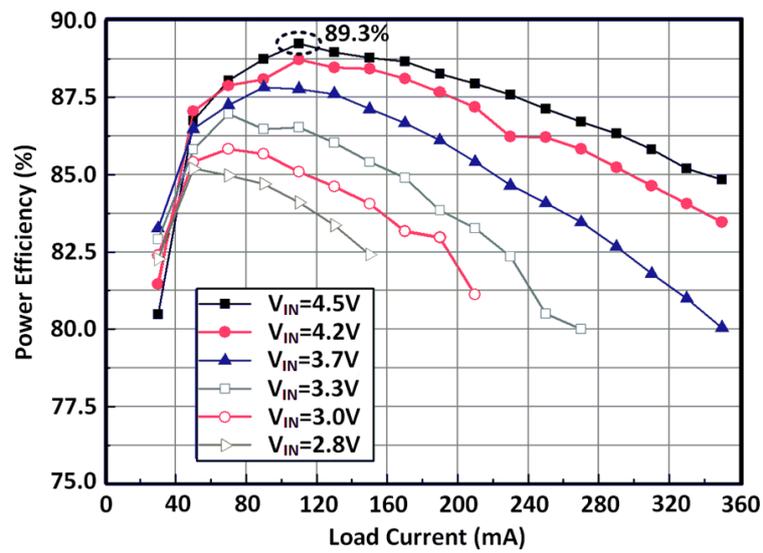|	[26]	[27]	[28]	[29]	[30]	This Work
Process	0.5 μm Power BiCMOS	0.5 μm BCD	0.5 μm BCD	90 nm 8V devices	0.18 μm BCD	0.35 um 5V devices
Chip Area (mm^2)	4.1	5.75	7	N/A	1.16	3.68
Frequency (MHz)	1	1.25	1.25	0.5	1.5	1
Inductor (μH)	4.7	4.7	4.7	N/A	N/A	4.7
Flying Cap (μF)	4.7	4.7	4.7x2	N/A	N/A	4.7
Max. Eff.	82.3% @ 0.33 W	87.1% @ 0.6 W	89% @ 0.6 W	90.1% @ 0.11 W	88% @ 0.6 W	89.3% @ 1.1 W
Input Range (V)	2.7-4.5	2.7-4.5 & 5	2.7-3.7	3.0-4.2	2.54.5	2.7-4.5
Max Power (W) @Vin = 3.7 V & Eff>80 %	0.5	2.4	2.6	0.22	1.4	3.5
Output Voltage (V) (V_P / V_N)	4.58 / -6.24	4.6 / -5.4	4.6 / -5.4	4.8 / -2.5	5 / -5	5.3 / -4.7
Output Cap (μF)	4.7+4.7	10+10	10+10	10+10	4.7x34.7x3	10+1
Line Regulation (mV/V) (V_P / V_N)	6 / 18	13.8 / 7.6	15.6 / 9.7	1.25 / 2.5	N/A / N/A	18 / 2
Load Regulation (8mV/mA) (V_P / V_N)	0.25 / 1	0.12 / 0.2	0.27 / 0.35	0.03 / 0.06	N/A / N/A	0.1 / 0.06
Output Ripple (mV) @	@100 mA	@300 mA	@200 mA	@20 mA	@60 mA	@30-350 mA
Output Ripple (mV) (V_P / V_N)	80** / 30**	50 / 60	80 / 65	17 / 50	20 / 20	1 / 30

*: Capacitors in compensation network are not included.
**: Ripples at heavy load condition estimated from measurement waveforms.

Table 5.1: Comparison between the proposed solution and previous works.

Conclusions

This thesis presented two switching DC-DC Converters for different target applications. Although the target of the two converters is different, for both applications (and, more in general, for switching DC-DC applications) the inductor is the main cause of waste of money and area. Each solution aims, in different ways, to reduce the impact on cost and area that the inductor has on the chip.

The first DC-DC converter was researched in collaboration with Infineon technologies and targets a high switching frequency for Post-Regulated Automotive applications in order to reduce the size of the inductor. In order to avoid using high voltage MOSFETs, a stacked power stage structure is proposed. The issues that arise from the internal voltage bias generation and of the parasitic bonding inductance are analyzed and mitigated as much as possible. Two different control strategies for this converter are presented: a more innovative One Cycle control, which integrates the switching voltage to generate a reset pulse for the PWM wave, and a more traditional Feed Forward control, integrating the input voltage to generate the sawtooth wave. Both solutions work at a fixed frequency, which is preferable for automotive applications. The chip with two layout versions of the power stage and the two control strategies has been fabricated and is currently undergoing measurements. Preliminary measurements show that the circuit is functional at 50 and 100 MHz. However, unwanted parasitic effects degrading the output load regulation, hence the efficiency. More accurate measurements and improvements to the setup which are currently ongoing are expected to improve the observed performance of the chip. Nonetheless, the circuit is promising and the research on the topic of high frequency is expected to continue. As mentioned in Chapter 2, a more realistic solution for a product could be re-optimizing the sizes of the power stage for lower frequencies (which would still be much higher than the usual 1-2 MHz of regular DC-DC). This would still have the benefit of reducing the inductor size, and would have a lower impact on the efficiency than the extreme 100 MHz case.

The second converter presented in thesis was developed in collaboration with the University of Macau. It consists a hybrid SIBO converter with a floating negative output voltage for high-quality AMOLED displays. With the SIBO topology, one inductor instead of two can be used for the supply of two outputs. AMOLED displays have more stringent requirements on its positive supply than the negative supply. That is because the positive supply affects the V_{GS} of the pixel current source, hence decides if the pixel is ON or OFF, while the negative only determines the V_{DS} of the current source. With careful considerations on the charge injection to the positive output, a shunt regulator regulated the positive output voltage, while a voltage mode PWM controller is applied to regulate the negative output. The hybrid converter topology and the proposed CCBB-LS do not require HV devices nor DNW, which further helps reducing the chip area and cost. Measurement results verified the near-zero voltage ripple on the positive output and a fast load transient response. The peak power conversion efficiency is 89.3% with an output power of 1.1 W. The maximum output power is 3.5 W

Bibliography

[1] D. M. R. W. Erickson, *Fundamentals of Power Electronics.* Springer, 2001.

[2] J. X. F. Wang and B. Wang, "Comparison Study of Switching DC-DC Converter Control Techniques," in *2006 International Conference on Communications, Circuits and Systems*, check 2006.

[3] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, Jan. 2004.

[4] T. W. C. C. H. Hsu and C. L. Wey, "A voltage-mode hysteretic boost DC-DC converter with dual control modes," in *2012 Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*, check 2012.

[5] S.-C. Hsu, C.-J. Chen, and C.-J. Tsai, "A High Frequency Power and Area Efficienct Charge-Pump-Constant-On-Time Controlled DC-DC Converter Based on Dynamic-Biased Comparator with 50mV Droop and 2us 1% Settling Time for 1.15A/1ns Load Step," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, check 2019.

[6] *Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier*, International Rectifier, check. [Online]. Available: www.irf.com

[7] V. Kursun, S. Narendra, V. De, and E. Friedman, "Low-voltage-swing monolithic dc-dc conversion," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 5, pp. 241–248, 2004.

[8] M. Belloni, E. Bonizzoni, and F. Maloberti, "High efficiency dc-dc buck converter with 60/120-mhz switching frequency and 1-a output current," in *2009 Proceedings of ESSCIRC*, 2009, pp. 452–455.

[9] V. Kursun, G. Schrom, V. De, E. Friedman, and S. Narendra, "Cascode buffer for monolithic voltage conversion operating at high input supply voltages," in *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 464–467 Vol. 1.

[10] F. Neveu, B. Allard, C. Martin, P. Bevilacqua, and F. Voiron, "A 100 mhz 91.5% peak efficiency integrated buck converter with a three-mosfet cascode bridge," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 3985–3988, 2016.

[11] J. Järvenhaara, H. Herzog, S. Sipilä, J. Tian, I. Filanovsky, and N. Tchamov, "High speed dc-dc dead time architecture," *IEICE Electronics Express*, vol. 12, 10 2015.

[12] G. Schrom, P. Hazucha, J. Hahn, D. Gardner, B. Bloechel, G. Dermer, S. Narendra, T. Karnik, and V. De, "A 480-mhz, multi-phase interleaved buck dc-dc converter with hysteretic control," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 6, 2004, pp. 4702–4707 Vol.6.

[13] S.-C. Hsu, C.-J. Chen, and C.-J. Tsai, "A high frequency power and area efficienct charge-pump-constant-on-time controlled dc-dc converter based on dynamic-biased comparator with 50mv droop and 2us 1% settling time for 1.15a/1ns load step," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2980–2983.

[14] P. Li, R. Bashirullah, P. Hazucha, and T. Karnik, "A delay locked loop synchronization scheme for high frequency multiphase hysteretic dc-dc converters," in *2007 IEEE Symposium on VLSI Circuits*, 2007, pp. 26–27.

[15] Y. Lu, S. Suresh, and D. Czarkowski, "Integrated controller for a 100 mhz dc-dc switching converter," in *APCCAS 2008 - 2008 IEEE Asia Pacific Conference on Circuits and Systems*, 2008, pp. 1864–1867.

[16] K. Smedley and S. Cuk, "One-cycle control of switching converters," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, 1991, pp. 888–896.

[17] C. Huang and P. K. T. Mok, "A 100 mhz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, 2013.

[18] Y. Nakajima, T. Takei, G. Motomura, T. Tsuzuki, H. Fukagawa, M. Nakata, H. Tsuji, T. Shimizu, K. Morii, M. Hasegawa, Y. Fujisaki, T. Kurita, and T. Yamamoto, "Flexible amoled display using an oxide-tft backplane and inverted oleds," in *2014 IEEE Photonics Conference*, 2014, pp. 42–43.

[19] "Introduction to OLED Displays Design Guide for Active Matrix OLED (AMOLED) Displays by *4D Systems*," Online https://www.4dsystems.com.auy.

[20] S. Forrest, P. Burrows, and M. Thompson, "The dawn of organic electronics," *IEEE Spectrum*, vol. 37, no. 8, pp. 29–34, 2000.

[21] I. Pappas, S. Siskos, and C. Dimitriadis, *Active-Matrix Liquid Crystal Displays - Operation, Electronics and Analog Circuits Design*, 11 2009.

[22] "PMOLED vs AMOLED-what's the difference? by *OLED-info*," Online https://www.oled-info.com.

[23] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-ccm/dcm simo switching converter with freewheel switching," in *2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315)*, vol. 1, 2002, pp. 390–476 vol.1.

[24] "TPS65133: ±5-V, 250-mA Dual-Output Power Supply by *Texas Instruments*," Online https://www.ti.com/lit/ds/symlink/tps65133.pdf.

[25] S. Lee, J. Yoon, J. Kim, C. Lee, H. Jung, J. Lee, and J. Choi, "High-capacity dc-dc converters for active matrix oled display," in *2010 IEEE Asia Pacific Conference on Circuits and Systems*, 2010, pp. 480–483.

[26] C.-S. Chae, H.-P. Le, K.-C. Lee, G.-H. Cho, and G.-H. Cho, "A single-inductor step-up dc-dc switching converter with bipolar outputs for active matrix oled mobile display panels," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 509–524, 2009.

[27] S.-W. Wang, Y.-J. Woo, Y.-S. Yuk, G.-H. Cho, and G.-H. Cho, "High efficiency single-inductor boost/buck inverting flyback converter with hybrid energy transfer media and multi level gate driving for am oled panel," in *2010 Symposium on VLSI Circuits*, 2010, pp. 59–60.

[28] S.-W. Wang, Y.-J. Woo, Y.-S. Yuk, B. Lee, G.-H. Cho, and G.-H. Cho, "Efficiency enhanced single-inductor boost-inverting flyback converter

with dual hybrid energy transfer media and a bifurcation free comparator," in *2010 Proceedings of ESSCIRC*, 2010, pp. 450–453.

[29] B.-C. Kwak, S.-K. Hong, and O.-K. Kwon, "A highly power-efficient single-inductor bipolar-output dc–dc converter using hysteretic skipping control for oled-on-silicon microdisplays," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 2017–2021, 2018.

[30] K. Lin, S. Ng, T. Huang, K.-H. Chen, S. Liu, P. Chiu, S. Chen, C. Shen, M. Hsieh, and H. Li, "P-56: A single-inductor bipolar-output dc/dc converter with high efficiency over wide load range for active matrix oled," *SID Symposium Digest of Technical Papers*, vol. 45, 06 2014.

[31] "TPS65135: Single-Inductor, Multiple-Output Regulator by *Texas Instruments*," Online https://www.ti.com/lit/ds/symlink/tps65135.pdf.

[32] S.-W. Hong, "11.6 a 1.46mm¡sup¿2¡/sup¿ simultaneous energy-transferring single-inductor bipolar-output converter with a flying capacitor for highly efficient amoled display in 0.5µm cmos," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 200–202.

[33] F. Mao, Y. Lu, E. Bonizzoni, F. Boera, M. Huang, F. Maloberti, and R. P. Martins, "A power-efficient hybrid single-inductor bipolar-output dc-dc converter with floating negative output for amoled displays," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4.

[34] H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, and G.-H. Cho, "A single-inductor switching dc–dc converter with five outputs and ordered power-distributive control," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2706–2714, 2007.

[35] M.-y. Jung, S.-h. Park, J.-s. Bang, D.-c. Park, S.-u. Shin, and G.-h. Cho, "12.5 an error-based controlled single-inductor 10-output dc-dc buck converter with high efficiency at light load using adaptive pulse modulation," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.