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Design of Wideband CMOS Direct-Conversion Receiver for 5G Wireless Applications

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Ph.D. Dissertation of
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Abstract

Facoltà di Ingegneria

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Design of Wideband CMOS Direct-Conversion Receiver for 5G Wireless Applications

by Karan Sohal

As data rates increase annually, to fulfil the ongoing demand for higher data rates, newer mobile communication standards extend the channel bandwidth as much as feasible, while also increasing the number of bands and perhaps employing more than one antenna in transmission and reception. To increase bandwidths, mm-wave bands above 24 GHz are exploited for the first time in the 5G standard. Using carrier aggregation, channel bandwidths in these bands could possibly reach 2 GHz. The use of mm-waves allows the implementation of new heterogeneous transceiver architectures. As an example, the mm-wave signal is down-converted to an IF frequency using a technology suited for high frequency applications (i.e., BiCMOS, SiGe), and then the signal from the IF band is down-converted to baseband using a technology suited for digital and baseband processing (i.e., CMOS). This thesis presents the design of a wideband direct-conversion receiver in 28nm CMOS technology as part of this idea. The receiver down-converts the RF signal from the 7 GHz IF frequency to baseband. One of the key challenges for the receiver is the wide baseband bandwidth in the order of GHz, which makes the design of the receiver's baseband section particularly demanding. Furthermore, as the number of bands and antennas (MIMO) increases, the number of external RF filters must be reduced, which imposes strict linearity requirements since the receiver must handle powerful out-of-band blockers. The presented receiver covers RF channel bandwidths ranging from 50 MHz to 2 GHz that belong to 5G-FR2 bands. The voltage gain of the receiver is 45 dB and can be programmed down to 0 dB. It has a baseband bandwidth of 25 MHz to 1 GHz and more than 33 dB OOB selectivity at a frequency 4 times the band edge, consistent with 5G specifications. For maximum gain, the receiver has a noise figure of 5.6 dB and a slope of less than 0.7 dB/dB in the noise increase as the gain decreases. For any

gain configuration, the receiver displays a measured in-band OIP3 of greater than +23dBm. The power consumption is 68 mW at maximum receiver gain and 56 mW at minimum receiver gain. The receiver has been fully integrated and measurement results are fully complying with the design specifications.
The receiver front-end is composed of two cascaded LNTAs based on a common-gate transformer-based architecture. It achieves wideband matching from 5 GHz to 9 GHz, a high RF gain of 80 mS, and gain variability of 31 dB. The LNTA drives a double-balanced passive mixer. Two baseband paths are used to cover the very wide bandwidth range required. The first consists of a Rauch filter followed by a first order TIA and is used to cover baseband channel bandwidth from 25 MHz to 200 MHz. The second consists of an open loop second order filter followed by a wideband filtering TIA and covers channel baseband bandwidth from 400 MHz to 1 GHz. The primary contribution of the author in the baseband section is the design of the open loop filter which provide second order low pass filtering in the current domain. The filter, based on a regulated cascode architecture, achieves a bandwidth up to 1 GHz and a gain variability of 14 dB, which is compliant with the receiver specifications. A frequency dependent negative capacitance is connected at the filter input that improves the filter Q and provides an out-of-band selectivity equivalent to a 3^{rd}-order Butterworth filter. In addition, different negative capacitance circuits have been studied including a novel frequency dependent negative capacitance circuit which provides negative in-band capacitance and positive out-of-band capacitance. Such a solution further improves the Q and selectivity of the filter. The filter was tested as a stand-alone block providing an in-band IIP3 of +16dBm, which is two times higher compared to state-of-the-art wideband open loop filters with comparable noise and power dissipation.

Acknowledgement

To my friends and family

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Introduction

Nowadays, mobile communication has become an essential part of people's daily lives. Practically, our mobile cell phones have become our everyday companions. They are used for a variety of tasks such as composing emails, making both voice and video conversations, watch live program streaming, run IoT applications, and a plethora of other chores that we could not have imagined in the past. This is possible thanks to the increased data rates, associated with the evolution of mobile wireless communication technologies from GSM to 5G. In order to meet the continuos demand of increased datarates, standards for mobile communications extend as much as possible the channel width, while including an increase number of operative bands and possibly adopting more than one antenna in transmission and reception. To increase bandwidths, mm-wave bands above 24 GHz are exploited for the first time in the 5G standard. Using carrier aggregation, channel bandwidths in these bands could possibly reach 2 GHz. The use of mm-waves allows the implementation of new heterogeneous transceiver architectures. As an example, the mm-wave signal is down-converted to an IF frequency using a technology suited for high frequency applications (i.e., BiCMOS, SiGe), and then the signal from the IF band is down-converted to baseband using a technology suited for digital and baseband processing (i.e., CMOS). This thesis presents the design of a wideband direct-conversion receiver in 28nm CMOS technology as part of this idea. The receiver down-converts the RF signal from the 7 GHz IF frequency to baseband. One of the key challenges for the receiver is the wide baseband bandwidth in the order of GHz, which makes the design of the receiver's baseband section particularly demanding. Furthermore, as the number of bands and antennas (MIMO) increase, the number of external RF filters must be reduced, which imposes strict linearity requirements since the receiver must handle powerful out-of-band blockers. The presented receiver covers RF channel bandwidths ranging from 50 MHz to 2 GHz that belong to 5G-FR2 bands. The voltage gain of the receiver is 45 dB and can be programmed down to 0 dB. It has a baseband bandwidth of 25 MHz to 1 GHz and more than 33 dB OOB selec-

tivity at a frequency 4 times the band edge, consistent with 5G specifications. For maximum gain, the receiver has a noise figure of 5.6 dB and a slope of less than 0.7 dB/dB in the noise increase as the gain decreases. For any gain configuration, the receiver displays a measured in-band OIP3 of greater than +23dBm. The power consumption is 68 mW at maximum receiver gain and 56 mW at minimum receiver gain. The receiver has been fully integrated and measurement results are fully complying with the design specifications.
Below it is described the organizzation of the thesis.

Chapter1: provides background information on the key metrics that must be considered when evaluating any cellular system. Following that, a panoramic overview of some of the most widely used communication systems is presented, demonstrating the evolution of wireless systems toward larger channel bandwidths and more stringent performance, devoting more attention on the requirements specified by the most recent mobile standards (4G and 5G), with a primary focus on the receiver specifications.

Chapter2: gives an overview of various receiver architectures, explaining their pros and cons. Following that, the concept of a new heterogeneous receiver architecture for 5G mmWave will be discussed in detail with an emphasis on how this solution can be both cost-effective and easy to implement from technology point of view. After that, the proposed receiver architecture will be discussed in detail as part of this heterogeneous transceiver, showing its main peculiarities, design challenges and the specifications.

Chapter3: deals with the design of a receiver's analog front-end. To achieve high RF gain, the front-end is made up of two cascaded LNTAs. The chapter starts with the design of 1° stage LNTA. The LNTA's topology and input-matching network technique will be described in detail. The post-layout simulation results for noise and linearity will be presented. Following that, the design of 2° stage LNTA will be discussed, with a focus on how fully differential signals enable gain-boosting through a transformer, thereby saving power and improve noise performance. The last section of the chapter is devoted to the design of a current-mode passive mixer.

Chapter4: covers the design of the baseband. Two baseband paths are employed to cover a large channel bandwidth ranging from 50 MHz to 2 GHz. The first consists of a Rauch filter followed by a first-order TIA and is used to cover baseband channel bandwidth from 25 MHz to 200 MHz, called low fre-

quency baseband (LF BB) path. The second consists of an open-loop second order filter followed by wideband filtering TIA and cover channel baseband bandwidth from 400 MHz to 1 GHz, called high frequency baseband (HF BB) path. The design of the HF-BB path is the first topic covered in this chapter. The primary contribution of the author from the BB section is the design of the open-loop filter. A special emphasis is given on its design and the concept of using frequency dependent negative capacitance to improve the quality factor and OOB selectivity of the filter is thoroughly explored. The chapter's final section is devoted to the design of a LF BB path. Each block of the baseband has been protoyped and tested as a stand-alone block. The measurement results of each block will be presented.

Chapter5: presents the measurement results of the entire receiver and discuss its overall performance, fully complying with the design specifications. The receiver's measurement setup will be explained first. The first section will present the measurement results for the HF-BB path. The performance of the receiver's input matching, transfer function, linearity and noise will be evaluated. The LF BB path measurement results will be reported in the following section, assessing the same performance characteristics mentioned previously. Finally, the measured receiver performance with the intial specifications will be presented.

Chapter 1

Evolution of wireless standards and design metrics

Abstract
Wireless communication standards have evolved over time to provide superior service quality and to accomodate a growing number of connected users. Many new features have been developed to maximize the amount of data delivered and received, requiring improved system performance and complicated wireless transceiver design. This introductory chapter delves further into design metrics, particularly for new generation high-bandwidth applications. A brief history of wireless networks is presented, with a focus on the characteristics and criteria that are important to design of a receiver for user devices.

1.1 Receiver Design Metrics

Wireless communication demands a large number of operations in both the analog and digital domains. For example, it modulate and transmit data on the transmitter (TX) end, detect a signal and rebuild original data on the receiver (RX) side. As wireless is a busy and hostile environment, each block must adhere to certain requirements in order to properly communicate with rest of the system. The standard set these requirements and converts them into precise metrics for each block. Some significant performance criteria that can be used to measure wireless receiver performance will be discussed in the following sub-sections. Sensitivity, bandwidth, linearity and noise are some of them.

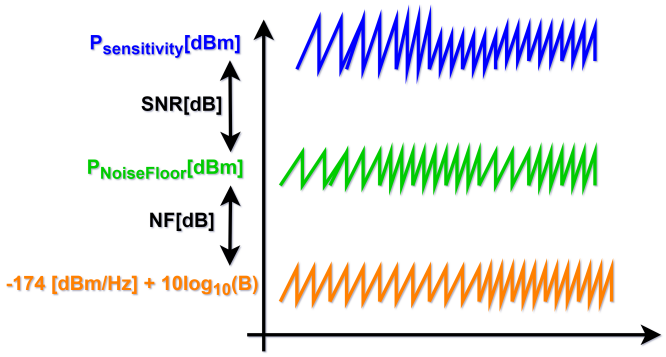


FIGURE 1.1: illustration of the receiver sensitivity.

1.1.1 Receiver Sensitivity and Noise Figure

Since a noisy environment contains both desired and undesired signals, the most important function of a RF receiver is to recognize the desired signal from the noisy environment while maintaining the signal quality. The term used to assess this crucial performance is the sensitivity of the receiver. For a given output signal-to-noise ratio (SNR), the receiver sensitivity is defined as the minimum detectable input signal power level by a receiver with acceptable signal quality. [1]

$$P_{sens[dBm]} = P_{Rs[dBm/Hz]} + 10log_{10}B + NF_{[dB]} + SNR_{min[dB]}, \tag{1.1}$$

where $P_{Rs[dBm/Hz]}$ is the noise power spectral density of antenna, $SNR_{min[dB]}$ is the minimum required Signal to Noise ratio at the output node and B is the channel bandwidth. $NF_{[dB]}$ expresses the noise figure of the receiver defined as the Signal to Noise ratio between input and output of the receiver chain.

$$NF_{[dB]} = 10log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right). \tag{1.2}$$

The first three terms in (1.1) gives the noise floor and they represent the total receiver noise referred to the input. The noise power spectral density of the antenna is K_BT, equals to $-174dBm/Hz$, given that the receiver input is matched to the antenna. Therefore, noise floor can be written as

$$P_{NoiseFloor[dBm]} = -174_{[dBm/Hz]} + 10log_{10}B + NF_{[dB]}. \tag{1.3}$$

This concept is illustrated in Figure 1.1. From (1.3), as that the noise floor is directly proportional to the bandwidth, the least detectable signal level will

increase for a given modulation scheme in the next generation of telecommunication systems with increasing data-rates and bandwidth. The maximum tolerable NF, being the actual requirement for RF designer can be calculated from (1.1), given the minimum SNR at the receiver output and acceptable sensitivity as described by the standard criteria.

1.1.2 Receiver Linearity

Another non-ideality that would affect the receiver performance is non-linear distortion. Because of the non-linear properties of the RF front-end devices, the interferers may intermodulate or a modulated interferer may cross modulate with the intended signal. As a result, distortions would occur, degrading the desired signal quality. The linearity properties of these devices can be characterized by gain compression (1-dB compression), third-order intercept point (IP3), either in-band IP3 or out-of-band IP3 and second-order intercept point (IP2).

In order to have clear insight on the term gain compression, the input/output characteristics of a non-linear device can be approximated with a Taylor's series expansion as:

$$V_o(t) \approx \alpha_1 V_{in}(t) + \alpha_2 V_{in}^2(t) + \alpha_3 V_{in}^3(t), \tag{1.4}$$

where $V_{in}(t)$ is the input signal, $V_o(t)$ is the output signal, α_2, α_3 are the second and third order non-linear coefficients and α_1 can be referred to as the device small signal gain when both α_2 and α_3 are negligible for small input swings. Assuming a single tone input signal, $V_{in}(t) = Acos(\omega_o t)$, passing through the non-linear device, the output can be expressed as:

$$\begin{aligned} V_o(t) &= \alpha_1 Acos(\omega_o t) + \alpha_2 (Acos(\omega_o t))^2 + \alpha_3 (Acos(\omega_o t))^3 \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right) Acos(\omega_o t) + \frac{\alpha_2 A^2}{2} cos(2\omega_o t) + \frac{\alpha_3 A^3}{4} cos(3\omega_o t). \end{aligned} \tag{1.5}$$

The non-linear device's output signal contains many harmonics of the input frequency as can be seen from (1.5). The device gain $\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right)$ at the fundamental input frequency is a function of input signal amplitude. This illustrates that the device gain deviates from its small signal value, as the input signal amplitude, A, increases. An extremely large input signal amplitude, in instance, would result in gain compression for $\alpha_1\alpha_3 < 0$, which is often the case in most RF circuits. Whereas for $\alpha_1\alpha_3 > 0$, the device gain expands. In order

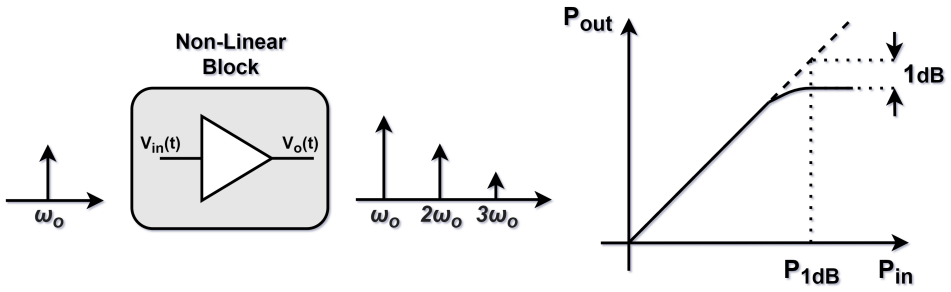


FIGURE 1.2: 1dB compression point of a tone in a non-linear block.

to evaluate the input signal level when significant gain compression occurs, a concept of 1-dB compression point, P_{1dB}, is used. P_{1dB} is defined as the input signal power that causes the linear small signal gain to drop by 1 dB, as shown in Figure 1.2. Thus, P_{1dB} can be calculated as: $P_{1dB} = \sqrt{0.145|\frac{\alpha_1}{\alpha_3}|}$.

Apart from large input signal, another scenario that can cause gain compression, is a strong undesired signal (interferer) comes with small desired signal. If in (1.4) it is assumed $V_{in}(t) = A_0 cos(\omega_o t) + A_1 cos(\omega_1 t)$, the term associated with $cos(\omega_o t)$ becomes

$$V_o(t) = \left(\alpha_1 + \frac{3\alpha_3 A_0^2}{4} + \frac{3\alpha_3 A_1^2}{2}\right) A_0 cos(\omega_o t) + ... \tag{1.6}$$

From (1.6), it is clear that if the amplitude A_1 of the interferer increases, the gain of the desired signal $A_0 cos(\omega_o t)$ drops. This is called desensitization of the receiver. This ultimately degrades the SNR of the system.

Another non-linearity related mechanism becomes particularly critical from receiver's prespective is the third-order intermodulation (IM3). This phenomenon occurs when the signal is accompanied by two tones at angular frequency ω_1 and ω_2. If $V_{in}(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$ then $V_o(t)$ becomes:

$$\begin{aligned} V_o(t) = \; & \alpha_1(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)) + \alpha_2(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^2 + \\ & + \alpha_3(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^3, \end{aligned} \tag{1.7}$$

which has components (associated with third-order non-linearity) at $2\omega_1 - \omega_2$

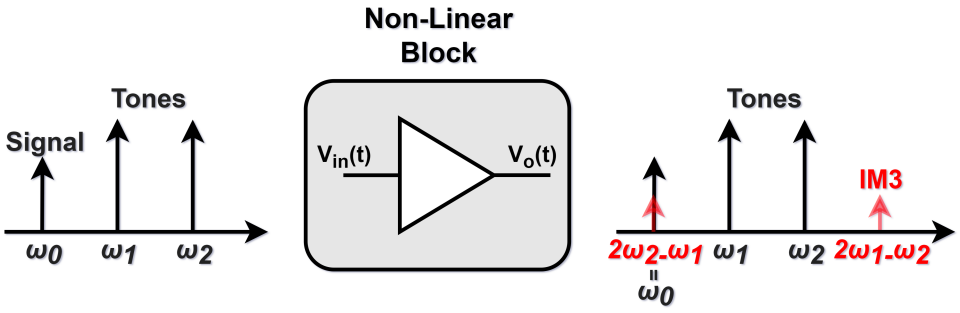


FIGURE 1.3: schematic description of IM3 tone falling on signal.

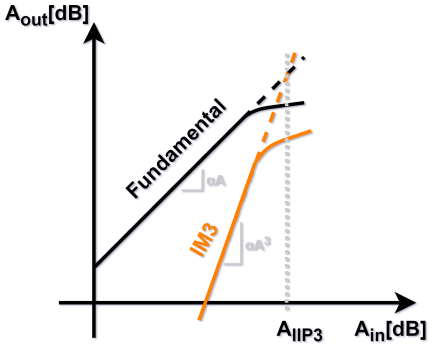


FIGURE 1.4: IIP3 as crossing point between IM3 and Fundamental on log scale.

and $2\omega_2 - \omega_1$:

$$V_o(t) = \ ... + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t + \\ + \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 - \omega_1)t + ... \tag{1.8}$$

Figure 1.3 depicts this phenomenon graphically, showing how if $\omega_o = 2\omega_2 - \omega_1$, the IM product might fall into the desired channel, lowering SNR. The two-tone test is used to assess receiver IM3 performance, in which two sinusoids of identical amplitude, A are delivered to the input and IM3 is measured. It is evident from (1.8) that IM3 rises as A^3, implying that the relative ratio of the Fundamental to IM3 increases as A^2. Since it is preferable to have a quantity that is not dependable on amplitude A, IM3 is measured in terms of IIP3.

This number indicates the input amplitude level corresponding to the intersection of input referred Fundamental and IM3 amplitude, as shown in Figure 1.4. Higher order non-linearites may appear at higher power levels, causing the Fundamental and IM3 slopes to vary from their predicted path. Intermdoulation then must be measured for lower input power levels, as illustrated in Figure 1.4., and IIP3 is extrapolated using the slopes (1 and 3 in a log scale) of the Fundamental and the IM3, resulting in:

$$A_{IIP3[dBV]} = A_{[dBV]} + \frac{A_{[dBV]} - A_{IM3[dBV]}}{2} \tag{1.9}$$

where $A_{IIP3[dBV]}$ is actual IIP3 expressed in dBV, $A_{[dBV]}$ and $A_{IM3[dBV]}$ are the amplitudes corresponds to the Fundamental and the IM3 respectively, referred to the input of the receiver. The same formula can be used with Fundamental and IM3 power expressed in dBm. In any wireless standard, there is a list of potential tests to assess the linearity of receivers. Each standard provides a measure for the designer to determine suitable system linearity parameters by specifying the interferer's amplitude and location in terms of intended signal bandwidth.

1.2 Evolution of Wireless Network Generations

Wireless networks have reached a significant milestone in their development. When it comes to cellular network advancements, during the last four decades, the number of users and apps have skyrocketed. To accelerate this progress, several new concepts and technologies have been used. The following part of this section provides a brief overview of the different wireless generations, with an emphasis on the most recent 4G and 5G standards.

One of the main reasons for the evolution of cellular standards is to fulfill the need of increased data speed and higher system capacity. Eventually, the question arises how it is possible to increase signal's data-rate in a communication system efficiently. In this regard, it is instructive to consider Shannon's theorem [2] which states that the capacity of a telecommunication system or in other words, the data-rate is directly proportional to the bandwidth of the channel. Thus, the idea of increasing signal bandwidth to increase data-rate sparked new ideas, such as allocating different channels from the same or different band to a single user. It can be done exploiting the channel-aggregation approach or using advanced modulation schemes in Multiple-Input-Multiple-Output structure to improve signal quality. A wireless system is often assigned

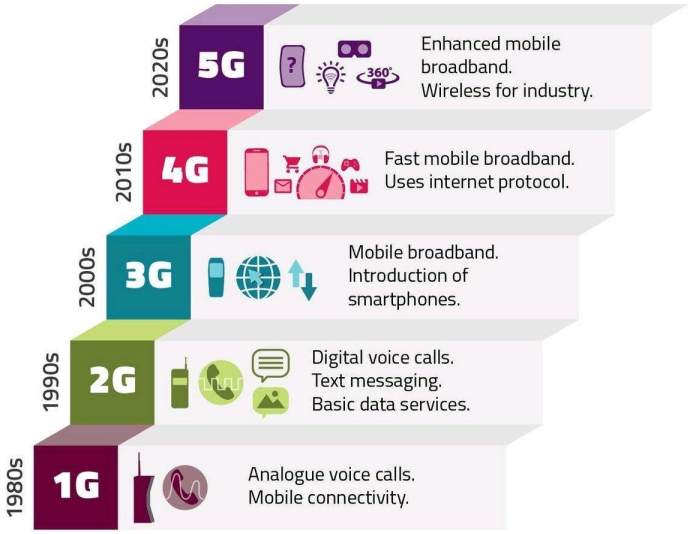


FIGURE 1.5: Evolution of wireless standards.

a predetermined frequency spectrum, however multiple access techniques enable users to efficiently share the available spectrum. Predominantly, multiplexing can be done in three dimensions for a wireless system: Time (TDMA), frequency (FDMA and its variation OFDMA) and code (CDMA). Figure 1.5 shows the evolution of the wireless standards over the period of time, highlighting the new features and advancements introduced by each standard.

1.2.1 Evolution from 1G to 3G

The first generation (1G) of the wireless network was developed in Japan around 1979 and it gained popularity in the US, UK and Europe in the 1980s. 1G networks were purely analog and they were mainly designed to provide voice services to mobile users. Different standard compose 1G, developed for different geographical areas. For example, key access technologies were Nordic Mobile Telephone (NMT) in many scandinavian countries like Norway, Sweden, Denmark, Finland and eastern Europe, Advance Mobile Phone Service (AMPS) in North America, Total Access Communication System (TACS) in UK and other [3]. All of these standards had the same characteristics. For example, AMPS employed FM modulation and operated around the 850 MHz band, with 832 channels spaced 30 kHz apart. AMPS uses Frequency-Division-

Duplexing (FDD) to send and receive data, using two distinct frequency bands. To address the issue of multiple access, 1G implemented the FDMA scheme, which assigns one channel per user, resulting in low capacity in congested areas and huge frequency gaps to minimize interference. Other problems hampered this network generation, such as poor hand-off reliability, security issues (calls were easily decrypted) and a small cell coverage area.

In 1991, the second generation (2G) of the wireless technology was first introduced in Finland. The fact that 2G was essentially a digital technology was the most significant breakthrough in comparison to 1G. This increased channel capacity are allowed for the installation of new services such as voice mail, mobile fax and Short Messaging Service (SMS). The main 2G access technology is represented by Global System for Mobile Communications (GSM) [4]. It operates at a data-rate of 64 kbps over a bandwidth of 30 to 200 kHz, which is suitable for data services like SMS and picture messages. As a multiple-access technique, TDMA is used. The TDMA system works by allocating the same channel to many users at various times. Multiple users can transmit on the same channel thanks to the usage of TDMA and enhanced channel bandwidth, increasing system capacity and number of users. 2G networks were further developed in the mid 1990's with the introduction of Code-Division-Multiple-Access (CDMA), which provided more features to 2G than GSM in terms of spectrum efficiency, number of users and data-rate [5]. General-Packet-Radio-Service (GPRS) and Enhanced-Data-GSM-Evolution (EDGE) were added to accomodate increased data-rates, with maximum data-rate of 171 kbps and 473 kbps respectively [6]. Despite the fact that digitalization of the communication system has resulted in smaller devices, more secure connections and improved call quality, it still suffers from a limited number of users and low data-rate. As a result, in Japan the new generation of cellular system was launched known as 3G.

The establishment of the third generation (3G) mobile technology was followed after the introduction of CDMA technique. In 3G, this multiple-access scheme is extensively utilized. CDMA signals, unlike FDMA and TDMA, can overlap in frequency and time. Each transmitter-receiver pair, on the other hand, is given a unique code, and each transmitted bit is multiplied by it before being modulated. To retrieve the original signal, the receiver uses the same code. Even though coding spreads the spectrum occupied by the transmitted signal (a technique known as "spread spectrum"), such multiple-access scheme has the potential to improve system capacity because mul-

tiple users can share the same spectrum. In the 3G framework, two main competing standards, CDMA2000 and WCDMA (UMTS) were developed. UMTS, for example, provides 5 MHz channel spacing and bandwidths ranging from 900 MHz to 2.1 GHz [7]. With such wide-band channels, mobile phones were able to offer video-calling for the first time. Smartphones became popular, and several programs supporting chat, e-mail, gaming, web-browsing, video-streaming and social-networking were developed for them. In order to further increase the data-rates, two new technologies were introduced in 3G: High-Speed-Downlink-Packet-Access (HSDPA) and High-Speed-Uplink-Packet-Access (HSUPA), which boosted the data-rates up to 2 Mbps. Another step forward in the HSPA network has been made with the introduction of HSPA+, which can theoretically improve transmission speeds up to 42 Mbps uplink and 22 Mbps downlink by employing sophisticated encoding techniques and multiple antennas to transmit and receive data requests. [8]

1.2.2 4G LTE

The fourth generation of wireless technology (4G) began in 2008 with the launch of Long Term Evolution (LTE), which increased data capacity over UMTS and met the growing demand for internet access and data services. The major aims of LTE were to increase data speeds, improve bit-rates at the cell edge, improve spectral efficiency, ensure more spectrum flexibility and reduce mobile power consumption. LTE was evolved throughout the years with the advent of LTE-Advanced (Rel. 10, 11 and 12) and LTE-Advanced-Pro (Rel. 13) [9]. Switching to different access technologies (such as UMTS and GSM) was possible in order to provide smooth coverage [10]. LTE is defined over a wide range of frequency bands, ranging from 700 MHz to 3.7 GHz, to allow it to be used all over the world. It provides the larger channel bandwidths than previous generations, following the trend seen in earlier standards. In particular, additional flexibility is provided by variable carrier width with values ranging from 1.4 MHz to 20 MHz. This, ofcourse, requires higher receiver reconfigurablitiy. In order to achieve higher data speeds, LTE must address problems related to multi-path transmission. In fact, when the symbol period approaches the time-delay introduced by channel, signal quality degrades due to Inter-Symbol-Interference (ISI). To overcome this issue, LTE employs OFDM, in which a high data-rate stream is first transformed into N parallel streams with N times lower data-rate. These are then impressed on N distinct carrier frequencies, which are referred to as sub-carriers. In comparison to single-carrier modulation, total spectrum occupancy and data-rate remain same, but each of the N streams now has lower bit-rate, allowing to tolerate

even a larger delay spread. LTE used variety of modulation techniques. In the first Rel. 8, only QPSK and 16QAM were used. In recent versions, these techniques have been combined with higher-order modulation techniques, such as 64QAM and 256QAM, to increase the datarate and improve the signal quality even more. Some of the important features of LTE standard are discussed below:

1.2.2.1 MIMO

MIMO stands for Multiple Input Multiple Output. LTE made use of multiple antennas in Base Station (BS) and User Equipment (UE) in order to increase data-rate. There are several ways in which MIMO is implemented in LTE. These vary according to the equipment used, the channel function and the equipment involved in the link.

- **Single Antenna:** This is the most common type of wireless transmission used in wireless connections. One antenna transmits a single data stream, which is received by one or more antennas. It may also be referred to as SISO: Single In Single Out or SIMO Single In Multiple Out dependent upon the antennas used. SIMO is also called receive diversity.

- **Transmit diversity:** This type of LTE MIMO technique make use of many antennas to transmit the same information stream. For this approach, LTE supports two or four channels. Using Space Frequency Block Codes, the information is coded differently. This setting improves signal quality during reception but does not increase data-rate.

- **Spatial Multiplexing:** This form of MIMO used within the LTE system involves sending two information streams which can be transmitted over two or more antennas. Spatial Multiplexing can be open-loop or closed-loop. In open-loop case, there is no feedback from the UE although a Transmission Rank Indicator (TRI) transmitted from the UE can be used by the base station to determine the number of spatial layers. Whereas, in the case of closed loop, a Pre-coding Matrix Indicator (PMI) is fed back from the UE to the base station. This enables the transmitter to pre-code the data to optimize the transmission and enable the receiver to more easily separate the different data streams.

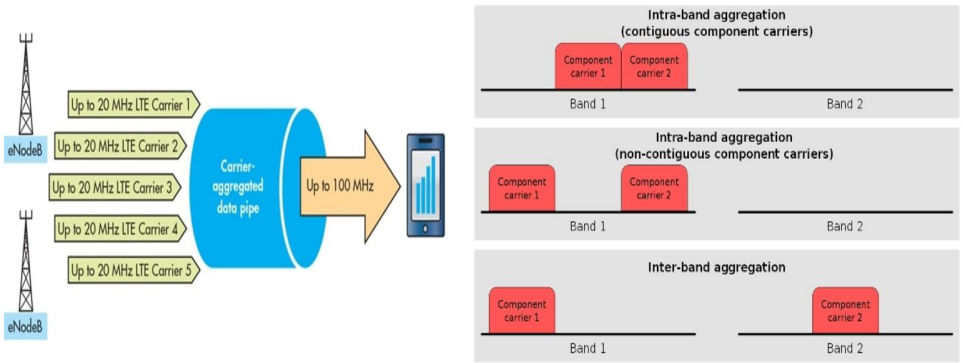
- **Multi-User MIMO:** This form of LTE MIMO enables the system to target different spatial streams to different users.

- **Beam-forming & MIMO:** This is the most complicated MIMO mode, and it is likely to include linear arrays that allow the antenna to focus on a specific region. As a result, the individual UE will have a beam produced in their specific direction, which will decrease interference and enhance capacity. A single code-word is sent over a single spatial layer in this case. A dedicated reference signal is used for an additional port. The terminal estimates the channel quality from the common reference signals on the antennas.

As the LTE standards progressed, so the number of antennas being supported increased. For many mobiles, the use of MIMO just resulted in improvements in signal performance, whereas for others it was able to provide data-rate improvements.

1.2.2.2 Carrier Aggregation

Carrier Aggregation (CA) is a feature of LTE-Advanced that allows mobile operators and devices to combine two or more LTE carriers into a single data exchange. It leads to an increase in network capacity and data speeds by exploiting fragmented spectrum allocations. This technology can apply to either



(a) (b)

FIGURE 1.6: (a) concept of carrier aggregation. (b) carrier aggregation schemes.

the FDD or TDD variants of LTE. In Carrier Aggregation technique, it is possible to group several carriers, referred to as component-carriers. In 4G LTE, multiple frequency bands are assigned to one device. There are component carriers with six specific frequencies: Those are 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz. One can combine at most 5 of these component carriers to transmit aggregated bandwidth of up to 100 MHz (see Figure 1.6(a)). There are different ways in which carrier aggregation can be done, as shown in Figure 1.6(b). When two or more component carriers belong to same frequency band then they come together. This arrangement is called intra-band contiguous carrier aggregation. Secondly, when the component carriers are from the same frequency band. However, they are separating by a spectrum gap then it's intra-band non-contiguous carrier aggregation. Lastly, when the component carrier belong to different frequency bands then they are placed in separate frequency blocks. It is called inter-band carrier aggregation.
Carrier Aggregation enables faster speeds, via multiples the number of LTE connections between the phone and the cell network. Instead of having just one LTE connection between the network and your phone, LTE modem that supports carrier aggregation when paired with a compatible network can actually bond together multiple, separate LTE connections and treat them as though they are one. It can double or even triple the internet speeds. In simpler terms, it is like widening the highway by adding more lane to create extra space on the highway for more cars to go at the same time.

1.2.3 5G

The use of mmWave frequency bands for mobile terrestial networks is one of the new aspects introduces in 3GPP Release 15, which includes the first definition of 5G standard. It is intended to address the stated objectives of ITU-2020, including greater spectral efficiency, higher number of users, higher data-rates, lower end-to-end latency, a more consistent user experience, higher device connection densities, prolonged battery life, service-based core network, etc. Although many of the fundamental 5G technology components build on 4G technology, referred to as FR1 (sub-6GHz Radio) by 3GPP [11], there are several technological advancements that are new in 5G. Among these new features is support for mm-wave frequency bands, otherwise known as FR2 in 3GPP vocabulary [12]. FR1 contains frequency bands covering the frequency range below 6 GHz. These bands are further classified into FDD bands, TDD bands, Supplementary Downlink/Uplink bands (SDL/SUL). The usable carrier bandwidths are increased compare to 4G, enlarging the available channel widths from 25 MHz to 100 MHz. Whereas, FR2 covers the mm-wave frequency

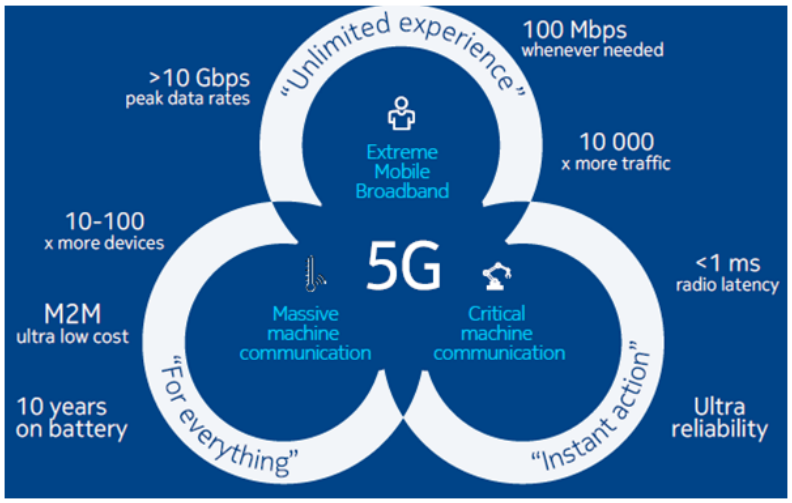


FIGURE 1.7: use cases of 5G mmWave.

range above 24 GHz, offering the carrier bandwidths in GHz range which rises the peak data-rate up to several tens of Gbps. This use of mmWave frequencies is an essential component of 5G technology, which seeks to ease mobile network capacity constraints in certain areas, or address new cases related to industrial automation, fixed wireless access, vehicle connection and potentially many more.

1.2.3.1 Use Cases of 5G-mmWave

The launch of 5G marks a new age of technical progress aimed at addressing a wide range of use cases, some of which may have not been possible to serve in the past, opens new frontiers for the wireless industry. While mobile broadband has been the primary use case for mobile operators so far, 5G plans to address additional large categories of use cases, such as massive IoT and critical communication (see Figure 1.7). Each of these groups has its own set of criteria in terms of throughput, latency, reliability, connection density and other performance metrics which may substantially increase the complexity of mobile networks. Futhermore, all these use cases would further exacerbate capacity costraints mobile networks, as increased data traffic will impose additional demands on those networks [13] [14]. Faced with those data traffic challenges, the mmWave frequencies which are specific to 5G technology, help to overcome some of the current capacity congestions as well as to address very time sensitive use cases. Here are some examples of the use cases of 5G-mmWave:

- **Enhance Mobile Broadband:** According to a recent research [15], existing mobile networks are congested, notably in densely populated regions, special venues or events, or specific market geographies but not everywhere. To relieve these top congested sites, mmWave might be implemented as part of broadband mobile network deployment, co-located with sub-6GHz frequencies as part of macro nodes or standalone smart cells at street level furniture. Variations in user throughputs over the day have also been used to support the usage of mmWave in mobile broadband networks. According to a recent research conducted by Open Signal across 77 countries, 4G download speeds varies between 31.2 Mbps and 5.8 Mbps, faster at the best hour of the day compared with the slowest hour of the day [16]. Cities see the biggest speed fluctuations, indicating that 5G can alleviate daytime congestion there since mmWave 5G might provide additional high capacitites. Another aspect that may exacerbate the present congestion difficulties in mobile networks is the expected growth in mobile traffic. According to CISCO research [13], consumer mobile data traffic will grow 7-fold from 2017 to 2022, with a compound annual growth rate of 48% due to two key contributing factors. One factor is that the number of wireless broadband connections continues to grow as more people use the internet and as the number of devices per capita increases. The second factor is that the content of mobile app offers is moving to greater data rates, such as 4K video, and all of the realities (VR, AR, XR). Therefore, for operators that do not possess sufficient sub-6GHz frequencies to address further traffic growth, mmWave frequencies may be the only option to do so.

- **Connected Vehicle:** Connected vehicle, commonly referred to as V2X (vehicle-to-everything) technology, enable vehicles to communicate with one another, roadside infrastructure and other road users. The example applications are road safety, traffic efficiency, smart mobility and autonomous driving, vehicle infotainment for passengers etc. There are several components of V2X, including vehicle-to-vehicle (V2V), vehicle-to-infrastructure (V2I), vehicle-to-pedestrian (V2P) communications. Each component has different requirements in terms of latency, throughput and reliability. For example, it is estimated that V2V information exchange requires up to 1 Mbps and within 5-10 ms in the case of cooperative maneuver planning and prediction. For cooperative perception function, V2V requires up to 10-20 Mbps within 10-50 ms. The required realiability is expected at 90-95%. [17] [18]

- **Industrial Automation:** Industrial automation is another potential area where mmWave can help enhance production efficiency and safety. It involves connecting industrial automation sensors, devices, and equipment with cloud-based systems in order to increase business value. Industry 4.0 use case based on robotics and slow-moving objects may be an area of interest. These paradigms would employ a range of techniques (i.e. imaging, sensing, XR) to boost production efficiency, with computers and robots constantly optimizing production and maintainance in highly flexible factories and plants. In such cases, which could be predominantly indoor, implementation of mmWave bands for the purpose of achieving very high wireless data throughput slow-moving robots in a separate network may be more plausible scenario for implementing mmWave on devices. Such type of devices would operate in environments where mmWave propagation characteristic may not be affected drastically like outdoor application. Furthermore, such devices may not be too restrictive from a power consumption, multi-antenna location, or beamforming performance. Equipped with advanced device designs, edge computing, mmWave cellular networks could provide highly capacity connectivity, enabling factories to become less dependent on wires and more flexible.

- **Fixed Wireless Access:** While morphological losses and building penetration are significant challenges in the mmWave frequencies, they are ideally suited for Line of Sight (LoS) of Gigabyte capacity links to buildings. Traditionally, mmWave frequencies have been used for backhaul applications. More recently, mmWave has been explored for Fixed Wireless Access (FWA), which uses wireless network technology rather than fixed lines to provide Internet access to homes (e.g. apartments) and businesses (e.g. universities, hospitals, retail shopping malls, etc.) It will boost wireless broadband fiber-equivalent connection using 5G ideas such as dual-connectivity, mmWave spectrum, and beamforming.

1.2.3.2 5G NR bands

3GPP Release 15 is the first release for NR (New Radio), and it aims to meet the ITU IMT-2020 criterias for 5G. While NR is mainly an evolution of LTE, it does include a number of significant new features, including support for higher frequency, mmWave bands. The NR bands were separated into two frequency ranges by 3GPP, shown in Table 1.1, with FR1 for bands below 6 GHz and FR2 for mmWave bands. The FR1 has been extended to 7.125 GHz in Release

16 to allow NR to be used in unlicensed bands in the 6 GHz region.

Frequency range designation	**Corresponding frequency range**
FR1	410 MHz - 7125 MHz
FR2	24250 MHz - 52600 MHz

TABLE 1.1: 3GPP Frequency ranges.

Operating Band	**UL operating band BS receive UE transmit**	**DL operating band BS transmit UE receive**	**Duplex Mode**
n257	26500MHz - 29500MHz	26500MHz - 29500MHz	TDD
n258	24250MHz - 27500MHz	24250MHz - 27500MHz	TDD
n260	37000MHz - 40000MHz	37000MHz - 40000MHz	TDD
n261	27500MHz - 28350MHz	27500MHz - 28350MHz	TDD

TABLE 1.2: mmWave bands.

In the FR2 range, 3GPP Release 15 defines only four bands: 24 GHz, 28 GHz and 38 GHz (see Table 1.2). All are defined as TDD to enable reciprocity-based beamforming. The main difference between the 3GPP's handling of FR1 and FR2 is that FR1 bands core and performance requirements are mostly based on conducted measurements, whereas FR2 bands specifications are largely based on OTA (Over The Air) measurements. Since higher frequency bands rely on various antenna methods (i.e. beamforming) to compensate for larger propagation losses, antenna systems are far more critical to the total system performance than FR1.

1.3 Additional Specifications

Some of the main requirements of the receiver specified by mobile standards are presented in this section, along with some quantitative examples from recent releases. Special attention is devoted to the RF receiver sensitivity and adjacent channel selectivity. In the later half of the section, more stringent specifications are presented that the designed receiver has to meet.

1.3.1 Sensitivity

Wireless standards define a reference sensitivity power level (REFSENS) that must be delivered to each of the two antenna ports in order to ensure that the throughput meets the specified criteria for the anticipated modulation and coding schemes, known as reference channels. For example, in 3GPP Release 15, specifications are provided for low SNR reference channels employing QPSK modulation with a coding rate of 1/5. In this case, sensitivity is necessary to guarantee a throughput of 95% of the maximum achievable, which corresponds to a SINR of -3 dB. The standard specifies sensitivity for each band and each allowable carrier bandwidth. Table 1.3 shows the reference sensitivity for power class 3 (used for UE) 5G NR mmWave bands.

Operating Band	**REFSENS (dBm) / Channel bandwidth**			
	50 MHz	**100 MHz**	**200 MHz**	**400 MHz**
n257	-88.3	-85.3	-82.3	-79.3
n258	-88.3	-85.3	-82.3	-79.3
n260	-85.7	-82.7	-79.7	-76.7
n261	-88.3	-85.3	-82.3	-79.3

TABLE 1.3: Reference sensitivity for power class 3 5G NR mmWave bands.

For an example, it is considered a 100 MHz channel from band n257 and by substituting the corresponding values in (1.1), the required NF can be extracted. It results in

$$P_{sens[dBm]} = -85.3 = -174 + 10log_{10}(10^7) + NF_{[dB]} - 3 + IM_{[dB]}, \quad (1.10)$$

where IM stands for Implementation Margin, which takes into account for any possible implementation non-idealitites that might impact signal processing before the demodulator and it is estimated to be 3 dB in this testing condition. As a result, the required NF to pass the test is 8.7 dB.

1.3.2 Adjacent Channel Selectivity

Adjacent channel selectivity (ACS) is a measure of a receiver's ability to receive a desired signal at its assigned channel frequency in the presence of an adjacent channel signal at a given frequency offset from the centre frequency of the assigned channel. ACS is the ratio of the receive filter attenuation on the assigned channel frequency to the receive filter attenuation on the adjacent

channel(s). According to 3GPP Release 15, the ACS requirement for UE for 5G NR FR1 bands and mmWave bands are specified in Table 1.4 and Table 1.5 respectively.

RX parameter	**Channel bandwidth**				
	10 MHz	**15 MHz**	**20 MHz**	**40MHz**	**50MHz**
ACS [dB]	33	33	33	33	33
RX parameter	**Channel bandwidth**				
	60 MHz	**80 MHz**	**90 MHz**	**100MHz**	
ACS [dB]	33	33	33	33	

TABLE 1.4: ACS for NR bands with F_{DL} and F_{UL} higher than 3.3 GHz.

RX parameter	**Channel bandwidth**			
	50 MHz	**100 MHz**	**200 MHz**	**400MHz**
ACS [dB] for band n257, n258, n261	23	23	23	23
ACS [dB] for band n260	22	22	22	22

TABLE 1.5: ACS for mmWave bands.

There are different tests specified for ACS in the presence of an interferer on the adjacent channel. The tests are different for bands belonging to the

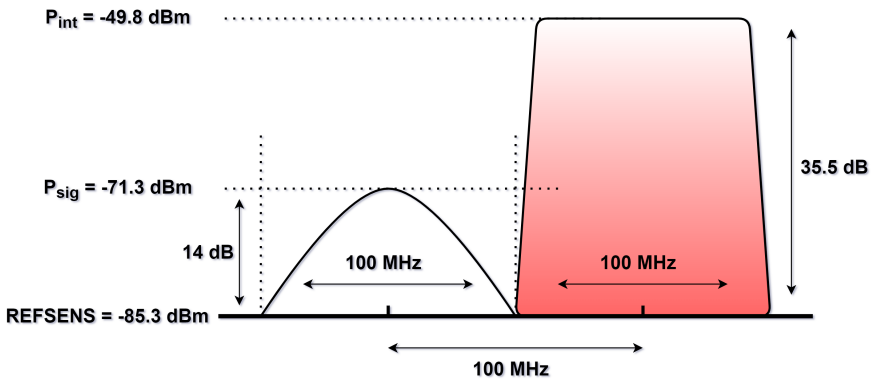


FIGURE 1.8: ACS test case for 100 MHz channel from operating band n257.

FR1 and mmWave bands. In both situations, the intended signal is set 14 dB above REFSENS, and the amplitude of the interferer varies with the carrier bandwidth. For instance, in the case of mmWave bands, the interferer power is set to be 35.5 dB above REFSENS for operating bands n257, n258, n261 and 34.5 dB above REFSENS for band n260. As an example, a case of 100 MHz channel from operating band n257 is reported in Figure 1.8. REFESENS for this reference channel is -85.3 dBm and a 100 MHz desired signal must be tested with an interferer in the adjacent channel whose bandwidth is same as the desired signal and its amplitude is 35.5 dB above REFSENS.

1.3.3 More Stringent Specifications

Previously, the exemplary sensitivity and selectivity requirements for general 5G recevier has been derived. However, the receiver presented in this thesis has more stringent specifications not only for noise and selectivity but also in terms of linearity, matching and gain configuration. The specifcations for the receiver are presented in Table 1.6. The proposed receiver must support a carrier frequency of 7 GHz and RF channel bandwidths ranging from 50 MHz to 2 GHz. The maximum achievable gain of the receiver chain should be 45 dB, and it should be programmble down to 0 dB. The receiver should be sufficiently

Item	**Condition**	**Specs**	**Unit**
Carrier Frequency	7000		MHz
Channel Bandwidth	Mode(50, 100, 200, 400,800,1600 and 2000)		MHz
Input VSWR	in all modes	1.5	
Gain Control Range	Max Gain	45	dB
	Min Gain	0	dB
Noise Figure	@LNA input max gain	5	dB
Noise Figure Slope		0.7	dB/dB
OIP3	All gain step, P_{RXOUT}=-8dBm	>15	dBm
Analog Filter Selectivity	From Bandwidth to 4 × Bandwidth	-33	dB
Inband Flatness	in all modes	1	dB
Power Consumption	Max gain mode		mW

TABLE 1.6: Receiver specifications.

linear to provide +15 dBm of IP3 at the output in all gain modes. It is expected to have less than 5 dB of noise figure, and the noise figure should not increase more than 0.7 dB for every dB of gain drop. The power consumption should be kept as low as feasible.

1.4 Conclusion

In this chapter, an evolution of mobile communication networks was provided, as well as an overview of the key requirements they impose on receivers, particularly for 5G NR, and the important specifications that the given receiver must meet. At this time, it should be obvious that the overall tendency of mobile networks is towards increasing speeds, increasing number of bands, multiplicity of antennas, and larger carrier bandwidths. The presence of several operational bands and antennas, as well as larger carrier bandwidths, makes it desirable to build receivers that can function over multiple bands and able to cover wider channel bandwidths. Especially, in the presented receiver, the necessity of wideband matching and gain configurability, as well as meeting the noise and linearity requirements for each gain mode, imposes significant challenges in the receiver's design, particularly in terms of its architecture and circuit topologies. Furthermore, larger channel bandwidths provide challenges on the design of the baseband portion of the receiver. The receiver architecture will be presented and discussed in detail in the next chapter, along with its advantages and disadvantages.

Chapter 2

Receiver Architecture

Abstract
With 5G posing different requirements to the mobile receiver than previous generations, the choice of wireless receiver is a key step in the mobile receiver design. It sets the requirements for individual components such as duplexers, filters, LNAs, Mixers and ADCs. In this chapter, an overview of conventional receiver architectures will be presented, together with its advantages and disadvantages, in order to make a justified choice of receiver architecture for 5G applications. Finally, the concept of heterogeneous transciever architecture for 5G mmWave will be presented along with the proposed current-mode direct conversion receiver architecture as part of this transceiver. The receiver architecture will be examined in detail, explaining each block's functionality in order to meet the required specifications.

2.1 Traditional Receiver Architectures

In this section, some of the important receiver architectures have been overviewed discussing their advantages and disadvantages.

2.1.1 Superheterodyne Receiver

In early days of cellular radio communication, the superheterodyne receiver is the most used reception technique and finds numerous applications from personal communication devices to radio and tv tuners. It was first introduced by Armstrong in 1921 [19], and is also known as the heterodyne or IF-receiver. As an example, a block diagram of superheterodyne receiver is shown in Figure 2.1.

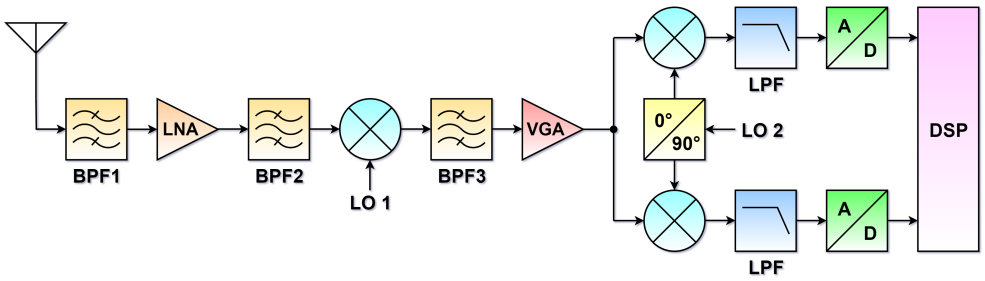


FIGURE 2.1: Block diagram of a dual-conversion superheterodyne receiver.

In a superheterodyne receiver, the signal from the antenna is first downconverted to IF by the first mixer, then downconverted to baseband after filtering by the quadrature down-conversion mixer. Its primary drawback is that not only the desired signal (located at f_c), but also the mirror frequency (located at $f_c - 2f_i$), is downconverted to IF. As a result, before mixing, the mirror frequency must be suppressed, which is done by BPF1 and BPF2, also known as image-reject filters [20]. The need for these filters is determined by the IF selection: if IF is high, the desired signal is distant from the mirror frequency. However, even when the IF is high, this results in strict filtering requirements, preventing the integration of these filters. This also means that variable filtering to accomodate frequency flexibility for 5G will be difficult. In addition to filtering, the LNA does some amplification prior to mixing to reduce the noise figure (NF) and therefore enhance the receiver's sensitivity. As a result, BPF1 also helps to prevent desensitization by removing out-of-band signal energy [21]. After downconversion to the IF, BPF3 applies further filtering to isolate the desired signal from other adjacent signals, commonly known as the channel select filter. Because this filtering is done at IF, the choice of IF has an impact on the filter requirements. For instance, if the channel separation remains the same choosing a high IF results in a higher required Q-factor than choosing a lower IF. Once again it is difficult to integrate these filters. As a result, choosing an IF is a compromise between image rejection (before mixing) and channel selection (after mixing). A variable gain amplifier (VGA) is used after BPF3 to enhance the signal to the ADC's optimal range. A signal is further downconverted to baseband after the VGA using analog quadrature downconversion. Although superheterodyne is known for its selectivity and sensitivity, the need of IF filters and two mixers make it unsuitable for

achieving a high level of integration at a low cost.

2.1.2 Homodyne Receiver

The homodyne, also known as direct-conversion or zero-IF receiver, was revived in 1980 [22] by the drive of the wireless industry and advancement in monolithic integration technology, despite the fact the concept was proposed around 1924. A block diagram of the direct-conversion receiver is shown in Figure 2.2. The primary difference between this and a superheterodyne receiver is that no IF is used here, or that the IF is set to zero. As a result, it trade off performance to lower cost and power consumption compare to superheterodyne receiver. Due to its simplicity and scalability, the homodyne receiver is the most used architecture in cellular devices and low-power applications, and it can be entirely integrated on chip because no high-performance BPF is required [23] [24]. This also increases the feasibilty to develop a tunable filter with adeguate performance for 5G.

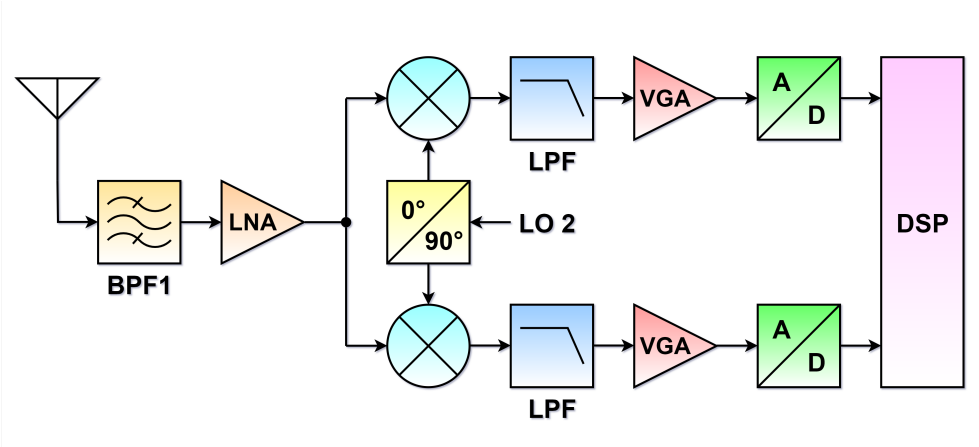


FIGURE 2.2: Block diagram of a direct-conversion receiver.

In homodyne receiver, the signal is directly downconverted to baseband without the need of an IF. As a result, since $f_i = 0$, the mirror frequency equals the frequency of the desired signal. However, there is still a problem with the mirror frequency: the desired signal is mirrored in the negative frequency range, resulting in the top end of the signal band from the postive frequencies overlapping with lower end of the signal band from the negative frequencies after downconversion, and vice versa. As a result, a quadrature downconversion is

required as shown in Figure 2.2. In most homodyne receivers, before mixing, the signal from antenna is filtered in order to prevent desensitization due to blockers and amplified in order to decrease the receiver's NF. After mixing, the desired signal is at baseband, and thus low pass filters (LPF) can be used for the channel selection. VGA's then bring the signal within the range of the ADC's where it is transformed to the digital domain and demodulated using DSP.
Compare to the superheterodyne receiver, the main advantage of the homodyne receiver is very high integration level that can be achieved, as in most designs no high Q band pass filters are required. However, this receiver architecture has an array of inherent challenges. Some of the system level issues associated with direct-conversion receiver are highlighted in the following subsections.

2.1.2.1 DC Offset

In direct-conversion receiver, as signal of interest is converted to baseband early in the receiver chain without any filtering other than RF-band selection, a variety of phenomenon contribute to the generation of DC signal, which appears as interfering signal in the band of interests, as illustrated in Figure

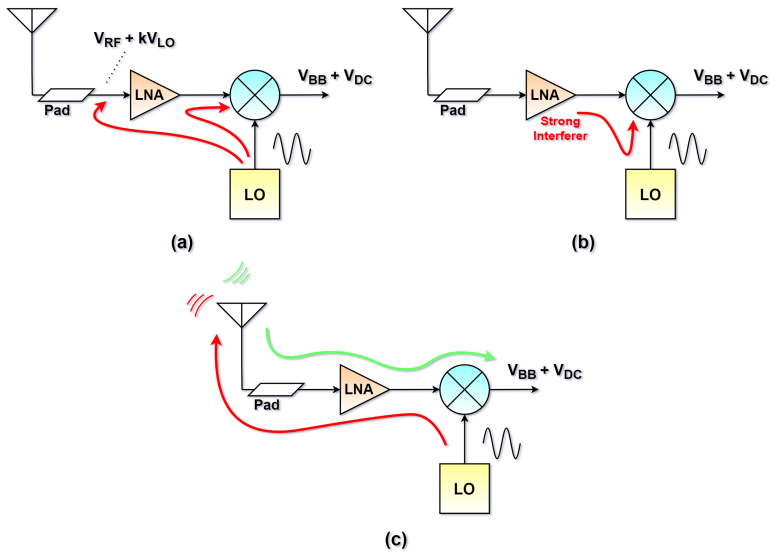


FIGURE 2.3: DC offset mechanisms in direct-conversion receiver: (a) self-mixing due to LO leakage, (b) self-mixing due to interferer (c) LO transmission and reception.

2.3.

- **Self-mixing of LO leakage:** The LO may be conducted or radiated in an unwanted path to the mixer's RF port, mixing with itself and creating an undesired DC component at the mixer output. Even worse, this LO leakage might reach the LNA input, resulting in an even more powerful effect. This phenomenon creates a significant obstacle against the integration of LO, mixer and LNA on a single silicon substrate, where numerous mechanisms can contribute to poor isolation. These include substrate coupling, ground bounce, bond wire radiation, and capacitive and magnetic coupling. One of the solution to mitigate this effect is high pass filtering in baseband [1]. However, if high-pass filter is poorly designed it may significantly degrade the received signal.

- **Strong in-band interferer:** A strong in-band interference signal, once amplified by the LNA, may find a path to LO-input port of the mixer. Thus, once again producing the self-mixing.

- **Radiation of LO leakage:** The LO power will be routed through the mixer and LNA to the antenna due to the non-ideal reverse isolation. The radiated power, which act as an interferer to other receivers in the corresponding band, may violate the provided system's emission regulations. It is crucial to note that while the LO frequency is within the receiver band, the front-end filters have no effect on this LO emissions. Furthermore, the emitted LO signal might be reflected by buildings or moving objects and received again by the antenna. This effect, however, is not so significant in comparison to the previously described LO self-mixing and blocking signal self-mixing. Although, one way to suppress this effect is to use differential LO with carefully designed symmetric paths. It leads to destructive interferences of the leaking phases on the antenna.

2.1.2.2 1/f noise

1/f noise, also known as flicker noise, is a drawback of the direct-conversion topology: as the signal is directly down-converted to baseband, flicker noise is the major baseband noise contributor. Associated with a flow of current, it has a spectral response proportional to 1/f. In RF circuits, 1/f noise tends to be modulated onto the RF signal, and in case of a mixer with baseband output, 1/f sees especially high gain. In practice, active mixer is the main source of the flicker noise in receiver, since the main method of reducing it in MOS is to increase the transistor's size, which increases the device capacitance,

adversely affecting RF gain. The 1/f noise of active mixer is much higher in CMOS technology as compare to mixer with bipolar switching core. However, in CMOS technology, the passive mixer architecture is dominating as in this architecture ideally, there is no DC current, hence 1/f noise contribution highly suppressed.

2.1.2.3 Second-order Distortion

In most systems, the third-order intermodulation is of importance as it usually falls in band, in the vicinity of the signals of interest, and is characterized by the IP3. In direct-conversion, second-order non-linearity becomes critical as it produces baseband signals, which now appear as interfering signals in the down-converted desired signal. This effect is schematically depicted in Figure 2.4. Second-order intermodulation (IM2) is strong especially in the case of single-ended LNA. As shown in the Figure 2.4, if there are two interferers close to each other, they produce a second-order intermodulation close to the DC at the output of the LNA. This tone can then feedthrough the mixer and appear as an interferer in the down-converted baseband signal. This effect can be nullified by using fully differential LNAs and mixers. However, all the real-circuits, exhibit some unbalance and hence leads to second-order non-lineariy and feedthroughs, due to the mismatches of the components. Therefore, it is important to evaluate the second-order performances of the direct-conversion receiver (measured by A_{IP2}).

2.1.2.4 I/Q Imbalance

Due to high frequency of the LO, it is not very practical to implement the IQ demodulator digitally. An analog demodulator exhibits gain and phase imbalances between two phases, as well as the introduction of DC offsets. Such imbalances distort the recovered constellation. Assuming α and θ are the amplitude and phase mismatches between the demodulator's quadrature ports, respectively, and the complex signal incident upon it has in-phase and quadrature components I and Q, then

$$\begin{aligned} I_{out} &= (Icos(\omega t) + Qsin(\omega t))2cos(\omega t) \\ Q_{out} &= (Icos(\omega t) + Qsincos(\omega t))2(1+\alpha)sin(\omega t + \theta) \end{aligned}$$

Filtering out the high frequency terms yields

$$\begin{aligned} I_{out} &= I \\ Q_{out} &= (1+\alpha)(Isin\theta + Qcos\theta) \end{aligned}$$

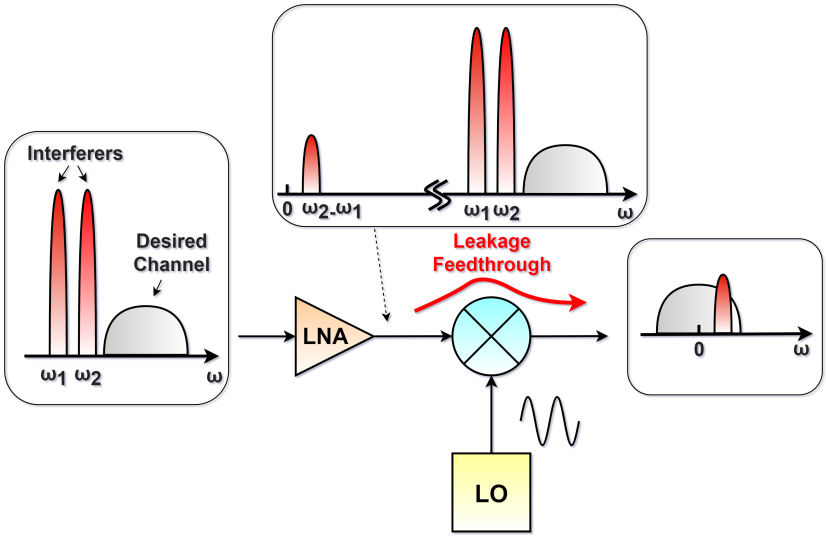


FIGURE 2.4: second-order distortion effect in direct-conversion receiver.

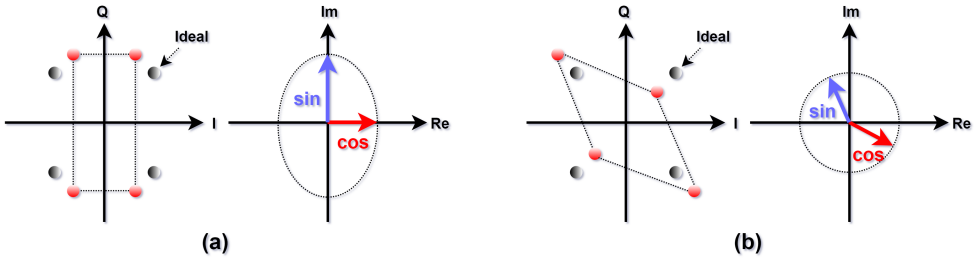


FIGURE 2.5: IQ demodulator imperfections: (a) gain imbalance and (b) phase imbalance.

Figure 2.5 shows how this affects a given constellation diagram. In direct-conversion receivers, however, the IQ matching is not as critical as in image-rejection architectures. Rather, it is only important insofar as the accuracy of the modulation is concerned.

In conclusion, the direct-conversion receiver is an attractive yet challenging receiving technique. It gained popularity due to the need for better portability

and lower-cost.

2.2 Heterogeneous Transceiver Architecture

The mmWave in the 5G standard opens up a lot of new possibilities, such as more available spectrum, larger channel bandwidths (up to GHz), and higher area spectral efficiency, it also poses a lot of design challenges for UE transceviers. For example, as the frequency of the signal increases, the propagation loss increases because the signal is more easily blocked by buildings and the human body. It is difficult to implement indoor-outdoor connectivity. As we move to higher frequencies, the performance of existing semiconductor technology gets limited, power consumption increases, and components costs get higher.

By considering aformentioned challenges, opens up the possibility of using new heterogeneous architecture for 5G mmWave transceivers. Figure 2.6 shows the block diagram of the proposed transciever, which is a split-IF architecture. The beam-forming (BF) module not only integrates the active antenna array for beamforming, but also allows for uplink and downlink frequency conversion. The BF module converts a mmWave 5G band signal to a low GHz intermediate frequency (IF) signal in the downlink path and an IF signal to a 5G band signal in the uplink path, as shown in the Figure 2.6. The local oscillator (LO) signal f_{LO1} can be tuned to achieve frequency conversion for a 5G TDD signal in the 28 GHz frequency band. Furthermore, by changing the LO frequency and corresponding hardware characteristics, this RF architecture can be applied to 37 GHz, 39 GHz, and other 5G frequency bands. This 5G BF module can be built with a technology that is better suited for high-frequency applications, such as BiCMOS, SiGe, or GaN. The signal from IF band can be down-converted to baseband using IF 5G radio which can be designed in technology suited for

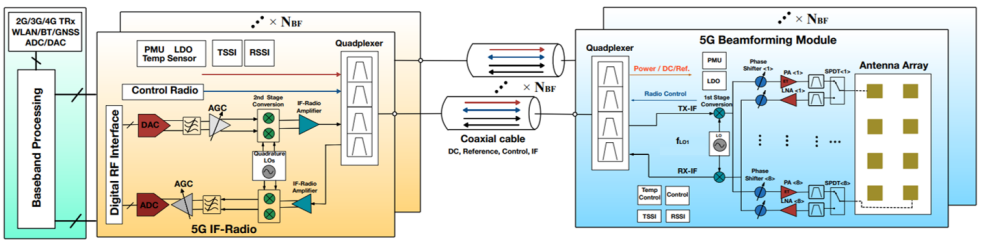


FIGURE 2.6: block diagram of 5G user equipment wireless system architecture.

digital and baseband processing, i.e. CMOS.
Moreover several factors contribute to the motivation and benefits of using this RF architecture:

- The high-performance mmWave circuits design necessitates a mmWave-enabled PCB, such as Rogers RO4003C, which is more expensive but electrically less lossy than the FR-4 laminate commonly used in today's smartphones for the main logic board (MLB) design. As a result, separating BF modules and MLB designs allows for cost-effective mass production.

- The front-end insertion loss is minimized by directly converting the mmWave frequency to the IF frequency on a BF module. Furthermore, because the connection is made via coaxial cables rather than routing traces on the MLB, better signal integrity can be achieved.

- It allows you to handle a variety of applications and scenarios without having to change the entire wireless system design. The placement and number of BF modules in the handset, for example, can be adjusted to suit various system specifications and use cases, making it cost-effective.

- Low-GHz IF radio is easier to implement than its mmWave counterpart, so it can be co-designed and manufactured alongside cellular standards like 3G and 4G in the same IC processes and SoCs. Furthermore, it can help with mass production testing for both BF and IF radio plus baseband modules.

2.2.1 Current-mode Direct-Conversion Receiver

A direct-conversion current-mode receiver is presented in 28nm CMOS technology as a part of this heterogeneous transciever architecture. In a 5G IF-radio, it downconverts the RF signal from 7 GHz IF frequency to baseband. A simplified block diagram of the receiver is shown in Figure 2.7.
In this architecture, the front-end LNA is replaced with a RF transconductance (LNTA). The LNTA drives a current mode passive mixer followed by a low input impedance filter or TIA. In such an approach, the impedance seen by the LNTA is given by the series combination of mixer switch resistance and the TIA's upconverted input impedance. As a result, low load impedance (Z_{RF}) at the output of the LNTA can be ensured. Depending on the value of R_{on} and Z_{BB} as provided by (2.1), Z_{RF} can be as low as 5 Ω and can have peak value less than 30 Ω. This architecture offers better performance in terms of noise,

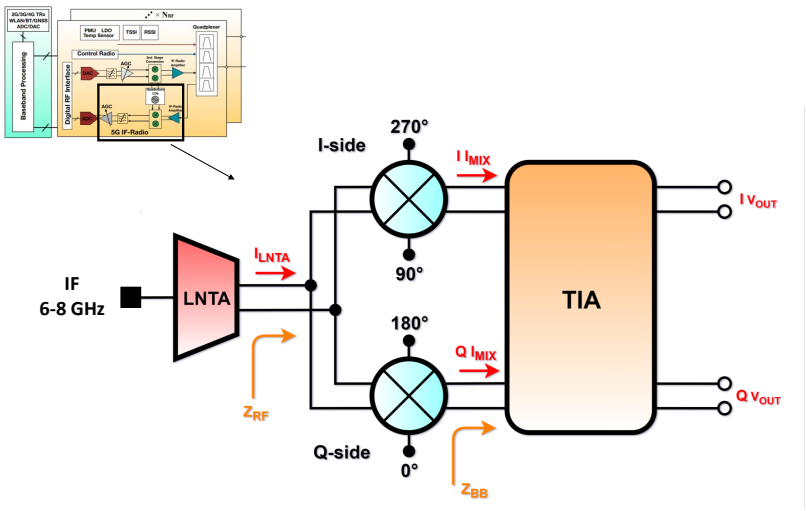


FIGURE 2.7: a simplified block diagram of current-mode direct-conversion receiver.

linearity and power consumption than active mixers and voltage-mode mixer implementations [25].

$$Z_{RF}(s) = R_{on} + \frac{2}{\pi^2}\{Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO})\} \tag{2.1}$$

In (2.1), R_{on} is the on-resistence of the passive mixer switch and Z_{BB} is the input impedance of the baseband filter, TIA. ω_{LO} is the local oscillator frequency in the direct conversion receiver. At low frequencies, $Z_{BB} \approx \frac{1}{G_{m,TIA}}$. As the information is carried in current, this architecture has the ability to handle large signals with minimum distortion [26] [27]. The advantage of having low output impedance of the LNTA in this design results in reduced output non-linearity with less output signal swings. Wide-signal operation and distortion of the LNTA is mostly determined by the MOSFET transconductance in the LNTA. By these architectural improvements, and by having low voltage signal swings, this receiver architecture can achieve large linearity figures.

2.3 Proposed Receiver Architecture

Within the framework of current-mode direct-conversion receiver, the block diagram of the proposed receiver architecture is presented in Figure 2.8. To

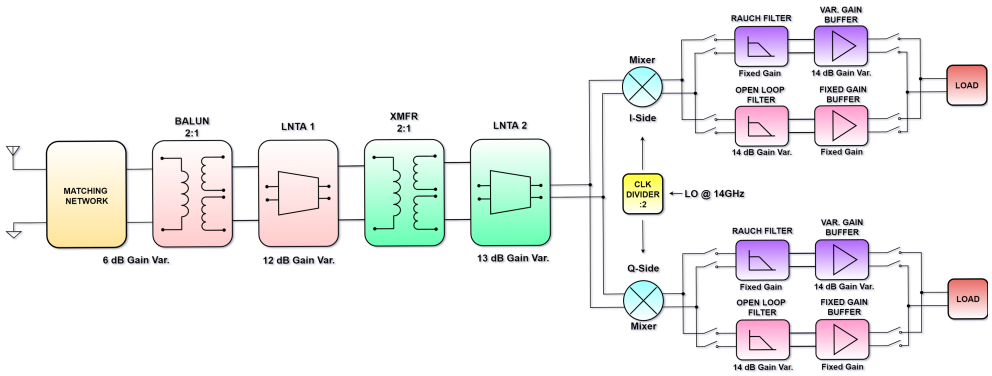


FIGURE 2.8: a block diagram of proposed current-mode direct-conversion receiver.

achieve high RF gain, the front-end is composed of two cascaded transconductance LNA (LNTA). The first LNTA is biased by a trifilar transformer, which also serves as a balun for matching. Similarly, a trifilar transformer is used to bias the second LNTA. Two LNTAs are used to increase RF transconductance gain, as it is difficult to obtain very large gain at baseband TIA due to the necessity for bandwidth in the order of GHz. Both trifilar transformers have turn ratio of 2:1, which gives a total current gain of 12 dB, results in an effective transconductance gain of 80 mS in a matching condition. In addition, the balun transforms the single-ended signal to a differential signal, allows to use fully-differential LNTA topology. As a result, second-order non-linearity is highly suppressed. A 45 dB of gain variability is required as a specification; two cascaded LNTAs offer great flexibilty in terms of gain variability. The front-end has a total gain variability of 31 dB, with 6 dB provided by a resistive divider in the matching network, 12 dB provided by the first LNTA, and 13 dB provided by the second LNTA.

The front-end drives the current-mode passive mixer. A 25% duty-cycle I-Q switching stage is implemented by using serial switches driven by 50% quadrature local oscillator (LO) signals separately, which improves the down-conversion gain by 3 dB and lowers the NF. LO signals are provided externally at $2f_{LO}$ and 25% duty-cycle clock is generated on chip using clock divider.

Following the mixer, there are two baseband paths that can be connected or disconnected from the mixer to cover a wide range of RF channel bandwidths from 50 MHz to 2 GHz. The one consists of an open-loop filter and fixed gain

TIA is used to cover larger RF channel bandwidths (from 800 MHz to 2 GHz) and is referred to as high frequency baseband (HF-BB) path. Similarly, the one with a Rauch filter and a programmable gain TIA is used to cover lower RF channel bandwidths (from 50 MHz to 400 MHz), and is called the low frequency baseband (LF-BB) path. In HF-BB path, the open-loop filter provides a 2^{nd} order low pass filtering in the current domain and offers a low input impedance to mixer and high driving impedance to the following closed-loop TIA. It provides a 14 dB of gain variability to achieve 45 dB of total gain variability in full RX chain. The TIA following the open-loop filter has fixed gain and it guarantees 1 GHz of closed-loop bandwidth. It is based on Operational Transconductance Amplifier (OTA) closed in feedback with a parallel RC network. The OTA is implemented with 3 cascaded Gm-stages and a feed-forward stage in order to ensure stability. It has an open-loop bandwidth of 7 GHz and open-loop gain of 24 dB at 1 GHz which is high enough to ensure good linearity performance. In LF-BB path, the Rauch filter uses a large capacitor to filter out clock harmonics. For both Rauch and the following TIA, the OTA is based on cascaded Gm stages and a feed-forward stage. In this path, the TIA offered 14 dB gain variability and the Rauch has fixed gain.

The gain control strategy of the receiver is illustrated in Figure 2.9. It is designed in such a way that NF and linearity criteria for each gain configura-

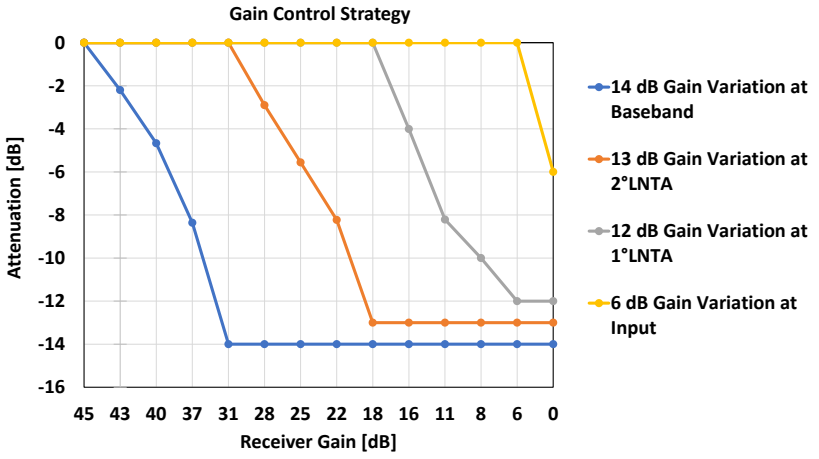


FIGURE 2.9: gain control strategy for receiver.

tion are satisfied. The gain start to decrease from the baseband. In four steps, 14 dB of gain configurability is accomplished. The baseband gain reduction has negligible impact on the overall NF, leaving enough margin to preserve the slope of NF of +0.7 dB for every dB of gain reduction. The following 13 dB of gain variation is implemented at second LNTA and 12 dB at first LNTA. As the front-end gain decreases, the NF begins to rise but always remains below the minimum requirement. The last 6 db of gain variability is achieved in the matching network using a resistive divider while maintaing the input matching. In addition, with this implementation an OIP3 of more than +15dBm is maintained for each gain configuration. From a design standpoint, the challenging specifications are NF of less than 5 dB in maximum gain mode and OIP3 of +15 dBm in minimum gain mode.

In conclusion, a wideband current-mode receiver architecture is presented within the context of direct-conversion receivers for 5G wireless applications. The proposed receiver architecture has two wideband cascaded LNTAs to achieve high RF transconductance gain and low noise figure. The receiver able to cover RF channel bandwidths from 50 MHz to 2 GHz belongs to 5G mmWaves. For this, two separate baseband paths are used. In the following chapter, the design of analog front-end will be presented and each block will be separately discussed in detail.

Chapter 3

Design of wideband analog front-end

Abstract
This chapter deals with the design of the analog front-end of the receiver. The chapter starts with the design of first-stage LNTA. The topology of the LNTA and input-matching network technique will be described in detail. The post-layout simulation results for noise and linearity will be presented. The design of the second LNTA will next be described, with a focus on how fully differential signals enable gain boosting through a transformer, saving power and improving noise performance. The last section of the chapter is devoted to the design of a current-mode passive mixer.

3.1 Design of CG LNTA with Integrated Trifilar Balun

The Common Gate (CG) amplifier is known for its high linearity and better operation in wide frequency range. The designed LNTA is based on a class AB p-n CG amplifier. A simplified single-ended diagram of the LNTA is presented in Figure 3.1. The signal is fed to the LNTA through an integrated transformer with one primary and two identical secondary coils. It splits the signal and inject it at the source nodes of the input transistors. The use of transformer allows the source voltage of the input transistors to go above power supply and below ground, provides class AB operation and low noise biasing. Furthermore, the small turn ratio (n:1 where n>1) between the secondary and primary lowers the voltage swing and provides the current gain at the secondary. The linearity of the input transistors is improved by reducing the swing at the source, while

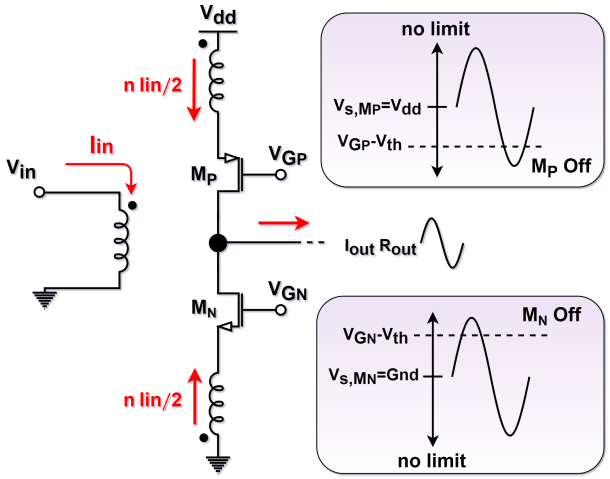


FIGURE 3.1: a simplified single-ended schematic of CG LNTA.

current gain accomplished without sacrificing linearity. As shown in Figure 3.1, the current is distributed nearly evenly between the two secondary coils, which have the same inductance and drive the same impedance. While the input should not compress, the output can if the load impedance is sufficiently high. However, current-mode operation requires a low impedance load, resulting in a high linearity and compression point.

A complete LNTA schematic is shown in Figure 3.2. This architecture is first presented in [28], where the LNTA is designed to operate at a frequency range of 1800-2100 MHz in saw-less receiver for TDD applications. In this work, the LNTA operating frequency range is increased to 6000-8000 MHz suitable for 5G receiver. The rise in carrier frequency introduces new design challenges, especially in the case of transformers. (addressed in 3.1.1). The transformer is used with 2:1 turn ratio which provides 40 mS of transconductance gain in matching condition. Furthermore, it act as a balun, converting single-ended signals to differential signals, allowing LNTA to employ a fully differential topology. In the LNTA, the fully differential signal path rejects the common-mode noise and second-order non-linearities. Wideband operation and excellent linearity are provided by the common-gate topology, but it has a large NF that is restricted by the matching condition. A traditional CG amplifier's NF is given as:

$$NF_{CG}(s) = 1 + \frac{\gamma}{g_m R_s} \tag{3.1}$$

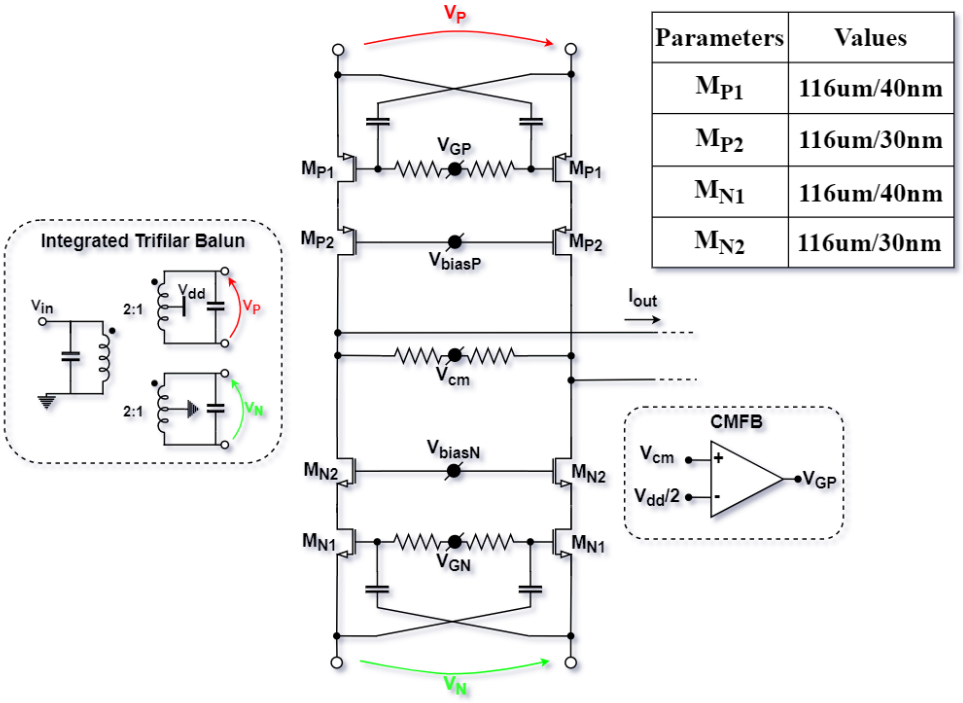


FIGURE 3.2: a complete schematic of CG LNTA.

where γ is the MOS excess noise factor, R_s and g_m are source resistance and MOS-transconductance respectively. To reduce noise, [28] employs passive gate boosting, in which the gate of the input transistor is connected to the primary of the transformer, which boosts g_m using the transformer's turn ratio. However, a 4-coil tranformer is needed to perform this operation. With the increase of the frequency, this approach is not feasible in this design due to the parasitic capacitances introduced by the transformer which limits the achievable SRF of the inductors. A different approach is adopted here which allows to eliminate the extra-coil in transformer that was required in [28]. The gate of the transistors are not connected to the transformer but are simply cross-coupled using cross-coupling capacitors. The cross-coupled capacitor apply the replica of the input voltage signal at source to the gate with a negative sign which doubles the applied v_{gs} voltage. As a result, the g_m of the transistor is boosted by a factor of 2, resulting in improved noise performance with no additional power consumption. By neglecting the transformer losses, the NF for the cross-coupled

LNTA topology results in:

$$NF_{CC}(s) = 1 + \frac{\gamma}{4g_m R_s} \tag{3.2}$$

In addition to noise reduction, cross-coupled capacitors improve immunity to common-gate signals (including second order distortion effects) at the LNTA's input since they are present at both the gate and source of the input device. As a result, the main term in CG LNTA third-order distortion, given by second-order non-linearity, dissappears, enhancing also the LNTA IIP3. Input transistors are cascoded to increase the output impedance and to have lower parasitics in order to improve the current-mode operation. A common-mode feedback network is used to fix the output voltage at $V_{dd}/2$.

3.1.1 Transformer design challenges

The transformer is an important component in the design of the LNTA. Because it is connected to the input pins, its noise is directly added to the source noise, degrading the NF. To minimize losses, the transformer should have coupling coefficient as close to one as possible and the highest Q achievable to decrease its intrinsic noise. In addition, the transformer ratio specifies the tradeoff between linearity and power consumption, as determined by the matching condition. In cross-coupled CG topology, matching condition is given by:

$$R_s = \left(\frac{1}{g_{mp}} || \frac{1}{g_{mn}}\right) n^2 \tag{3.3}$$

where R_s is the source resistance, n is the transformer ratio (for a transformer n:1) and the g_{mp} and the g_{mn} are the transconductance of the n and p MOS transistors respectively. By assuming $g_{mp} = g_{mn} = g_m$, the matching condition further simplified as

$$R_s = \frac{n^2}{2g_m} \tag{3.4}$$

It is clear from (3.4) that increasing the transformer ratio, for a transformer n:1, to improve transconductance gain necessitates increasing the g_m accordingly to ensure matching, resulting in higher static power dissipation in LNTA. On the contrary, when the transformer ratio is reduced, the linearity decreases because the MOS transistors are solicitated with a higher voltage. Futhermore, a large transformer ratio introduce more parasitic capacitances between the primary and secondary coils, degrading the quality factor. By considering above tradeoffs, a turn ratio of 2:1 has been used to avoid huge parasitic capacitances and

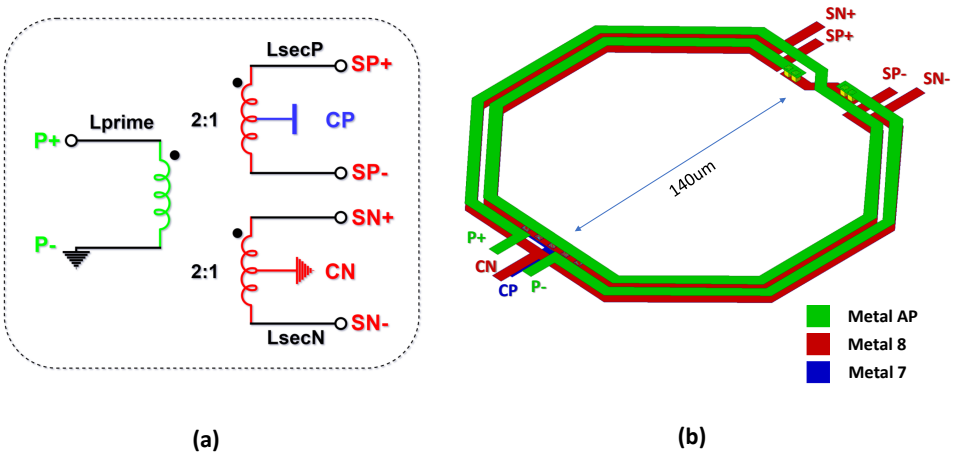


FIGURE 3.3: a 2:1 trifilar balun: (a) schematic (b) layout

power consumption.
For integrated transformers, the performance is strongly related to the available technology. The design employs TSMC 28nm CMOS technology, which provide 8 stack metal layers, the thickest of which being metal 8, as well as an additional alluminum metal (AP) for bond pads. Metal 8 and metal AP are used to achieve high Q for primary and secondary windings. The schematic and layout of the transformer are shown in Figure 3.3. A stacked topology is chosen over co-planar to maximize the coupling between two windings. As shown in Figure 3.3(b), the primary winding is made of metal AP and has two turns with width size of 6μm and spacing of 3μm. Two secondary coils are built on the bottom plane utilizing metal 8 to produce a 2:1 turn ratio. The width and spacing of the secondary coils are same as the primary coils in order to maximize the coupling. In addtition, secondary coils require centre tap to provide Vdd and Gnd connection. To minimize mismatches, the centre tap should be in the same location for both secondary coils. For LsecN (connected to Nmos in LNTA), Gnd is provided using the same metal 8 as the coil, whereas Vdd is provided at the centre tap of LsecP (connected to Pmos in LNTA) using metal 7. This choice also facilitates the connection of Vdd and Gnd with external circuitary since metal 8 and metal 7 are used for Gnd and Vdd connections in the chip. Electromagnetic simulations (EM) are used to characterize the transformer performance. The plots of inductance values and quality factor

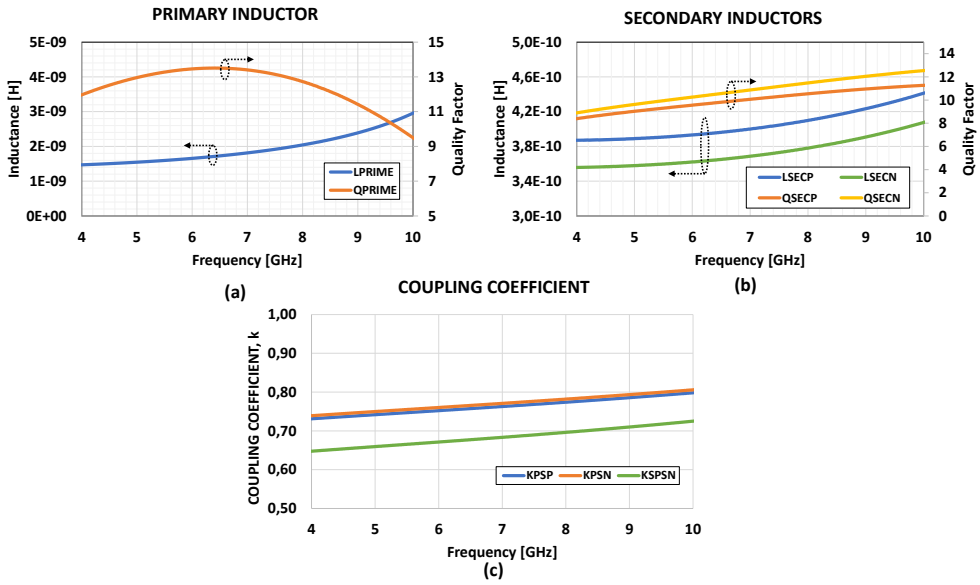


FIGURE 3.4: (a) inductance and quality factor of primary coil. (b) inductance and quality factor of secondary coils. (c) coupling coefficient between different coils.

for the primary and secondary coils of the transformer are shown in Figure 3.4(a) and 3.4(b) respectively. The coupling coefficient, k, between different coils is shown in Figure 3.4(c). The primary coil has an inductance of 1.4 nH and Q of 10.7 at 7 GHz. For secondary coils, LsecP has smaller diameter than LsecN being the internal coil in the layout. The inductance value of 370 pH and Q of 10.8 for LsecP and an inductance value of 400 pH and Q of 10.1 for LseN is achieved. The coupling coefficient of 0.77 is achieved between primary and secondary coils thanks to the stacked topology.

3.1.2 Input matching network

For an input matching, a simple circuit model for a transformer is considered, shown in Figure 3.5(a), where the primary coil has self inductance L_P and two secondary coils are combined into a single secondary coil with self inductance L_S. These inductors are magnetically coupled with a coupling coefficient k and turn ratio n = $\sqrt{\frac{L_S}{L_P}}$. The effective turn ratio for this $1:n$ transformer is given by n/k [29]. The ohmic losses of metal traces, substrate losses, and other losses are represented on the primary and secondary sides, respectively, by the resis-

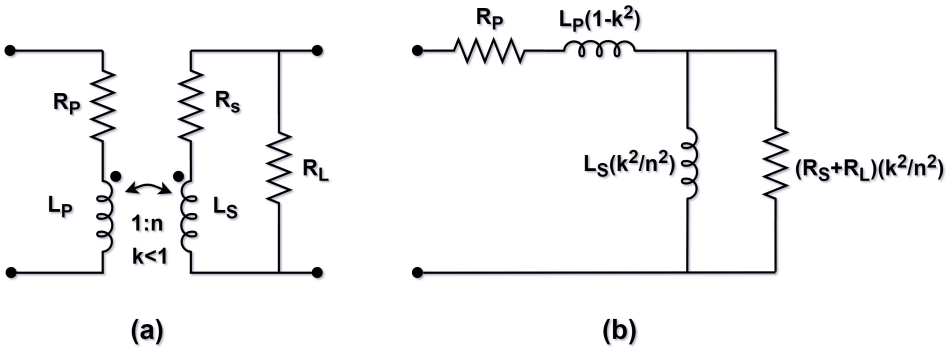


FIGURE 3.5: (a) circuit model of 1:n transformer with finite Q modelled as resistor in the primary and secondary inductors. (b) simplified transformer model used to estimate the input impedance.

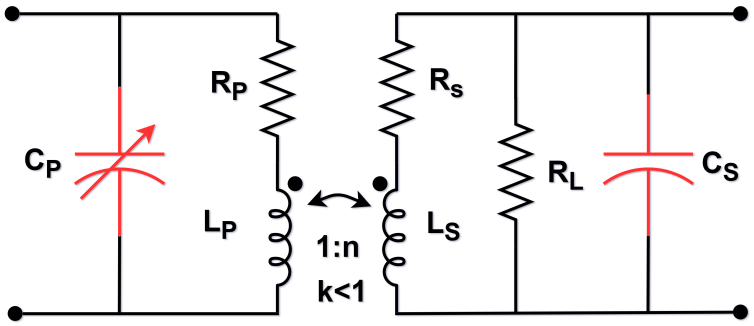


FIGURE 3.6: proposed matching network with tuning capacitors on both primary and secondary sides.

tors R_P and R_S. The load resistance, $R_L = \left(\frac{1}{g_{mp}} || \frac{1}{g_{mn}}\right)$, is given by placing in parallel the impedances seen by the two secondary coils of the trifilar balun.

The impedance at the primary for a transformer in which the secondary coil is terminated with a load R_L can be simplified to the form shown in Figure 3.5(b). The leakage inductance, $L_P(1-k^2)$, is caused by the finite coupling between L_P and L_S [30] [29]. The impedance at the secondary which consists of L_S in parallel with (R_S+R_L) can be reflected back to primary with a scaling factor of $(k/n)^2$. The reflected impedance appears in series with $L_P(1-k^2)$ and R_P. This model demonstrates that the transformer's input impedance has

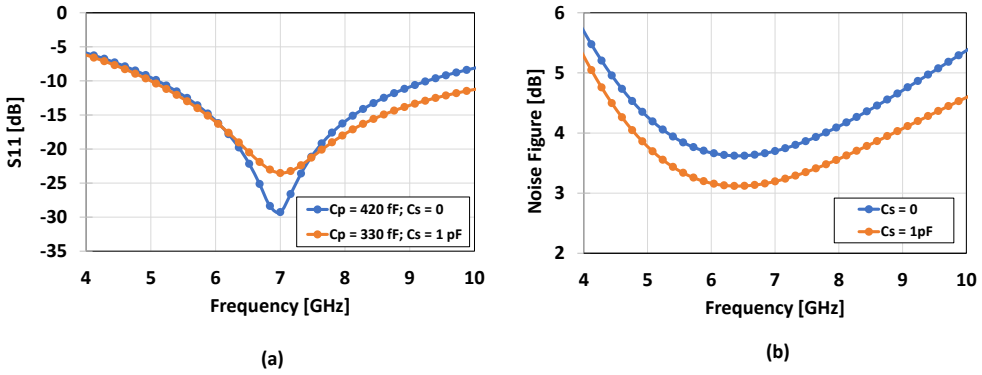


FIGURE 3.7: (a) S11 plot. (b) NF of overall LNTA.

both resistive and inductive components. Therefore, to get real impedance, the inductive components must be resonated with the capacitive element at the desired frequency. This tuning capacitor can be connected to either the primary or the secondary side of the transformer. In this design, the tuning capacitors are added on both primary and secondary sides, represented by C_P and C_S, as shown in Figure 3.6. The tuning capacitor on the primary side, C_P has little influence on the transformer insertion loss, whereas the capacitor C_S can be used to decrease the transformer losses as demonstrated in [31]. Furthermore, C_S reduces the thermal noise of the LNTA input transistors. Both cases, with and without C_S, have been simulated to achieve power matching around 7 GHz. The values of tuning capacitors are: $C_P = 420fF$ for $C_S = 0$, while $C_P = 330fF$ for $C_S = 1pF$. It is worth mentioning that C_P also contains the pad capacitance of 80 fF. Figure 3.7(a) shows the S11 plot for both cases. From 5 GHz to 9 GHz, the return loss is above 10 dB in both cases. From 6 GHz to 8 GHz, return loss is above 16 dB, corresponds to VSWR of 1.37, which meets the requirements. Figure 3.7(b) shows the overall NF of the LNTA with and without C_S. The effect of C_S is evident, as using a $C_S = 1pF$, improves the transformer insertion loss and thermal noise of the input transistors, results in the overall NF improvement of 0.5 dB at 7 GHz.

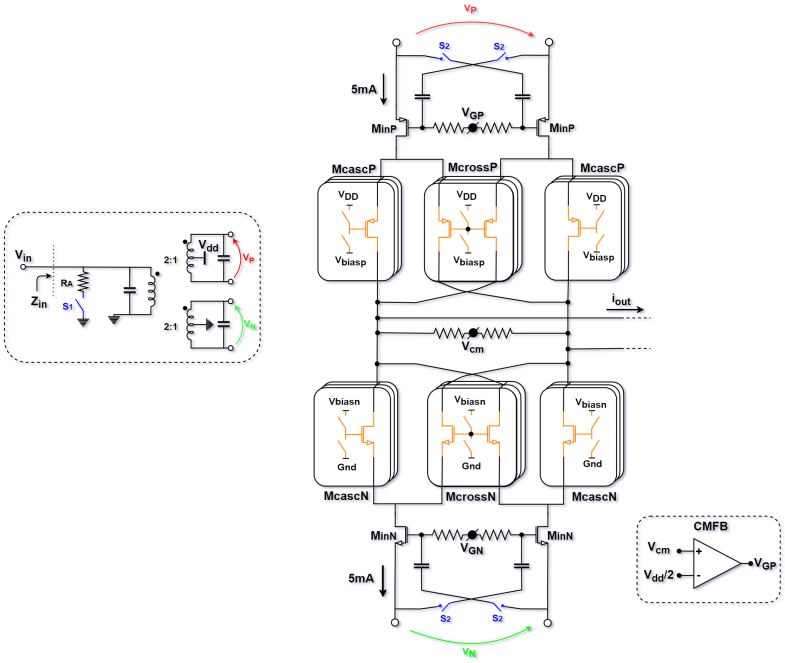


FIGURE 3.8: CG LNTA with transconductance gain variability.

3.1.3 Implementation of gain variability in LNTA

The gain variation in LNTA is implemented using current-steering technique. Figure 3.8 shows an LNTA schematic with variable gain. The transistors M_{crossP} and M_{crossN} are cross-coupled, causing the current to be steered from one branch to the other, resulting in the attenuation of the current gain. By neglecting the transformer losses, an overall transconductance gain, $G_m \triangleq \frac{i_{out}}{v_{in}}$, of this architecture can be written as:

$$G_m = \frac{g_{m,inP}}{n}\left(\frac{g_{m,cascP} - g_{m,crossP}}{g_{m,cascP} + g_{m,crossP}}\right) + \frac{g_{m,inN}}{n}\left(\frac{g_{m,cascN} - g_{m,crossN}}{g_{m,cascN} + g_{m,crossN}}\right) \quad (3.5)$$

By assuming $g_{m,inP} = g_{m,inP} = g_{m,in}$, $g_{m,cascP} = g_{m,cascN} = g_{m,casc}$, $g_{m,crossP} = g_{m,crossN} = g_{m,cross}$ and $g_{m,cross} = xg_{m,casc}$, (3.5) can be simplified as:

$$G_m = \frac{2g_{m,in}}{n}\left(\frac{1-x}{1+x}\right) \quad (3.6)$$

From (3.6), the gain of the LNTA may now be changed by altering the value of x. For this purpose, the cascode transistors and the cross-coupled transistors

are split into slices of smaller width and connected them in parallel. Each slice can be controlled separately using digital bits. For maximum gain, all cross-coupled transistors are off and all cascode transistors are on. To perform gain variability, a part of M_{cross} is turned on by connecting its gate to the appropriate bias voltage (VbiasP for PMOS and VbiasN for NMOS) and at the same time a part of M_{casc} is turned off by connecting its gate to the Vdd for PMOS and to the Gnd for NMOS. In this way, using four digital bits, a total 12 dB of transconductance gain attenuation is achieved. Figure 3.9(a) shows the gain variation of the LNTA. The maximum transconductance gain is 40 mS and it is varied down to 10 mS or a factor of 4 (12 dB) using current-steering technique. Then another 6 dB of attenuation is performed at the input of the balun using passive attenuation while maintaining the input power matching. When S_1 is off and S_2 is on, resistor R_A is disconnected and the matching condition is given by (3.4). When S_1 is on and S_2 is off, it connects R_A at the input and disconnects the cross-coupled capacitors in the LNTA. As a result, the impedance reflected back at the primary of the transformer becomes double and input impedance is given as:

$$Z_{in} = R_A || \left(\frac{n^2}{g_{m,in}} \right) \tag{3.7}$$

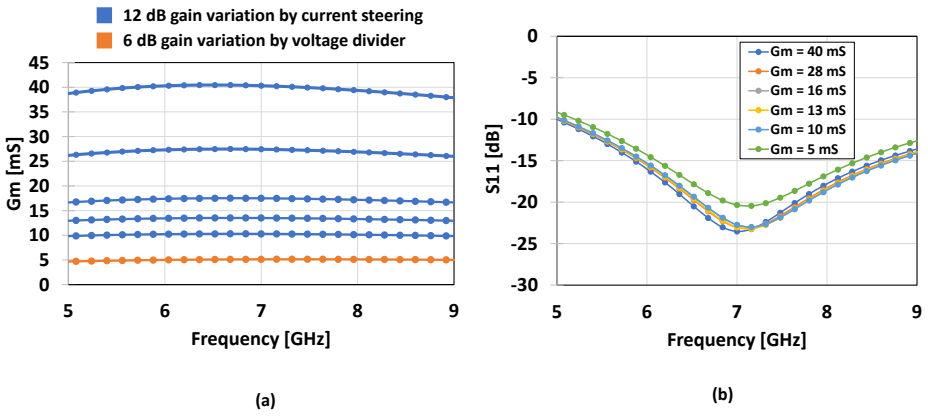


FIGURE 3.9: (a) LNTA gain variation. (b) S11 plot for each gain configuration.

To achieve input power matching, $\frac{n^2}{2g_{m,in}}$ was equal to 50 Ω in 3.4, which means $\frac{n^2}{g_{m,in}}$ becomes 100 Ω. From (4.4), by setting $R_A = 100\Omega$, the input impedance, Z_{in} becomes 50 Ω, providing input power matching and 6 dB of attenuation via the voltage divider at the input. Consequently, the transconductance gain is further reduced to 5 mS, as illustrated in Figure 3.9(a). The S11 plot for all gain configuration is shown in Figure 3.9(b).

3.1.4 Linearity and noise performance

Linearity is simulated using two tones spanning the bandwidth of the LNTA from 6 GHz to 8 GHz with a 100 MHz offset frequency. Figure 3.10(a) shows the IIP3 with respect to the frequency of IM3 tone. An IIP3 of +20.6 dBm is achieved throughout the bandwidth thanks to cross-coupled complementary CG topology. The IIP3 remains above 20.4 dBm for over wide range of frequency from 6 GHz to 8 GHz. The linearity simulations are also performed for each gain configuration. Figure 3.10(b) shows the IIP3, for two tones at 7.1 GHz and 7.2 GHz with IM3 tone falling at 7 GHz, with respect to the LNTA transconductance gain. Since the non-linearity is dominated by the input transistors, IIP3 remains constant around +20.5 dBm when gain is varied in LNTA using current steering technique. However, when the gain is reduced

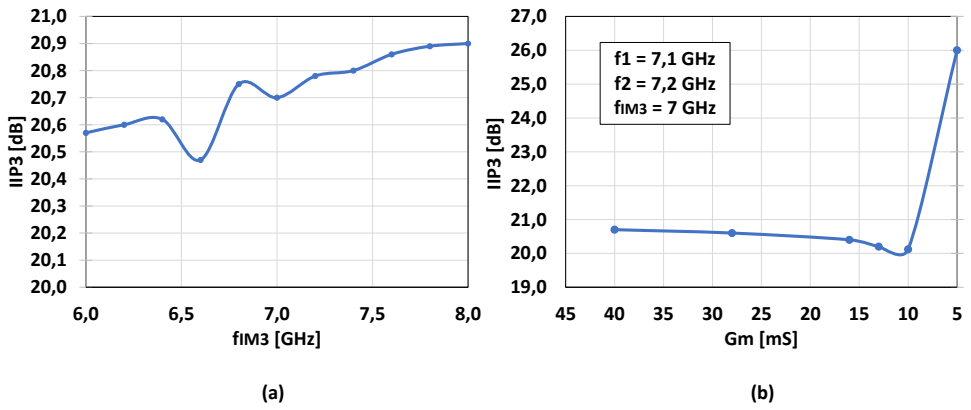


FIGURE 3.10: (a) simulated IIP3 vs IM3 tone frequency. (b) IIP3 vs LNTA transconductance gain.

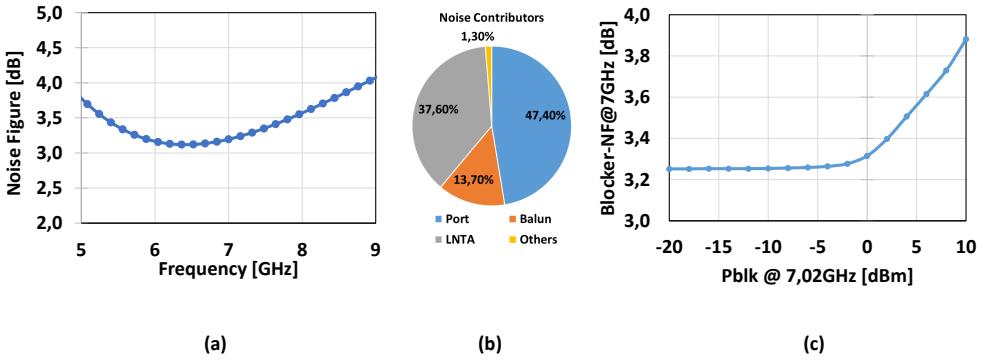
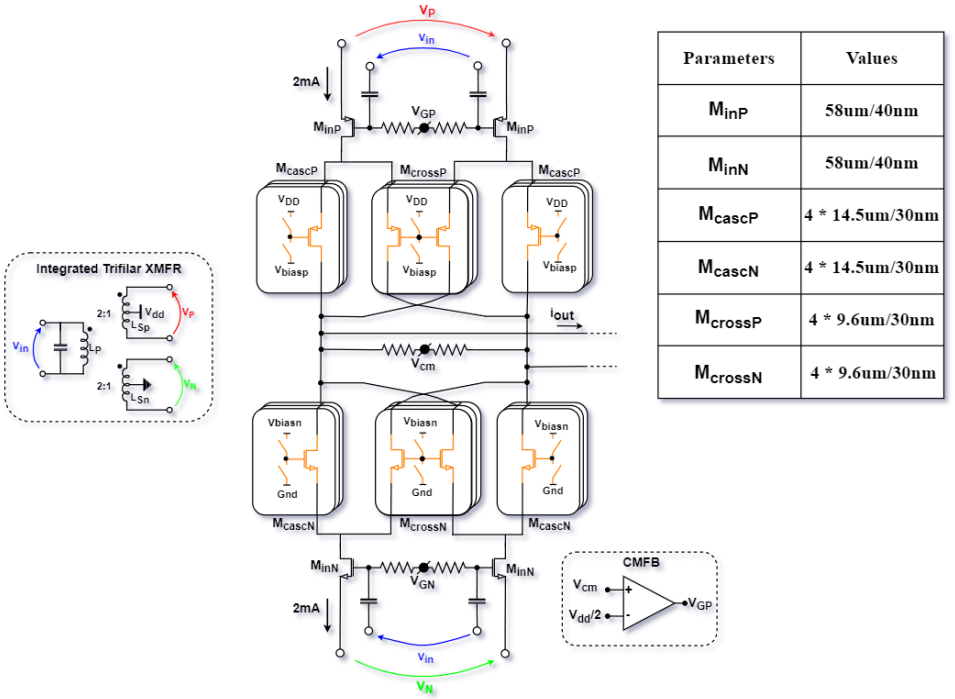


FIGURE 3.11: (a) simulated NF for maximum LNTA gain. (b) Noise contributors. (c) blocker NF.

at the input using voltage divider, the v_{gs} applied at the input transistors of the LNTA decreases, hence, increasing the IIP3 of the LNTA up to +26 dBm. The simulated NF for maximum gain configuration is shown in Figure 3.11(a). It remains below 3.5 dB throughout a wide frequency range of 6 GHz to 8 GHz. Figure 3.11(b) shows the pie chart of the noise contributors. As this topology's noise performance is restriced to the input power matching, LNTA is the major noise contributor with 37.6% of the total noise. Out of this 37.6%, input transistors contribute 60% of the noise. Balun generates 13.7% of the overall noise and remaining 1.3% is given by the parasitics in the matching network. The blocker-NF is defined as the in-band NF of the LNTA when a blocker is introduced into the LNTA. The blocker is introduced at 20 MHz offset from the desired frequency. The NF of the LNTA is barely degraded by 0.1 dB at a blocker power of 0 dBm, as illustrated in Figure 3.11(c).

3.2 Design of 2° stage CG LNTA with passive gate boosting

A complete schematic of the second stage CG LNTA is shown in Figure 3.12. The architecture of the second stage LNTA is identical to that of the first stage



Parameters	Values
M_{inP}	58um/40nm
M_{inN}	58um/40nm
M_{cascP}	4 * 14.5um/30nm
M_{cascN}	4 * 14.5um/30nm
M_{crossP}	4 * 9.6um/30nm
M_{crossN}	4 * 9.6um/30nm

FIGURE 3.12: second stage CG LNTA with passive gate boosting and current steering for gain variation.

LNTA. However, in this case, by exploiting the fact that the input signal is fully differential, a passive gate boosting is applied. In contrast to the first-stage LNTA, the capacitors at the gate of the input transistors are not cross-coupled and are instead connected to the primary side of the transformer. As a result, the g_m of the input transistors is boosted by a factor of (1+n) with respect to CG stage, where n is the turn-ratio for n:1 transformer. A similar current-steering technique is used for the gain variation. By assuming that the transconductances of the PMOS and NMOS are equal and $g_{m,cross} = x g_{m,casc}$, the transconductance gain of the second stage LNTA is given as

$$G_{m2} = \frac{g_{m,in}(n+1)}{n}\left(\frac{1-x}{1+x}\right) \tag{3.8}$$

where n is the turn ratio for n:1 transformer, $g_{m,in}$ is the transconductance gain of the input transistor and x is the ratio between M_{cross} and M_{casc} transconductance gains. Again, by altering the value of x a total 13 dB of transconductance gain variation is implemented in this stage.

3.2.1 Transformer design and characteristics

The passive-gate boosting depends on the turn ratio of the transformer. It improves the noise performance of the CG stage by boosting the g_m but on the other hand, it degrades linearity since the gate-source voltage swing likewise increased by (1+n). Thus, by considering the trade-off between linearity and noise, a 2:1 transformer is used here as well. The schematic and layout of the transformer is shown in Figure 3.13. To increase the coupling, a stacked topology is employed once again. Because the bottom layer would provide too much series resistance, it is not possible to use three layers stacking to have both symmetric secondary coils and maximum quality factor. The two secondary coils are thus realized on the same plane using metal 8, while the boosting coil is realized with metal AP as the primary coil. Having a 2:1 transformer, two secondary are created by using the exact same shape as the primary and only changing the metal layers. In contrast to the balun layout, the primary and secondary coils are in the same direction here. This layout saves area while also making it easier to connect the primary to the LNTA. The two centre taps of the secondary coils are on the other side and can easily be connected to the Vdd and Gnd. EM simulations are performed to characterize the transformer. At 7 GHz, the primary coil inductance is 1.8 nH and the Q is 9. Two inductor values for secondary coil are 500 pH each and Q is around 10. Thanks to the

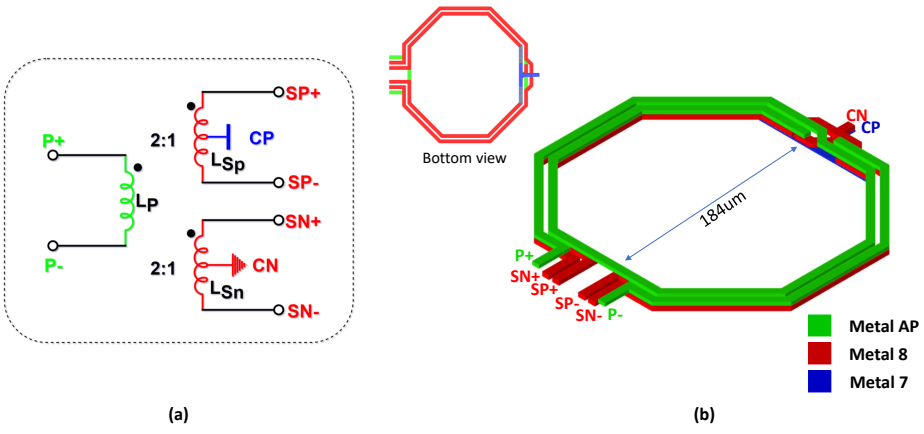


FIGURE 3.13: second stage 2:1 transformer: (a) schematic (b) layout

mutual constructrive coupling between coils, the transformer has achieved a coupling coeffiecient of 0.8.

3.2.2 DC-offset cancellation loop

The output current of the first stage LNTA is routed through the transformer. At DC, two outputs are short-circuited through the transformer's primary coil. As a result, no DC-offset propagate to the next stage. The output current of the second stage LNTA, on the other hand, is dc-coupled to the switching mixer with no capacitor in between used for DC blocking. It is done to decrease the parasitic capacitance at the output of the LNTA, since this parasitic capacitance could potentially reduces the impedance seen at the output with the increase of the f_{LO} that results in the OP-AMP noise amplification in the baseband. As there is no AC-coupling capacitor between the 2°LNTA and the mixer, the differential DC-offset at the output can create DC current that passes into mixer, resulting in 1/f noise increase. Furthermore, low frequency intermodulation tones generated by second-order non-linearity (due to mismatches) will transfer to the next stages downstream and could result in the receiver desensitization in the presence of large TIA gain in the baseband.

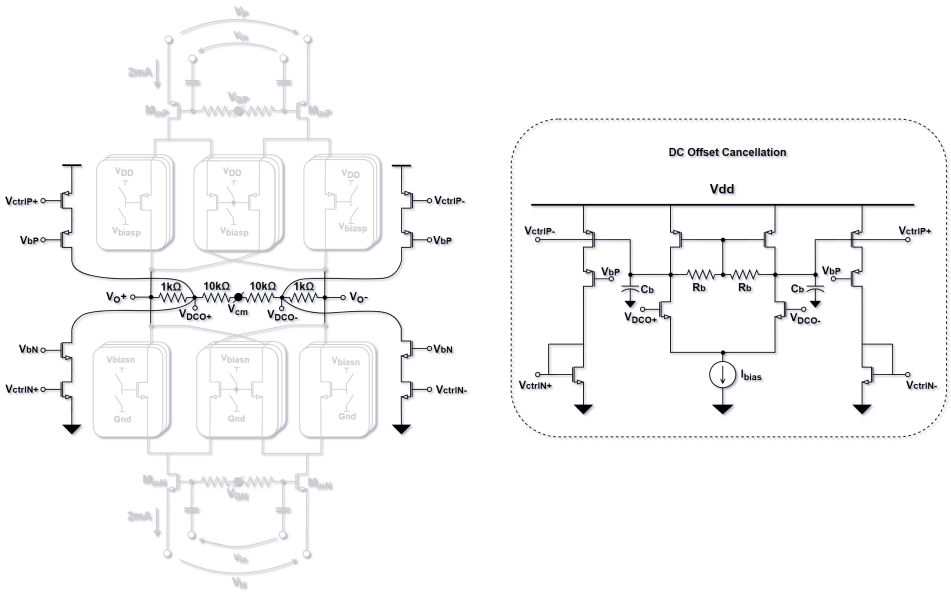


FIGURE 3.14: a DC offset cancellation loop at the output of the second stage LNTA.

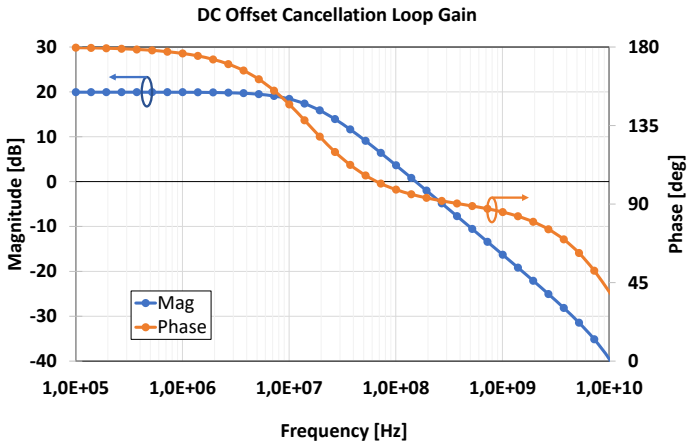


FIGURE 3.15: magnitude and phase response of the DC offset cancellation loop.

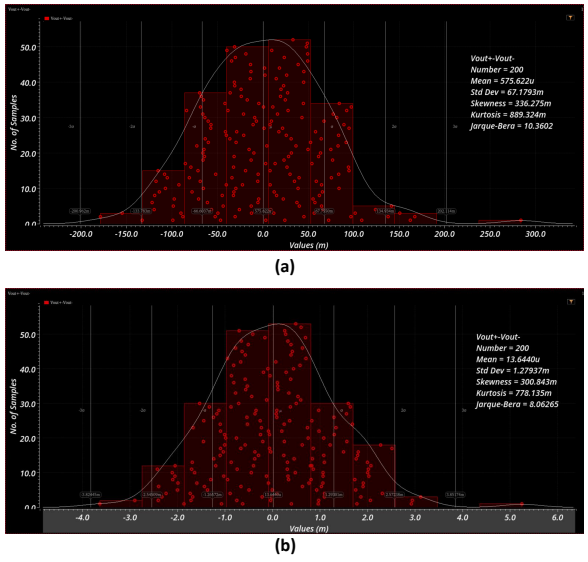


FIGURE 3.16: Montecarlo simulations of the output DC offset voltage: (a) without DC offset cancellation. (b) with DC offset cancellation.

A differential DC offset cancellation loop, as shown in Figure 3.14, is used to reduce the DC offset at the output of the 2° LNTA. To avoid loading the output with parasitic capacitance from the input transistors, DC offset is sensed at the output through a resistive divider. The loop inject the differential current with opposite polarity to the offset voltage at the same node. Figure 3.15 shows the magnitude and phase response of the loop gain. A loop gain of 20dB is achieved. For stability, a capacitor, C_b, of value 2.8 pF is connected at the drain of the input transistor. The dominant pole is at 15 MHz, given by $\omega_p = 1/(RC_b)$, where R is the parallel resistance of R_b and output resistance of nmos and pmos transistors. The loop has a phase margin of 96°. The loop gain drops to -35 dB at 7GHz, such that it does not effect the desired RF signal. Montecarlo simulations of over 200 samples are perfomed to evaluate the efficacy of the DC offset cancellation loop, taking into consideration component mismatches and process variations. The histogram of differential DC voltage $(V_o^+ - V_o^-)$ without dc offset cancellation is shown in Figure 3.16(a). An offset voltage with standard deviation of 60 mV is obtained. After implementing the loop, the standard deviation drops to 1.3 mV. According to the simulations, this offset is restricted by the mismatch between the input transistors of the loop itself.

3.3 Cascaded LNTAs simulation results

The two cascaded LNTAs are simulated with 50Ω load termination, representing mixer's input impedance, as shown in Figure 3.17. Each branch of 1°LNTA uses 5 mA dc bias current to achieve 40 mS of transconductance gain and the power matching condition at the input. A capacitor, C_x, of value 125 fF is used to resonate the second transformer around 7 GHz. Thanks to the passive-gate boosting, the 2° LNTA uses only 2 mA of bias current in each branch to provide low load impedance to the 1°LNTA and doubles the overall transconductance gain. The gain variation of two cascaded LNTAs is shown in Figure 3.18. The overall transconductance gain is 80 mS , which can be tuned down to 4.5 mS using the current-steering technique in 1°LNTA and 2°LNTA. A voltage divider at the input provide an additional 6 dB of gain variation. Figure 3.19(a) shows the NF plot for the maximum gain. At 6 GHz, the NF is about 3.5 dB and it remains below 4 dB up to 8 GHz. With respect to the only 1°LNTA, in cascaded LNTAs topology, the NF exceeds only by 0.4 dB at 7 GHz, because of the high gain provided by the 1°LNTA. Figure 3.19(b) shows the noise contribution of the each stage for output integrated noise from 6 GHz to 8 GHz when the gain is set to maximum. The noise is dominated by the 1°LNTA with 33.33%

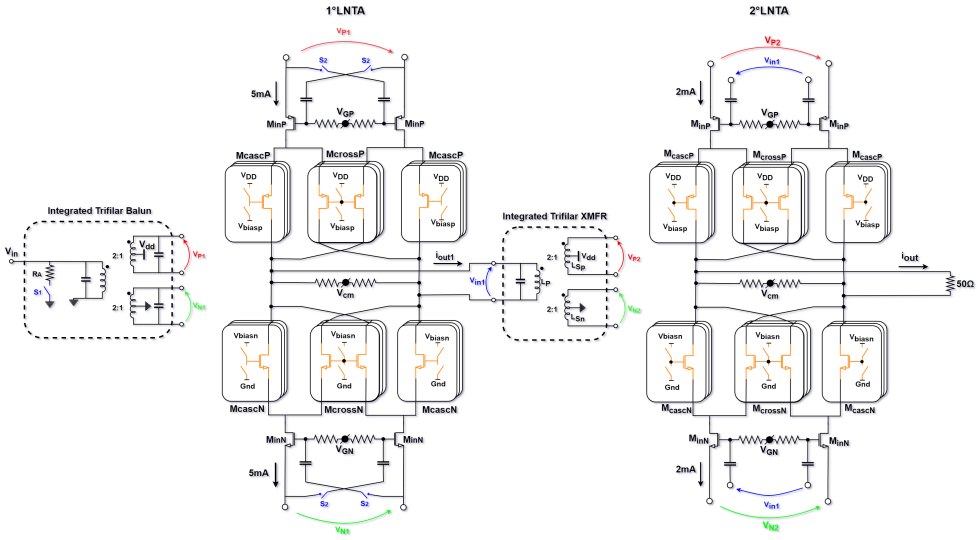


FIGURE 3.17: complete front-end composed of two cascaded LNTAs terminated with 50 Ω load.

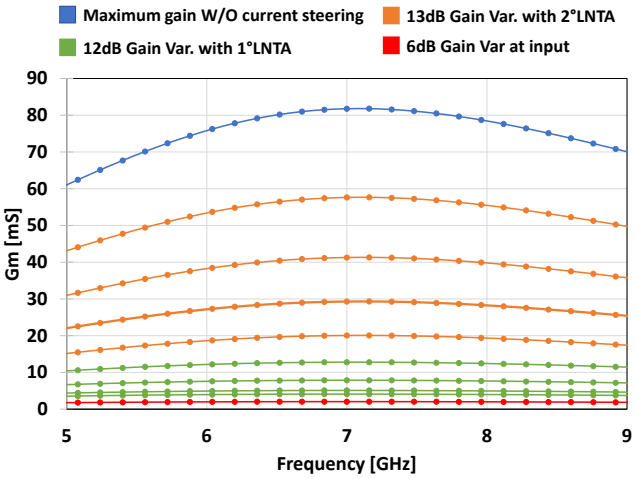


FIGURE 3.18: gain variation in the front end.

of the noise contribution, while the second stage transformer and 2° LNTA contribute just 6% of the overall noise. So, in cascaded LNTAs topology by us-

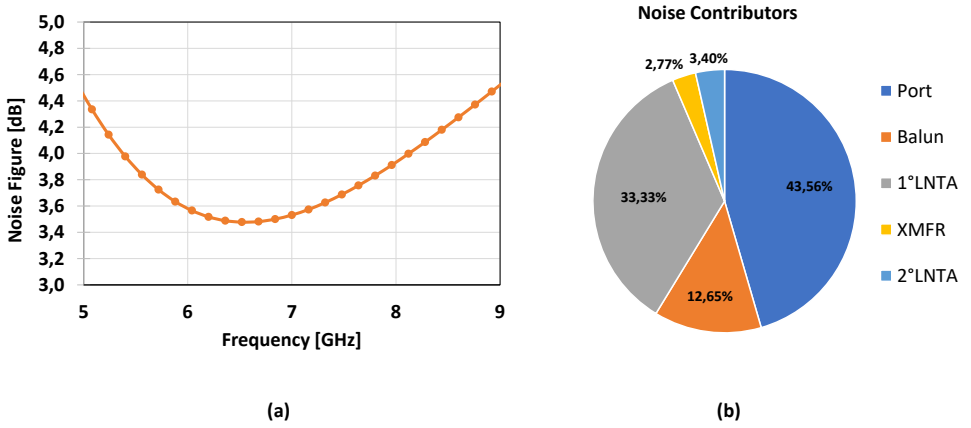


FIGURE 3.19: (a) NF of the front-end for max gain. (b) noise contributors

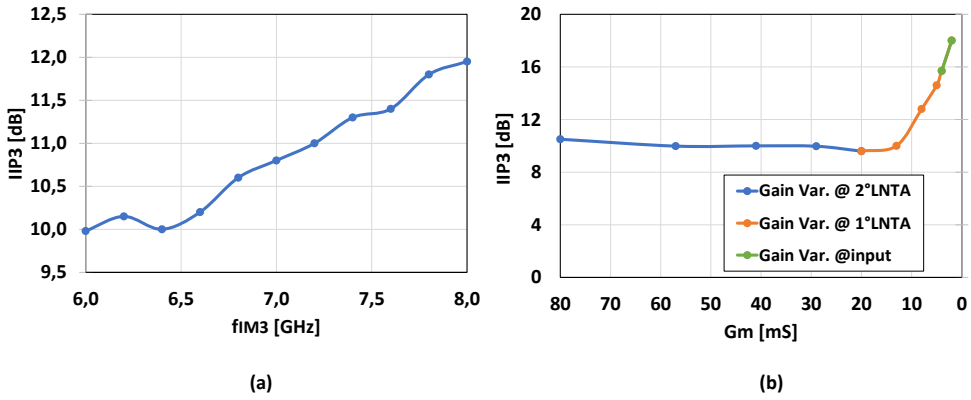


FIGURE 3.20: (a) IIP3 vs IM3 tone frequency. (b) IIP3 vs transconductance gain variation in the front-end.

ing 40% of bias current with respect to 1°LNTA, the overall transconductance gain is doubled while having no significant effect on the overall noise, thanks

to the passive gate boosting technique used in 2°LNTA. Figure 3.20(a) shows the IIP3 with respect to the IM3 tone frequency, for two tones spanning the receiver's bandwidth with 100 MHz of frequency offset. In-band IIP3 is 10.8 dBm at 7 GHz. According to the simulations, the linearity of the cascaded LNTAs is limited by the input transistors of the 2°LNTA as the increased gate to source voltage leads to heavily soliciting the transistor, thereby lowering the IIP3. Figure 3.20(b) shows the IIP3 for two tones at 7.1 GHz and 7.2 GHz and IM3 tone at 7 GHz with respect to RF transconductance gain variation. IIP3 is +10.8 dBm at maximum gain; when the gain drops from the 2° LNTA IIP3 remain constant. However, when the gain start decreasing from 1°LNTA, the gate-source voltage at the input transistors of 2°LNTA decreases as well, raising the IIP3 to +15.7 dBm. When the gain at the input reduced, IIP3 rises to +18 dBm.

Table 3.1 summarizes the overall performance of the 1° stage LNTA and cascaded LNTAs, as well as the comparisons to the state-of-the-art LNTAs. Considering only 1° stage LNTA, this work achieves a very high IIP3 of 20.5 dBm in comparison to other works, with the exception of [33], which achieves a record 36 dBm IIP3 (when one of the blockers is at a pre-defined frequency) by suppressing the Tx blocker with programmable N-path filters. This achievement, however, required a huge power consumption. In the cascaded LNTAs solution, the overall transconductance gain is doubled without degrading the noise performance. However, the IIP3 drops to 11.8 dBm as it is limited by the input transistors of 2° stage LNTA. This work is the only one with programmable transconductance gain. A very high transconductance gain of 80 mS is achieved with comparable noise and linearity performance to state-of-the-art LNTAs, except [34] where Gm is 242 mS but it burns nearly 3 times

	This Work Cascaded LNTAs	This Work 1°LNTA	TMTT 2014 [32]	RFIC 2015 [33]	TCAS-II 2015 [34]	TCAS-II 2015 [35]
Technology [nm]	28	28	45	32	65	180
Freq. [GHz]	6-8	6-8	0.1-3	0.4-6	0.6-10.5	0.05-1.2
Pdc [mW]	24	18	16	81-209	72	18
NF [dB]	3.6-3.8	3.2	3.4-5	3.6-4.9	4.5	2.9
OOB IIP3 [dBm]	11.8	20.5	12	36	6.5	7.5
Gm [mS]	80-2	40-10	34.5	NA	242	10
Gain [dB]	NA	NA	NA	10	NA	NA
External Component	NO	NO	YES	NO	NO	YES
Area [mm^2]	0.16	0.07	0.06	0.28	0.08	0.07

TABLE 3.1: Analog front-end simulated performance comparison with State-of-the-Art.

the power.

3.4 25% duty-cycle current-mode switching mixer

A current-mode passive mixer is used to perform the down-conversion. In this mixer architecture transistors act as switches, directing the injecting RF-current between the different BB branches, so as to multiply the input current by a square-wave with frequency f_{LO}, resulting in signal downconversion. To deal with differential input current both I and Q paths are equipped with double balanced mixers, such as the one shown in Figure 3.21. All of the switches are driven by 25% duty-cycle LO waveforms, such as the one shown in Figure 3.22, which also shows a 90° phase shift between signals driving the I and Q paths.

The 25% duty-cycle-LO driven current mixer has been already widely employed in the literature because it offers significant advantages over other mixer topologies, as proven by many authors [36–38]. The described solution, in particular, has a high potential for noise and linearity improvements. When it comes to noise, for example, as transistors contribute flicker noise at the mixer's output proportionally to the bias current [1, 39], passive mixers are a good choice for reducing such a noise contribution because they carry zero dc current.

The 25% duty-cycle provides significant benefits as well. This choice, in addition to boosting current down-conversion efficiency by 3 dB over its 50% duty-cycle equivalent, mitigates the influence of finite rise and fall times of the LO-waveform. Even if the LO-waveform edges have finite slope, the 0° and 180° (or 90° and 270°) waveforms never overlap, and the associated branches never on at the same time. As demontrated in [38], this feature provides considerable improvements in terms of noise and blocker handling capability.

As can be seen from the clock waveforms in Figure 3.22, the I and Q paths are never on at the same time. This results in a higher impedance at the mixer's BB port, which becomes approximately equals to the output impedance of the LNTA, rather than the parallel combination of such impedance with the quadrature mixer's on-resistance, which is characteristic of a 50% duty-cycle implementation. This gives significant advantage in terms of noise reduction. In reality, as will be demonstrated in chapter 4, if the BB channel-select filter is driven with low-impedance, the OP-AMP input-referred noise is amplified. Un-

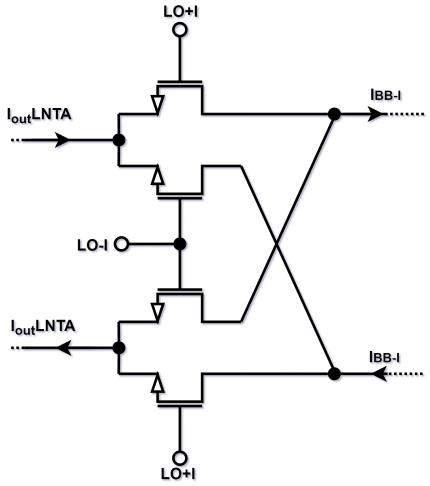


FIGURE 3.21: I-side mixer schematic.

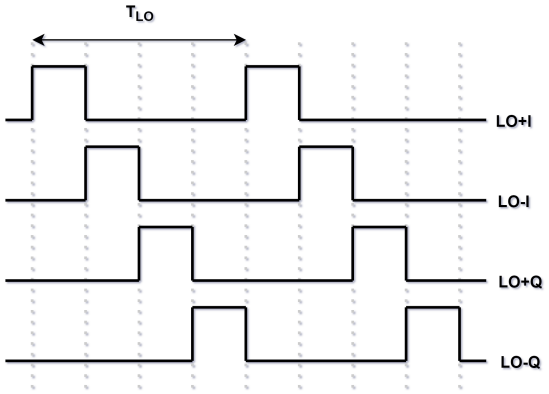


FIGURE 3.22: Quadrature phase 25% duty-cycle LO waveforms.

fortunately, the output impedance of the LNTA is lowered by its output parasitic capacitance. This capacitance determines an equivalent driving impedance for the BB section, which is proportional to $1/(2f_{LO}C_{out})$, where C_{out} is the output capacitance of the LNTA, as computed in [39], and examined in further detail in [40], exploiting a switched-capacitor model.

The aforementioned driving impedance is also crucial for BB linearity, because a low value for such impedance causes the BB filter's loop gain to

be decreased, which significantly affects its linearity performance. In general, current-mode mixers enable high linearity performance of the overall receiving chain. If the baseband is appropriately designed, the voltage swing across the switches and on the non-linear parasitic capacitance at the LNTA output are reduced, resulting in a reduction in the injection of non-linear terms.

The mixer used in this receiver design is made up of NMOS switching transistors. In comparison to PMOS switches, such switches can offer the same on-resistance with a smaller channel width, decreasing capacitive loading for the clock generation circuit. The channel width of the transistor, W, was optimized for linearity and noise to be 40μm, resulting in an estimated equivalent on-resistance of about $R_{on} = 20\Omega$.

3.4.1 Biasing

The biasing schematic of one transistor of the switching mixer is shown in Figure 3.23. In order to get the most possible headroom for voltage swings, the common-mode voltage, V_{cm}, at the mixer's input and output is adjusted to $V_{dd}/2$ utilizing CMFB loops. The bias voltage, V_b, at the transistor's gate is set to $V_{cm} + V_{LO}/4$ to ensure that the transistor turns on strongly. If the LO square-wave goes from 0 to V_{LO}, the gate of the transistor switch between $+\frac{V_{LO}}{2}$ and $-\frac{V_{LO}}{2}$ around DC offset voltage $V_b + V_{avg}$. For the case of 25% duty-cycle LO square-wave, V_{avg} is given as $\frac{V_{LO}}{4}$. When the transistor is on, the

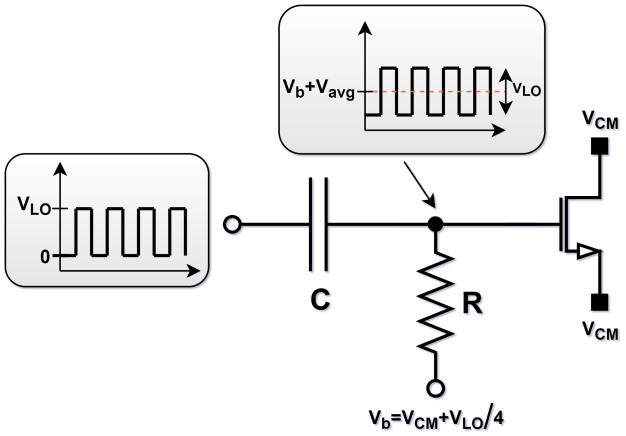


FIGURE 3.23: simplified schematic of transistor biasing in a mixer.

voltage at gate goes to $V_{cm} + V_{LO}$. By considering the v_{gs} of the transistor, it will see full V_{LO} swing. When transistor is off, the gate voltage goes to V_{CM} and conseguently, v_{gs} goes to 0. As a result, the DC bias level at the gate of the switches is set such that they operate near the threshold of conduction, resulting in lower average on-resistance and improved mixer linearity, gain and noise performance.

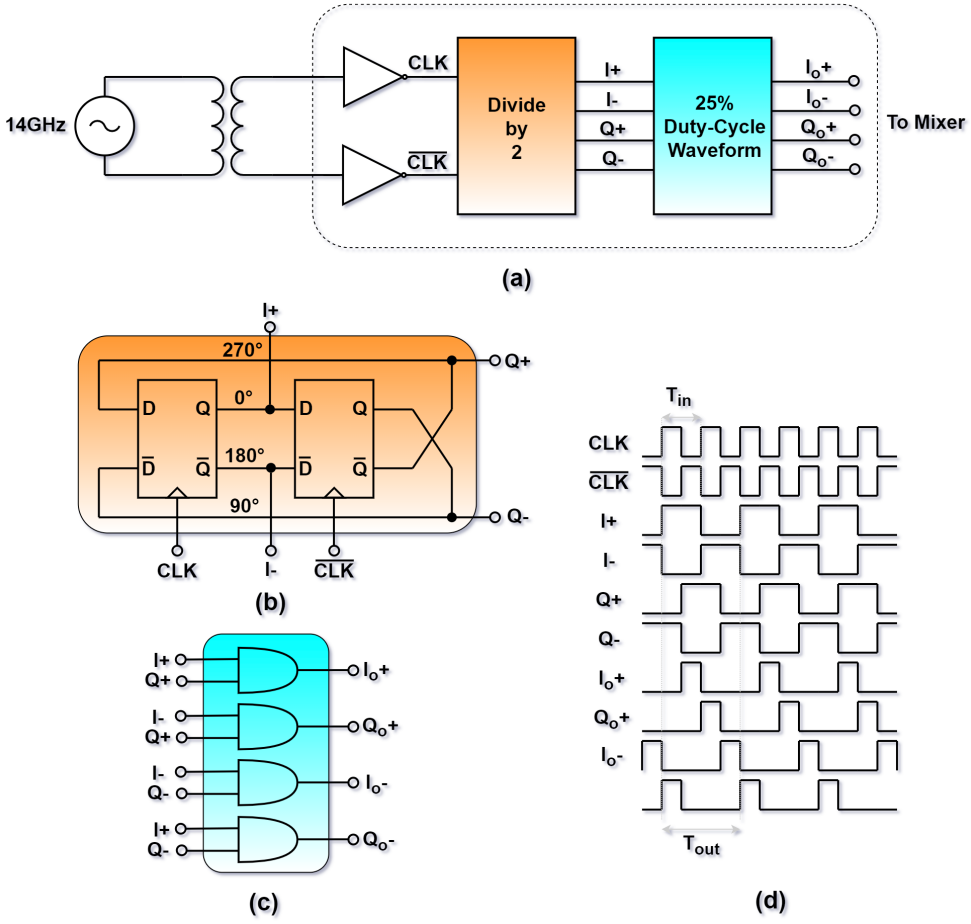


FIGURE 3.24: (a) LO generation circuitary. (b) Frequecy divider. (c) AND gates to generate 25% duty-cycle. (d) signal waveforms.

3.4.2 25% duty-cycle divider

The LO generation path of the mixer is shown in Figure 3.24(a). The first two self-biased inverters in parallel serves as input buffer, reshaping the distorted high-frequency clock waveform caused by pad parasitics while simultaneously providing input matching. A symmetric LO waveform is important for maintaining balanced switch operation so that the switching quad does not worsen the mixer noise figure while also producing second-order intermodulation products. The division by 2 block is implemented using two cascaded D flip-flops in feedback as shown in Figure 3.24(b). They generate I and Q signals with a duty-cycle of 50%. Then four AND gates are used to generate a 25% duty-cycle LO signals.

In conclusion, this chapter, presents a design of very linear wideband analog front-end. It's made up of two LNTA's in a cascade to achieve very high Gm of 80 ms which is programmable down to 2 ms. The presented analog front-end provides state-of-the-art performance in terms of noise and linearity. In the final section, a current-mode switching mixer with a 25% duty-cycle is presented. The next chapter will go over the design of the receiver baseband.

Chapter 4

Design of Baseband for 5G Wireless Receiver

Abstract
The design of the baseband is covered in this chaper. As previously stated, two baseband paths are employed to cover a large RF bandwidth ranging from 50 MHz to 2 GHz. The chapter starts with the design of the high-frequency baseband (HF-BB) path. It consists of an 1GHz bandwidth open-loop current-mode filter followed by a wideband TIA. A special emphasis will be given on the design of an open-loop filter, where the concept of using negative capacitance to improve the quality factor and out-of-band selectivity of the filter will be thoroughly explored. The last section of the chapter is devoted to the design of low-frequency baseband (LF-BB) path, which consists of a Rauch filter and an output buffer. Each baseband block has been prototyped and tested as a stand-alone block. The measurement results of each block will be presented.

4.1 High Frequency Baseband Path

In Chapter 2, it is mentioned that HF-BB path need to cover RF bandwidth ranging from 800 MHz to 2 GHz. In order to cover this range, a baseband filter with a bandwidth in the GHz range is required. In a traditional BB architecture, the mixer is followed by a closed-loop TIA, as shown in Figure 4.1. Despite the fact that modern filters based on Operational Transconductance Amplifier (OTA) can have good linearity and low noise, for filter bandwidth exceeding a few hundred MHz, the OTA gain-bandwidth product (GBW) need to exceed several GHz, resulting in a very large current consumption [41]. In addition, it requires a large capacitor termination to filter the clock harmonics.

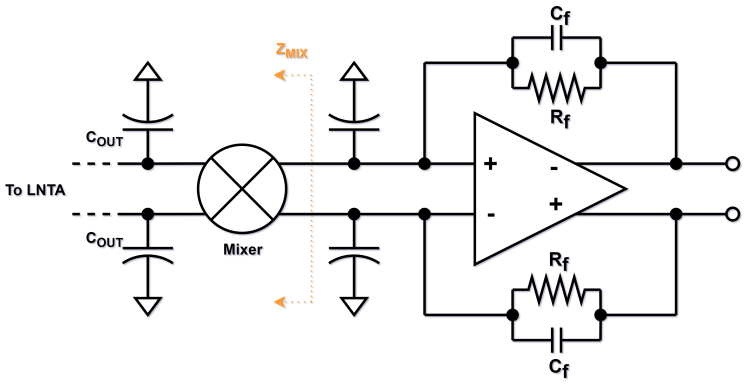


FIGURE 4.1: traditional baseband architecture in current-mode receiver.

As explained in [39], at low frequencies, the down-converted impedance at the output of the mixer (assume to be a current mode passive one) can be written as

$$Z_{mix}(f_{RF}) \approx \frac{1}{4f_{RF}C_{out}} \tag{4.1}$$

From (4.1), it is clear that as RF frequency increases, the TIA driving impedance goes down. This both lowers the loop gain of the TIA and results in a stronger amplification of the OTA noise. Figure 4.2 shows a simplified design of an OTA to demonstrate the noise amplification effect at DC. $\overline{V}^2_{n,in}$ represents the input referred noise of the OTA and R_{mix} denotes the downconverted impedance at the mixer's output at DC. The noise current $\bar{i}^2_n$ generates

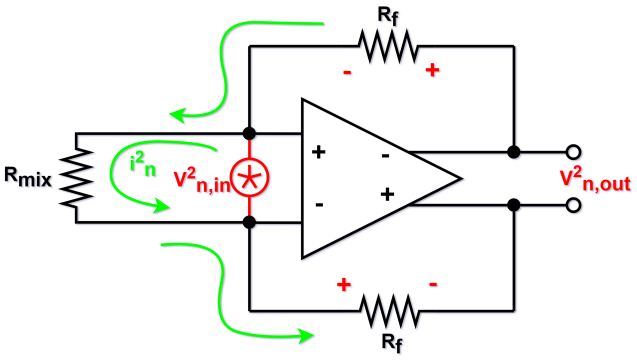


FIGURE 4.2: simplified schematic of TIA to show noise amplification at low frequency.

by $\overline{V}_{n,in}^2$ is given as

$$\bar{i}_n^2 = \frac{\overline{V}_{n,in}^2}{R_{mix}^2} \tag{4.2}$$

This noise current flows through the feedback resistors, R_f and conseguently the noise at the output of the TIA is given as

$$\begin{aligned} \overline{V}_{n,out}^2 &= \frac{\overline{V}_{n,in}^2}{R_{mix}^2} R_f^2 + \overline{V}_{n,in}^2 + \frac{\overline{V}_{n,in}^2}{R_{mix}^2} R_f^2 \\ &= \overline{V}_{n,in}^2 \left(1 + \left(\frac{2R_f}{R_{mix}}\right)^2\right). \end{aligned} \tag{4.3}$$

From (4.3), it can be seen that as the mixer's downconverted output impedance decreases, it amplifies the noise of the TIA at the output.

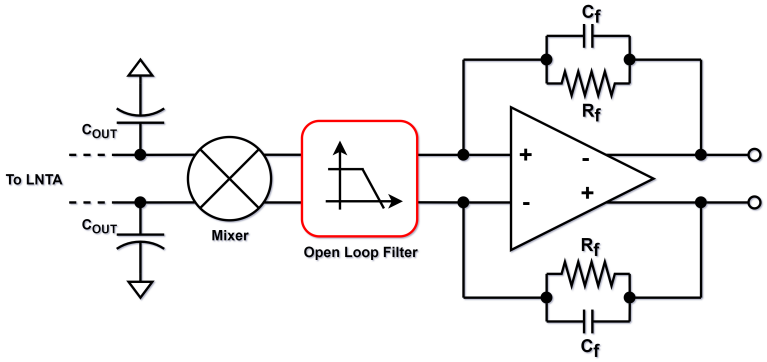


FIGURE 4.3: introducing an open loop filter in front of the baseband.

As the channel bandwidths and carrier frequency increases, it becomes very challenging to fulfil the requirements of an OTA-based TIA. The solution adopted in this work is to use an open-loop second-order filtering current-mode amplifier in front of an OTA-based first-order TIA (see Figure 4.3) that drives the following stages. The open-loop current amplifier filters the interferers in the current-domain and offers a low-input impedance to the mixer and a high driving impedance to the following TIA. As a result, the requirements of the closed-loop TIA are highly relaxed. The design of the open-loop filter will be discussed in detail in the following subsections.

4.1.1 Common-Gate Filter

An open-loop filter promising for large bandwidth can be implemented using a Common-Gate (CG) stage. One potential CG solution was originaly presented in [42], to accomplish wideband RF filtering for TV tuners. The operating principle of the filter is graphically explained in Figure 4.4. A simplified schematic of CG stage is shown in Figure 4.4(a) where the input signal is provided using an equivalent Norton current generator with finite impedance, R_s, which models, in a very simplified manner, the driving impedance provided by the LNTA and mixer.

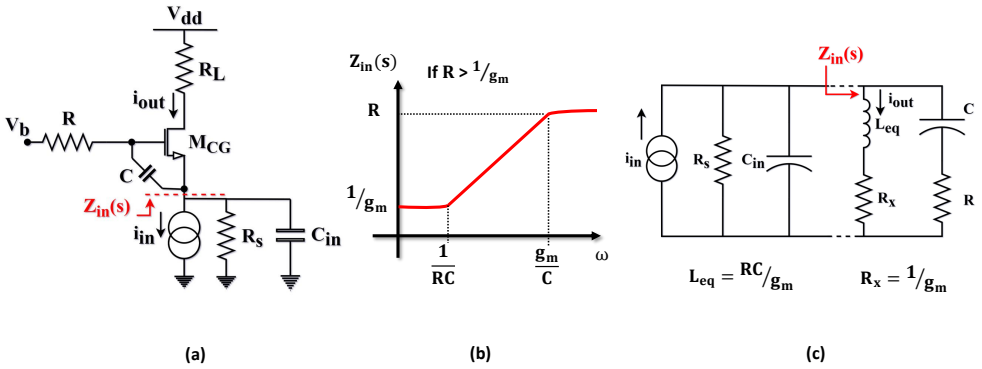


FIGURE 4.4: (a) schematic of CG stage with feedforward capacitor C. (b) input impedance Z_{in} at source of CG stage. (c) equivalent RLC model.

The frequency behaviour of the circuit can be described by determining an input impedance, Z_{in}, looking into the source of transistor M_{CG}. It can be computed as follows:

$$Z_{in}(s) = \frac{1}{g_m} \frac{(1 + sCR)}{\left(1 + s\frac{C}{g_m}\right)} \tag{4.4}$$

The CG operates as a simple cascode with an input impedance, $Z_{in} = \frac{1}{g_m}$, for very low frequency signals. At higher frequencies, capacitor, C, shunts the v_{gs} of the CG transistor, and if it is ensured that $R > 1/g_m$, it creates an inductive impedance behaviour. Figure 4.4(b) shows a graphic representation

of impedance Z_{in}. When the capacitor C_{in} is connected in parallel with Z_{in}, the circuit resembles the RLC network shown in Figure 4.4(c). The equivalent inductance is determined by the slope of Z_{in}, $L_{eq} = \frac{RC}{g_m}$, with its losses represented by R_x in an equivalent model whose value is $\frac{1}{g_m}$. It is simple to show that the current flowing through the equivalent inductor is a 2^{nd}-order low-pass filtered version of i_{in}. The exact transfer function of the resulting biquad can then be calculated as:

$$T_{CG}(s) = \frac{i_{out}}{i_{in}} = \frac{g_m R_s}{1 + g_m R_s} \frac{1}{1 + s(\frac{RC + R_s C + R_s C_{in}}{1 + g_m R_s}) + s^2(\frac{RC R_s C_{in}}{1 + g_m R_s})} \tag{4.5}$$

where

$$\omega_o = \sqrt{\frac{(1 + g_m R_s)}{RC R_s C_{in}}} \tag{4.6a}$$

$$Q = \frac{\sqrt{(1 + g_m R_s)(RC R_s C_{in})}}{RC + R_s C + R_s C_{in}} \tag{4.6b}$$

In (4.5), (4.6a) and (4.6b) g_m is the transconductance of the transistor M_{CG}, while the other parameters are indicated in Figure 4.4(a). From (4.6b), if $\sqrt{\frac{R_s}{R}} << \sqrt{\frac{R}{R_s}}$, the expression of Q can be further simplified as

$$Q = \frac{\sqrt{(1 + g_m R_s)(RC R_s C_{in})}}{RC + R_s C + R_s C_{in}} \approx \frac{\sqrt{1 + g_m R_s}}{\sqrt{\frac{RC}{R_s C_{in}}} + \sqrt{\frac{R_s C_{in}}{RC}}} \tag{4.7}$$

From (4.7), the denominator term can be seen as $x + \frac{1}{x}$, which has a minima for $x = 1$. This imposes a condition to achieve maximum Q which is $RC = R_s C_{in}$. Furthermore, the Q is proportional to the driving impedance R_s in the numerator. This aspect is especially important in 5G, because the equivalent driving impedance given by the mixer tend to reduce as the LO frequency increases which limits the maximum achievable Q for this CG topology. This effect may also be observed intuitively in Figure 4.4(c) where the driving impedance R_s appears in parallel to the equivalent inductor given by the CG, potentially lowers the Q of the biquad's complex-conjugate (CC) poles.

In order to calculate the power spectral density of the parallel noise source at the input of the filter, the noise contribution from the every component in the circuit need to be evaluated. The schematic shown in Figure 4.5 can be used for the noise analysis where all the noise sources are highlighted. The

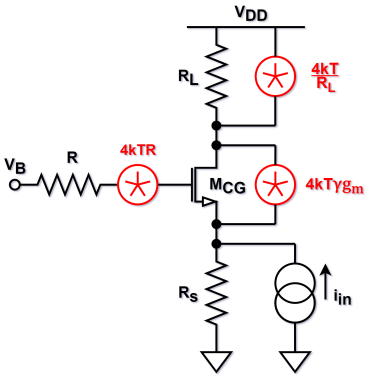


FIGURE 4.5: simplified schematic for low frequency noise analysis of CG.

power spectral density of the parallel noise source at the input, denoted by $\frac{\overline{di^2_{n,in}}}{df}$, can be calculated by referring the noise sources to the filter input. Thus,

$$\frac{\overline{di^2_{n,in}}}{df} = \frac{\overline{di^2_{n,gm}}}{df} + \frac{\overline{di^2_{n,R}}}{df} + \frac{\overline{di^2_{n,RL}}}{df} \tag{4.8}$$

where

$$\frac{\overline{di^2_{n,gm}}}{df} = \frac{4\kappa T\gamma}{g_m R_s^2} \tag{4.9a}$$

$$\frac{\overline{di^2_{n,R}}}{df} = \frac{4\kappa TR}{R_s^2} \tag{4.9b}$$

$$\frac{\overline{di^2_{n,RL}}}{df} = \frac{4\kappa T}{R_L}\frac{(1+g_m R_s)^2}{g_m^2 R_s^2} \tag{4.9c}$$

To provide a low input impedance, a large current is required to enhance the g_m of the CG. This might be a problem from noise point of view since the restricted voltage supply forces a lower resistance R_L, which makes its noise contribution more dominant as can be seen from (4.9c)

In conclusion, it can be stated that CG topology can achieve very wide bandwidth but suffers from two main drawbacks: 1) a low in-band input impedance requires a large current in the CG branch, with considerable noise from the load resistance R_L. 2) the low driving impedance limits the achievable Q of the biquad poles and consequently the selectivity. These two points will be addressed in the following sections by adding some circuit modifications.

4.1.2 Regulated Cascode Architecture

To overcome the first issue, the topology known as Regulated-Cascode architecture can be utilized. This architecture is easily achieved by connecting the amplifier A to the CG stage's source and gate. The low-frequency input-impedance of the resulting circuit is equal to $1/g'_m(1+A)$, as shown in Figure 4.6. When compared to the CG, this input impedance value is lowered by a factor of (1+A), implying that the current in the CG branch of the regulated cascode may be reduce by the same amount while attaining an input impedance equal to the CG filter.

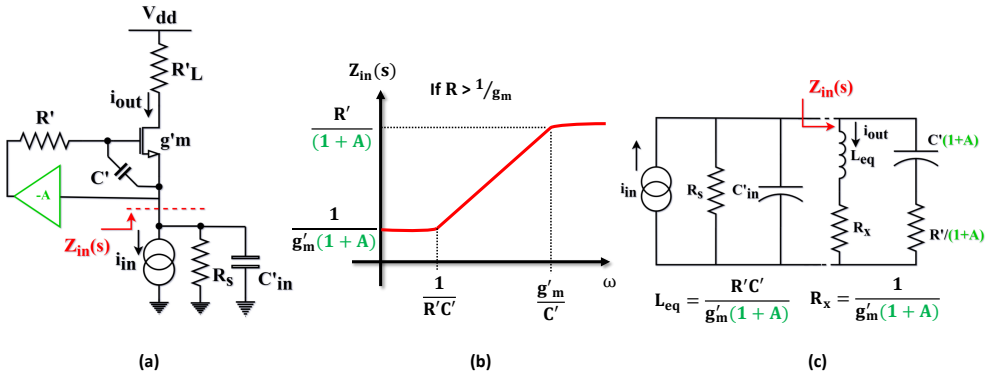


FIGURE 4.6: (a) regulated cascode architecture with amplifier A in feedback. (b) input impedance Z_{in} at source of CG stage. (c) equivalent RLC model.

The input impedance, Z_{in}, has the same frequency behaviour as the CG filter, with the exception that the impedance associated with CG, R and C is scaled by (1+A), as illustrated in Figure 4.6(b). The resulting transfer function (i_{out}/i_{in}) of the regulated cascode architecture is given as

$$T_{reg-casc}(s) = \frac{i_{out}}{i_{in}} = \frac{g'_m R_s(1+A)}{1+g'_m R_s(1+A)} \cdot \frac{1}{1+s\left(\frac{R'C'+R_sC'(1+A)+R_sC'_{in}}{1+g'_m R_s(1+A)}\right)+s^2\left(\frac{R'C'R'_sC'_{in}}{1+g'_m R_s(1+A)}\right)} \tag{4.10}$$

where

$$\omega_o = \sqrt{\frac{(1 + g'_m R_s(1 + A))}{R'C'R_sC'_{in}}} \tag{4.11a}$$

$$Q = \frac{\sqrt{(1 + g'_m R_s(1 + A))(R'C'R_sC'_{in})}}{R'C' + R_sC'(1 + A) + R_sC'_{in}} \tag{4.11b}$$

Figure 4.6(c) shows that the amplifier A reduces the effect of the driving impedance R_s by scaling down the impedance of the equivalent RLC network that models Z_{in}.
The regulated cascode architecture may also provide benefits in terms of noise. Similarly to the CG filter, the noise contribution for each component in (4.8) for regulated cascode is as follows:

$$\frac{\overline{di^2_{n,gm'}}}{df} = \frac{4\kappa T\gamma}{(1 + A)^2 g'_m R_s^2} \tag{4.12a}$$

$$\frac{\overline{di^2_{n,R'}}}{df} = \frac{4\kappa TR'}{R_s^2(1 + A)^2} \tag{4.12b}$$

$$\frac{\overline{di^2_{n,RL'}}}{df} = \frac{4\kappa T}{R'_L} \frac{(1 + (1 + A)g'_m R_s)^2}{(g'_m R_s(1 + A))^2} \tag{4.12c}$$

$$\frac{\overline{di^2_{n,A}}}{df} = \frac{4\kappa T}{g_{m,A}R_S^2} \frac{(A)^2}{(1 + A)^2} \tag{4.12d}$$

where amplifier, A, is assumed to be a simple Common-Source (CS) with transconductance of $g_{m,A}$ and load resistance of R'. Some assumptions can be made in order to compare the noise of two topologies. If the input impedance of the two topologies is considered to be the same, i.e. that $g'_m = g_m/(1 + A)$. Second, it is expected that the current saved in the Regulated Cascode CG branch may be utilized in A, resulting in $g_{m,A} = g_m \cdot A/(1 + A)$ and $R' = (1 + A)/g_m$. Third, it is assumed that voltage drop on R_L is constant, such

that $R'_L = R_L/(1+A)$. Equations (4.12) can be written as

$$\frac{\overline{di^2_{n,gm'}}}{df} = \frac{4\kappa T\gamma}{(1+A)g_m R_s^2} \tag{4.13a}$$

$$\frac{\overline{di^2_{n,R'}}}{df} = \frac{4\kappa T}{g_m R_s^2(1+A)} \tag{4.13b}$$

$$\frac{\overline{di^2_{n,RL'}}}{df} = \frac{4\kappa T}{R'_L(1+A)}\frac{(1+g_m R_s)^2}{(g_m R_s)^2} \tag{4.13c}$$

$$\frac{\overline{di^2_{n,A}}}{df} = \frac{4\kappa T}{g_m R_S^2}\frac{A}{1+A} \tag{4.13d}$$

The noise contributed by the CG transistor is decreased by a factor of (1+A) in the regulated cascode architecture, as shown in (4.13a). However, in the latter topology, the extra noise supplied by amplifier, A, must also be considered. The overall noise generated by the (4.13a) and (4.13d) results exactly equal to (4.9a), implying that the regulated cascode produces no advantage in transistor noise under the specified assumptions. On the contrary (4.9c) and (4.13c) show that the noise contributed by the load resistor, R_L, is reduced by the factor of (1+A).

An open-loop filter based on regulated cascode architecture is recently reported in [43], where it is incorporated in a mixer-first receiver and has a baseband bandwidth of 130 MHz. Such a solution however fails to work when the baseband frequency exceeds a few hundred MHz. One of the reasons is that the auxiliary amplifier (A in Figure 4.6(a)) used in [43], requires a high g_m to reduce its noise contribution, resulting in a lower value of R' to have appropriate boosting gain. Correspondingly C' must be increased in order to maintain a constant pole frequency at ω_0. As C' increases and becomes comparable to C'_{in}, it degrades the filter Q. Furthermore, in order to achieve high g_m, the amplifier A dissipates a very large power. In this work, a different approach is adopted which enables to extend the bandwidth upto 1 GHz and gives better noise performance with less power consumption.

4.1.3 Regulated Cascode Filter with Cross-Coupled Diodes

In the proposed architecture, the amplifier, A, is substituted with cross-coupled diode-connected transistors, as shown in Figure 4.7. This corresponds to a gain A of -1, which reduces the in-band impedance by a factor of two or, alternatively, reduces the noise of the load resistor, R_L, by half for the same in-band

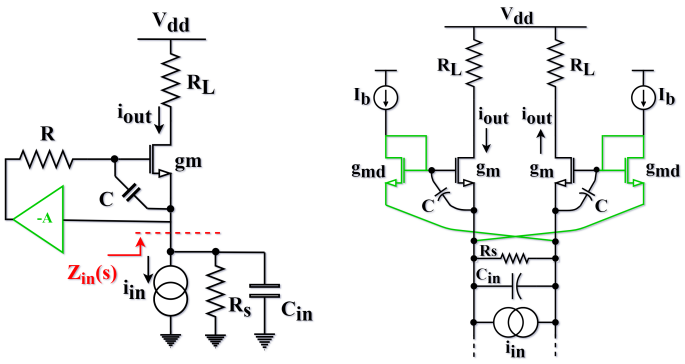


FIGURE 4.7: implementing an amplifier, A, with cross-coupled diode-connected transistors.

impedance. In addition, this solution permits to extend the filter bandwidth up to GHz range without compromising the filter Q. Because the diode-connected mosfets are also utilized to bias the CG stage, there is no additional power dissipation. The resistor, R, in the solution is given by $1/g_{md}$ where g_{md} is the transconductance of the diode-connected mosfet. The g_m/g_{md} ratio is set to 5 to achieve inductive in-band impedance in the CG stage. The noise generated by the diode-connected transistor limits the lower value of g_{md}. It can be deduced from (4.9b) that when g_{md} decreases, its noise contribution starts becoming dominating. The transistor's are sized so that the noise of the diode-connected MOS remains lower than the noise of the CG transistor. The upper limit for the value of g_{md}, on the other hand, is bounded by the power dissipation in the filter.
With this approach, however, either a higher Q can be achieved by double the g_m with same bias current in relation to CG topology or the noise from the load resistor can be reduced by selecting the same g_m with less bias current. In addition, the Q is still primarily constrained by the driving impedance R_s. So, in order to further improve the Q of the filter, a negative capacitance circuit is employed, which will be explained in the following subsection.

4.1.4 Negative Capacitance to enhance Q and OOB selectivity

To address the second issue related to CG topology, namely the limited achievable Q due to low driving impedance, a negative capacitance is added at the input of the filter using the Miller effect within a positive feedback loop, as was done in [43], [44] and [45]. However, both [44] and [45] employ op-amp

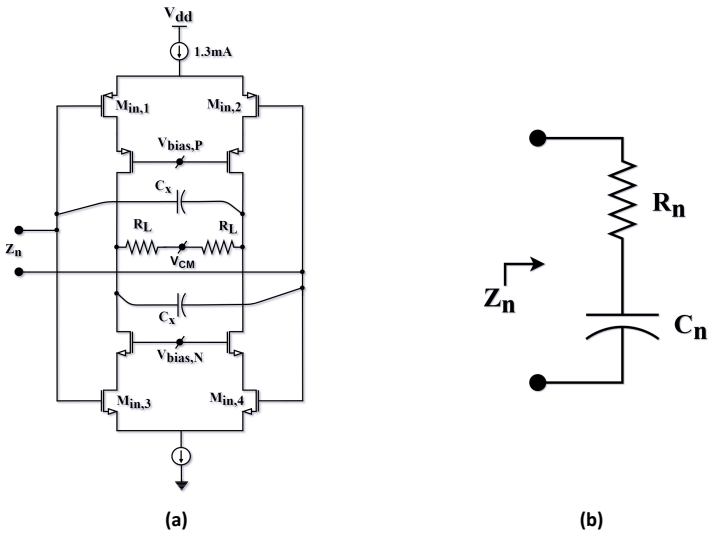


FIGURE 4.8: (a) negative capacitance circuit. (b) an equivalent model.

based solution, which need extremely high power consumption even when the filter bandwidth is just 5% of the one used here. On the other hand compared with [43], the required amplification is reduced allowing to maintain its value constant in frequency beyond 1 GHz. The actual impementation is shown in Figure 4.8(a). Two capacitors, C_x, are connected between the inputs and the non-inverting outputs of the complementary (p-n) amplifier loaded by resistor R_L. The single-ended impedance, $Z_{n,SE}$, implemented at the input is stated as

$$Z_{n,SE}(s) = \frac{1}{sC_x(1 - g_m R_L)} + \frac{R_L}{(1 - g_m R_L)} \tag{4.14}$$

If the voltage gain of the amplifier, $g_m R_L$, is greater than one, the impemented impedance can be seen as the series of negative capacitance $C_n = (1 - g_m R_L)C_x$ and a negative resistance $R_n = R_L/(1 - g_m R_L)$, as shown in Figure 4.8(b).

The effect of the negative capacitance is analyzed placing at the circuit input C_n in series with R_n, as illustrated in Figure 4.9(a). In place of having a $Z_{C_{in}} = 1/sC_{in}$ in shunt with $Z_{in}(s)$, i.e. the source impedance of the CG, it has C_{in} in shunt with C_n and R_n whose impedance $Z_{c,tot}$ is given by:

$$Z_{c,tot}(s) = \frac{1}{s(C_{in} + C_n)} \frac{(1 + sC_n R_n)}{\left(1 + \frac{sC_{in}C_n R_n}{C_{in}+C_n}\right)} \tag{4.15}$$

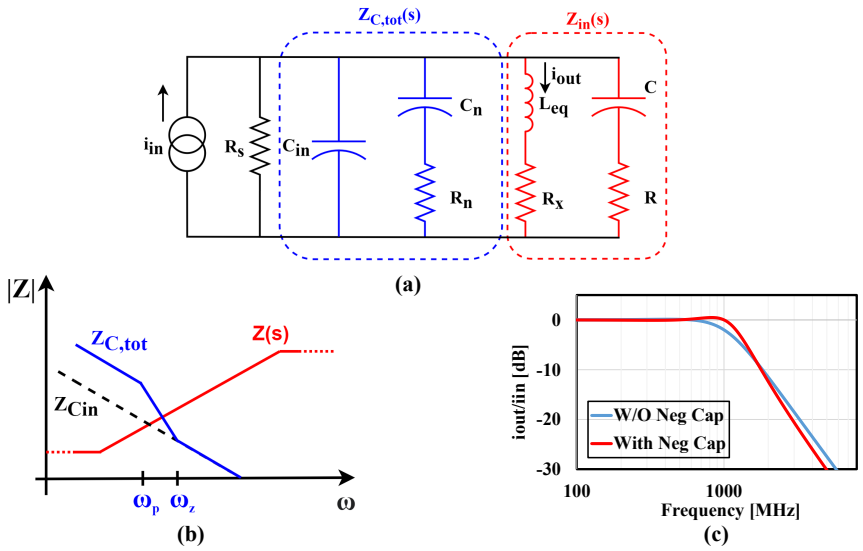


FIGURE 4.9: (a) equivalent model of the filter with negative capacitance. (b) corresponding impedance magnitude plots. (c) i_{out}/i_{in} frequency response.

A plot of the impedances is shown in Figure 4.9(b). From (4.15), at low frequency, where R_n can be neglected, the negative capacitance C_n partially cancels C_{in}. As frequency increases, $Z_{c,tot}$ has a pole at $\omega_p = \frac{C_{in}+C_n}{C_{in}C_nR_n}$ followed by a zero at $\omega_z = \frac{1}{C_nR_n}$. Placing the pole and zero close to ω_0 causes the equivalent capacitance shunting the input node of the filter to increase around ω_0. As a result, the poles Q and the out of band selectivity are increased. This behaviour is evident in Figure 4.9(c) where the transfer function i_{out}/i_{in} is shown with and without the negative capacitance.

4.1.5 Complete Filter Design

The complete filter topology is shown in Figure 4.10. A stacked NMOS-PMOS structure is used to double the transconductance and lower the noise for a given current. The bias current of the stacked NMOS-PMOS CG transistors ($M_{CG,x}$) is set controlling the current through the diode-connected transistors ($M_{D,x}$), which are one-fifth of the input transistors in size. A CMFB loop is used to set the DC voltage at the source of the four CG transistors ($M_{CG,x}$) around $V_{dd}/2$. Furthermore, all the capacitor (C_{in}, C and C_n) are implemented as arrays that can be digitally controlled to change the bandwidth of the filter. The output signal currents $i_{out,P}$ and $i_{out,N}$ at the top and bottom side of the 4 CG devices

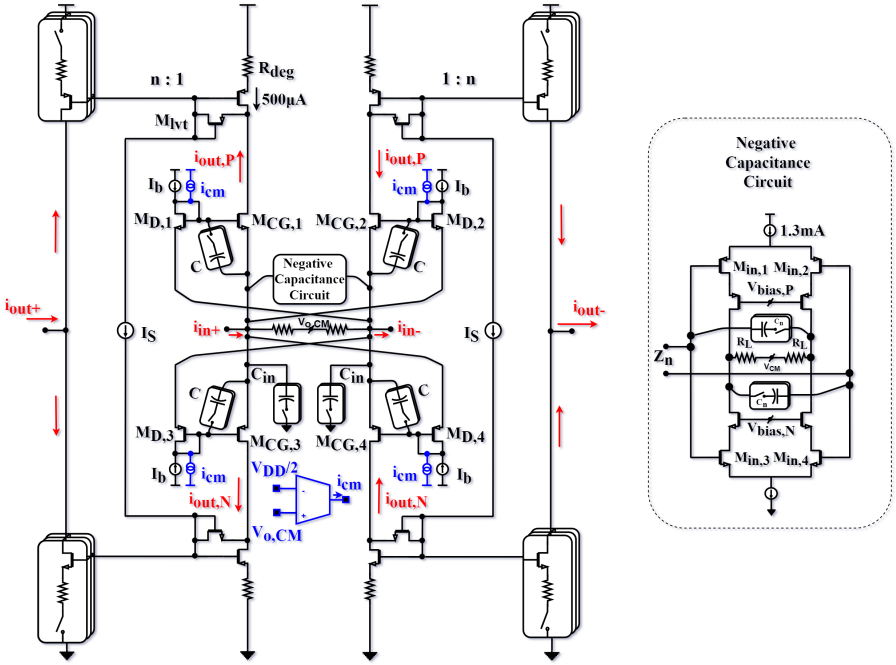


FIGURE 4.10: complete schematic of the open loop filter with negative capacitance circuit and bias currents.

Parameter	Value
V_{DD}	1.5 V
I_b	100 μA
I_S	20 μA
$g_{m,CG}$	10 mS
$g_{m,D}$	2 mS
C_{in} (max BW)	3 pF
C (max BW)	250 fF
R_{deg}	225 Ω

(A)

Parameter	Value
V_{DD}	1.5 V
$g_{m,in}$	12.5 mS
C_x (max BW)	865 fF
R_L	143 Ω

(B)

TABLE 4.1: Parameter values: (A) CG filter. (B) Negative capacitance circuit.

are recombined through two current mirrors whose gain is programmable from 5 to 1 so that in-band current gain is programmable from +14 dB down to 0 dB. Furthermore, in the diode-connected transistors of the current-mirror, a suitable DC voltage is created between gate and drain using a diode-connected

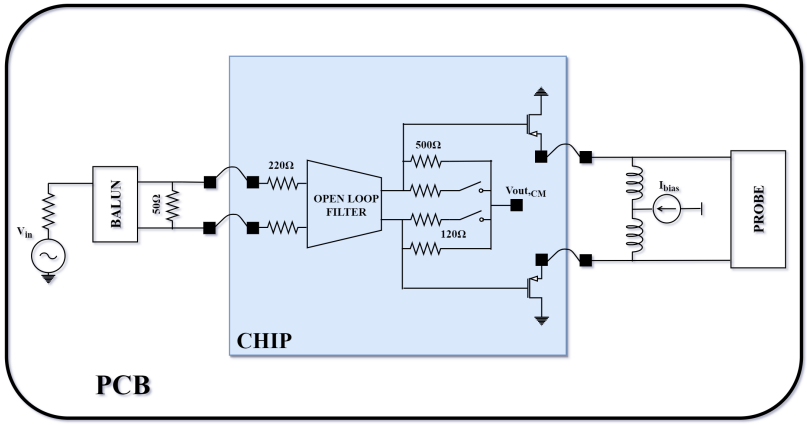


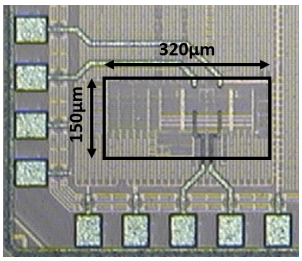
FIGURE 4.11: open loop filter test bench.

low threshold transistor (M_{lvt}) to improve signal compression. The mirrors use degeneration resistors (R_{deg}) to increase linearity and improve noise.

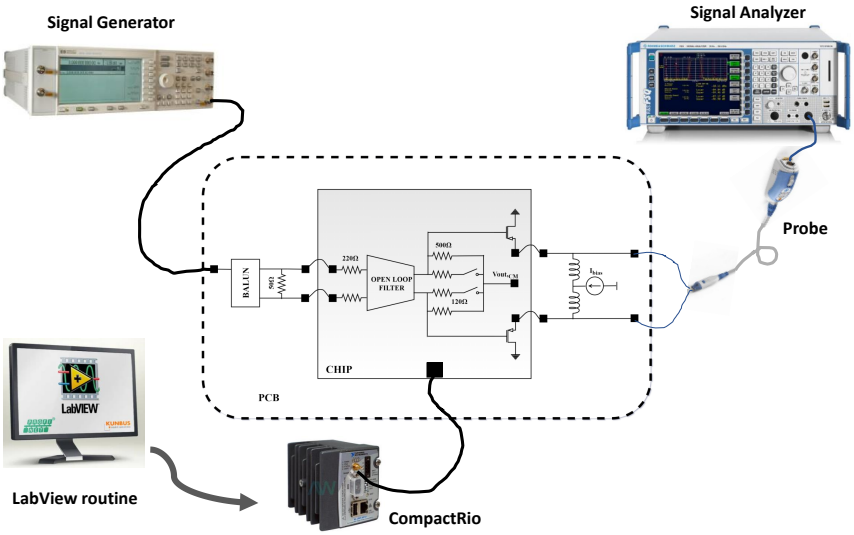
4.1.6 Measurement Results

The open loop filter has been tested as a stand-alone block. The test bench of the filter is shown in Figure 4.11. The recombined output currents from the current mirrors are sent to two load resistors that are also used to set the common mode bias voltage at the output. The load resistors can be switched from 100 Ω, when doing linearity measurement, to 500 Ω when doing noise measurement. The outputs are followed by two externally biased source followers implemented using PMOS transistors to buffer the loading from board traces and probes. The bare-die is wire-bonded on a PCB for measurements and the differential input signal is generated through a wideband on-board 1:1 balun. Input matching is realized on the board placing a 50 Ω resistor differentially after the balun.

The filter prototype is fabricated in tsmc 28nm HPC technology. The chip micro-photograph is shown in Figure 4.12a. It has an active area of 320μm × 150μm. The filter transfer function is measured using the configuration depicted in Figure 4.12b. A *NI cRIO-9014* is used to provide the biasing and



(a)



(b)

FIGURE 4.12: (a) microphotograph of the chip. (b) measurement setup for stand-alone open loop filter.

digital bits for gain and bandwidth variation using a software routine implemented in NI Labview. The input signal is provided by *HP ESG-4000A* signal generator, and the output signal is measured on *R&S FSQ8* signal analyzer using a wide bandwidth *R&S RT-ZD40* probe.

The filter transfer function with maximum current gain and bandwidth (i.e. 5x and 1 GHz respectively) is shown in Figure 4.13. The measurements are done up to 4 GHz due to the limitation of the probe bandwidth which has a bandwidth of 5 GHz. The measurements agree well with the simulations. The transfer function has an OOB roll-off close to 60 dB/dec in the frequency range up to 4 GHz, due to a pole associated with the current mirror and

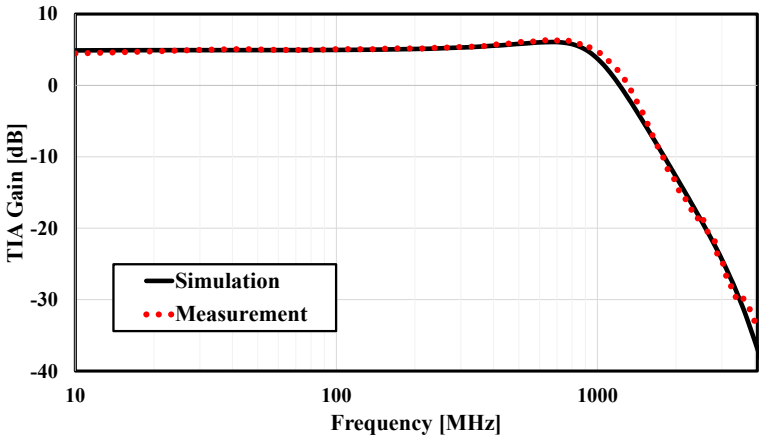


FIGURE 4.13: filter transfer function at maximum gain and bandwidth.

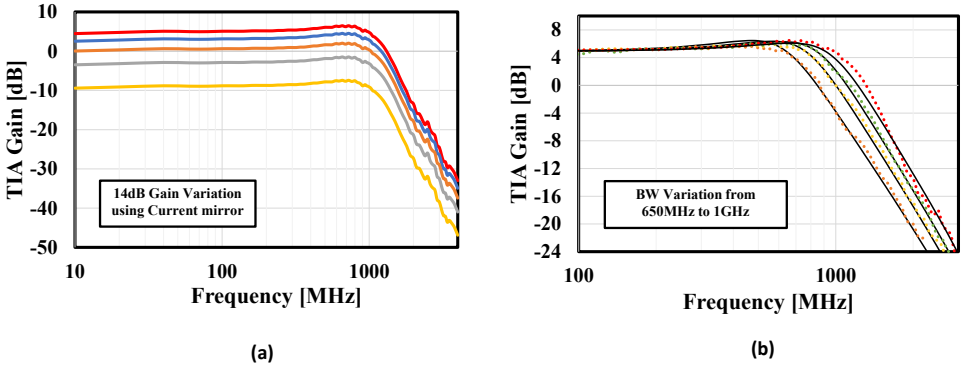


FIGURE 4.14: (a) filter transfer function with different gain settings. (b) filter transfer function with different bandwidths.

to the negative capacitance. Figure 4.14(a) shows the filter transfer function while changing the gain of the current mirror. The gain variability of 14 dB

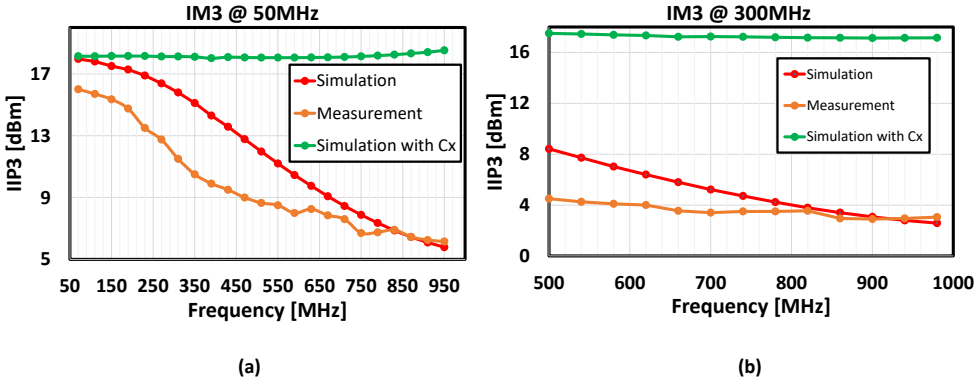


FIGURE 4.15: IIP3 measurements with two tones spanning the bandwidth of the filter.

is implemented in 4 steps. The filter power dissipation scales from 11 mW at maximum gain to 5 mW at minimum gain. Figure 4.14(b) shows the filter bandwidth variation. In this solution, the bandwidth is varied from 1 GHz down to 650 MHz using digitally controlled capacitive arrays. Linearity test is reported in Figure 4.15. IIP3 is measured with two tones spanning the the bandwidth of the filter while keeping the frequency of the IM3 tone at 50 MHz in Figure 4.15(a) and at 300 MHz in Figure 4.15(b). It can be noticed that the IIP3 drops as the tone frequencies increase. Simulations demonstrate that the circuit's non-linearity is restricted by the high impedance found at the current mirror's input and predicts a behaviour of the IIP3 with frequency that qualitatively approaches the measured one, as shown in Figure 4.15. From Figure 4.16, the input impedance of the current mirror without C_x is given as:

$$Z_x(s) = \frac{1 + g_{m,cm} R_{deg}}{g_{m,cm}} \frac{\left(1 + \frac{sC_p}{g_{m,lvt}}\right)}{\left(1 + \frac{sC_p}{g_{m,cm}}\right)} \tag{4.16}$$

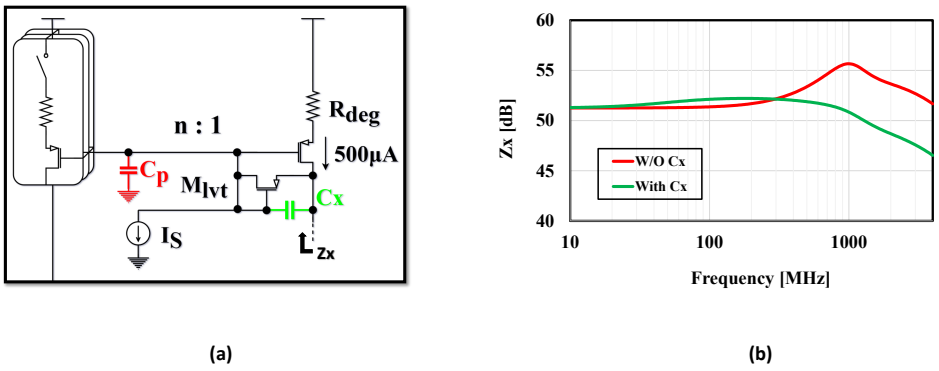


FIGURE 4.16: (a) C_x in shunt with M_{lvt} in the open loop filter current mirror. (b) input impedance of the current mirror.

However if a capacitor C_x is put in shunt with M_{lvt} as shown in Figure 4.16 and make sure that $C_x >> C_p$, (4.16) becomes

$$Z_x(s) = \frac{1 + g_{m,cm}R_{deg}}{g_{m,cm}} \frac{1}{\left(1 + \frac{sC_p}{g_{m,cm}}\right)} \tag{4.17}$$

It can be noticed from (4.17), C_x cancels the in-band zero and conseguently the impedance seen at the input decreases sufficiently near the band edge as shown in Figure 4.16(b). Simulations are performed with value of $C_x = 800fF$ and it results in the IIP3 of +18dBm throughout the bandwidth of the filter as shown in Figure 4.15. Moreover, the capacitor C_x also filters out the noise of the M_{lvt} improving the overall noise of the circuit. Such a shunt capacitor however, extends the bandwidth of the mirror thereby reducing the selectivity of the filter beyond 2.5 GHz (by about 2 dB at 4 GHz). The input noise integrated within the maximum filter bandwidth of 1 GHz is 169 μV_{rms}.
Table 4.3 summarizes the experimental results and compares the performance to the state-of-the-art CMOS filters in the GHz range. The proposed filter is based on a regulated cascode architecture instead of a Gm-C architecture. The filter has an outstanding +16dBm of IIP3 shows that this architecture is potentially very linear compare to Gm-C one if the impedance at the drain of the CG is sufficiently low. This filter and [46] are the only two that offer gain

	This Work 2021 [47]	ESSCIRC 2014 [48]	ISSCC 2012 [49]	ESSCIRC 2010 [50]	TCAS-I 2009 [46]
Technology	28nm CMOS	28nm LP CMOS	65nm CMOS	40nm CMOS	65nm CMOS
$P_{diss.}$[mW]	5/11	5/30	19/140	21	36
Supply[V]	1.5	1.1	1.0/1.4	1.1	1.2
Topology	Regulated cascode	Gm-C	Gm-C	Sallen-key biquad	Gm-C
Type	Butterworth	Chebyshev	Chebyshev	Butterworth	Chebyshev
In-band gain [dB]	-9/5	0	1.3	0	9/43
f_c[MHz]	650-1000	200-3000	4700/10000	1760	240
order	2^{nd}	5^{th}	3^{rd}	5^{th}	5^{th}
IIP3[dBm]	+16	+2	+7	-8	-2.5
Input N_0[$nV_{rms}/\sqrt{Hz}$]	5.34	7.3	5.02	6	7.8
FoM_{conv}[dBJ^{-1}]	164.8	155.4	153.2	148.6	147.3
FoM_{IM3}[dBJ^{-1}](with C_x)	152 (162.5)	n.a.	153.1	n.a.	130.5

TABLE 4.3: Filter performance summary and comparison with State-of-the-Art.

programmability, which is a desired feature in a receiver's baseband. To make a comparison a conventional Figure of Merit (FoM_{conv}) is used that includes all essential specifications and is defined as: $FoM_{conv} = IMFDR3{+}10log(N\frac{BW}{P_{diss}})$ where N is the order of the filter, BW the bandwidth in Hz, P_{diss} the power dissipation in Watts and $IMFDR3$ the intermodulation-free dynamic range defined as $(2/3)(IIP3[dBm] - V_n[dBm])$, with V_n being the integrated input-referred noise. By considering the IIP3 at lower frequency, this design has a FoM_{conv} that exceeds all previous designs. For fair comparison another FoM is presented that considers the distance of the IM3 tone from the band edge. $FoM_{IM3} = FoM_{conv} + 10log(\frac{f_{IM3}}{f_c})$. Even though FoM_{IM3} drops because of the 16 dB drop in IIP3 going from low frequency to band edge, it is still comparable to the best design. However, as stated earlier by using C_x, FoM_{IM3} improves to 162.5.

4.1.7 Improved Filter design

The open-filter design is improved to meet the specifications of the receiver. Figure 4.17 shows the filter schematic with the modifications. As previously stated, capacitor C_x is used in shunt with M_{lvt} to increase the filter's linearity at higher frequencies. However, it increaes the current mirror bandwidth, which reduces the filter's OOB selectivity. To fulfill the receiver's OOB selectivity requirement of 33 dB, a novel negative capacitance circuit is utilized, which will be explained in detail in the following subsection. Furthermore, with the new

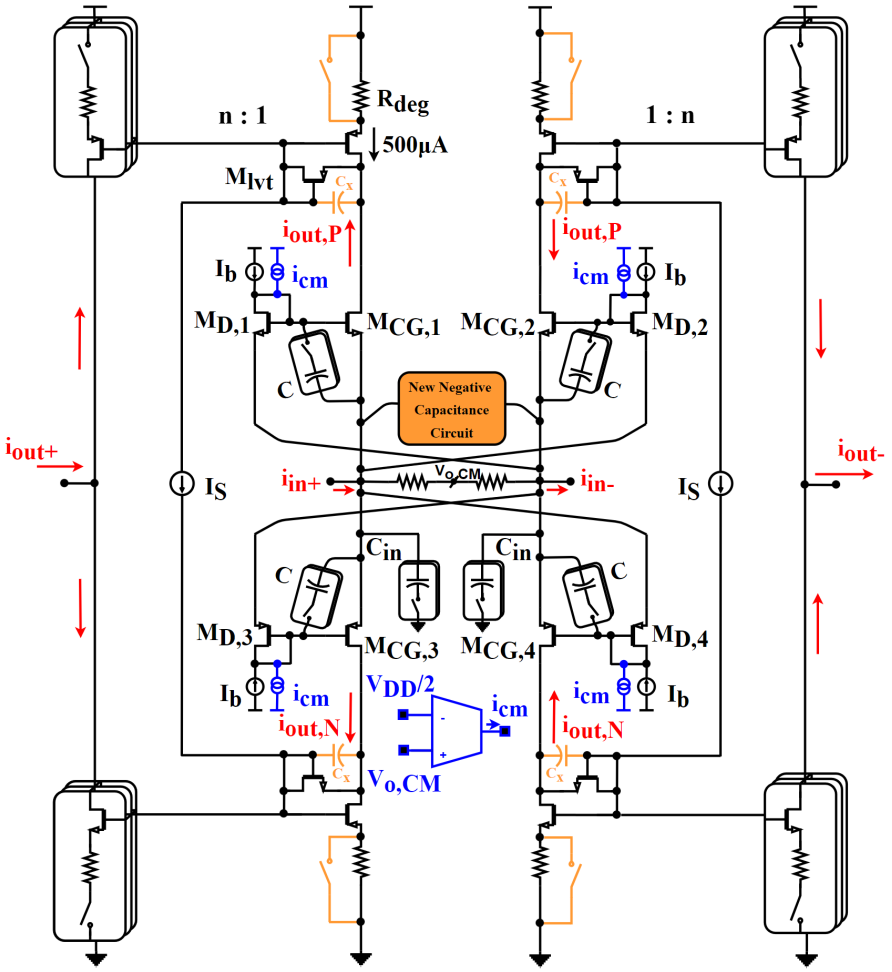


FIGURE 4.17: improved open loop filter.

design, there is the option of short- circuiting the current mirror's degeneration resistors, which significantly improves linearity at the minimum baseband gain. However, it increases the noise from the current mirror but since at the minimum baseband gain , there is enough margin in terms of noise requirement it does not effect the overall receiver performance. To put it another way, a better trade-off between noise and linearity is implemented.

4.1.8 New Negative Capacitance Circuit

To improve the open loop filter Q and OOB selectivity a novel negative capacitance circuit is presented in Figure 4.18. In contrast to the earlier negative capacitance circuit (see Figure 4.10), which provided negative resistance OOB, this circuit gives negative capacitance in the filter band and positive capacitance outside of the band, enhancing the filter's selectivity. Two cross-coupled transistors are connected at the source of the input transistors, as illustrated in the Figure 4.18 (a), to create a negative differential resistance of value $-2/g_{m2}$. An explicit gate to source capacitor C_{gs} is connected at the input. The single-ended input impedance of the circuit, denoted by $Z_{n,Cgs}(s)$, can be calculated as:

$$Z_{n,Cgs}(s) = \frac{1}{sC_{gs}(1-A)} \frac{\left(1+\frac{s(C_{gs}+2C_f)}{g_{m1}-g_{m2}}\right)}{\left(1-\frac{s2C_f}{g_{m2}}\right)} \tag{4.18}$$

where $A = \frac{g_{m1}}{g_{m1}-g_{m2}}$, is a dc gain from gate to source. The frequency behaviour of $Z_{n,Cgs}(s)$ is shown in Figure 4.18 (b). From (4.18), at lower frequencies, if g_{m1} is greater than g_{m2}, the gain from gate to source, A, becomes greater than 1, resulting in an equivalent in-band negative capacitance of value $C_{gs}\left(\frac{g_{m1}}{g_{m1}-g_{m2}}\right)$. At higher frequencies capacitance C_{gs} shunting the v_{gs} of input

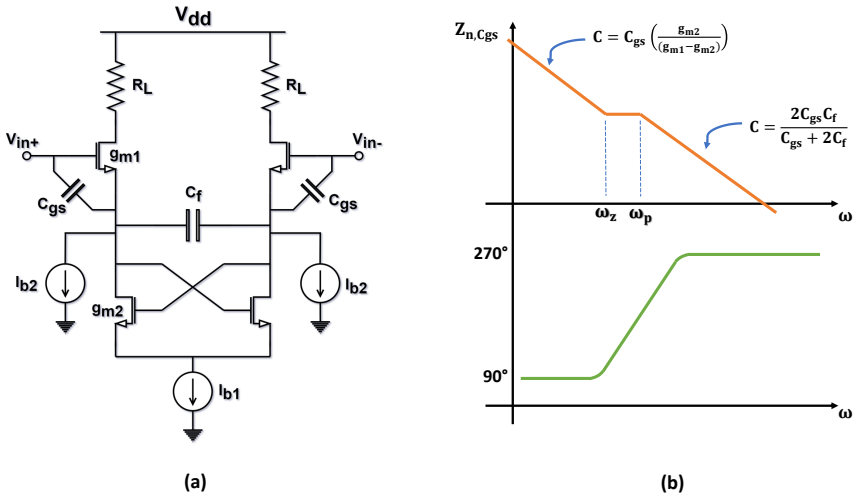


FIGURE 4.18: (a) negative capacitance circuit using gate to source capacitance, C_{gs}. (b) frequency behaviour of the input impedance, $Z_{n,C_{gs}}$.

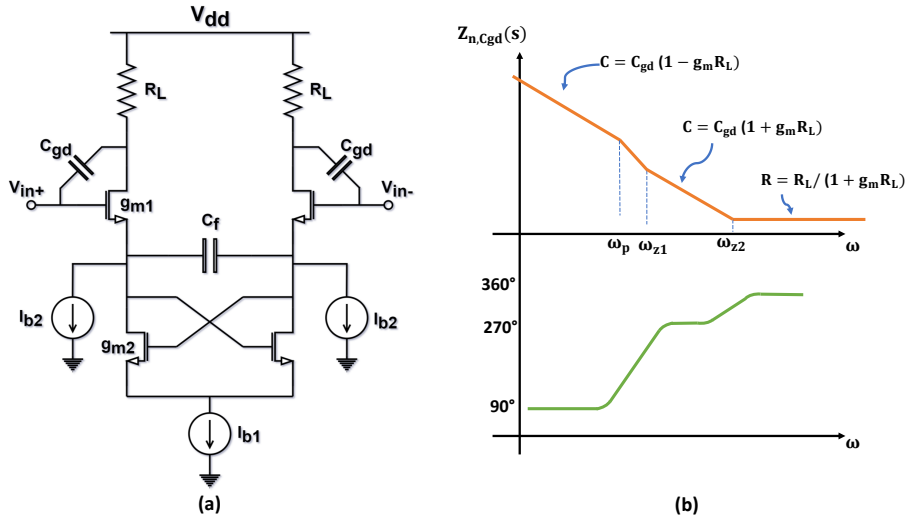


FIGURE 4.19: (a) negative capacitance circuit using gate to drain capacitance, C_{gd}. (b) frequency behaviour of the input impedance, $Z_{n,C_{gd}}$.

transistor which gives a zero at $\omega_z = -\frac{(g_{m1}-g_{m2})}{C_{gs}+2C_f}$ and then capacitor C_f and negative resistance $1/g_{m2}$ gives a RHP pole at $\omega_p = \frac{g_{m2}}{2C_f}$. Together they provide a 180° phase shift which transforms the negative capacitance to a positive capacitance of value $\frac{2C_{in}C_f}{C_{in}+C_f}$, given by the series of C_{gs} and $2C_f$.

Similarly, if the same circuit is considered with explicit capacitor from gate to drain, C_{gd}, as shown in Figure 4.19(a). The equivalent single-ended input impedance of the circuit in this case can be written as:

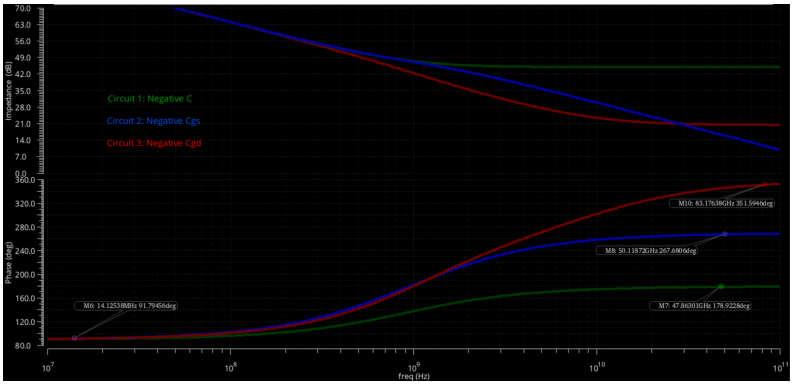
$$Z_{n,Cgd}(s) = \frac{1}{\left(1 - \frac{g_{m1}g_{m2}R_L}{g_{m1}-g_{m2}}\right) sC_{gd}} \frac{\left(1 + \frac{s2C_f}{(g_{m1}-g_{m2})}\right)(1 + sR_LC_{gd})}{\left(1 + \frac{s2C_f}{(g_{m1}-g_{m2})}\frac{(1+g_{m1}R_L)}{(1-g_{m1}R_L)}\right)} \tag{4.19}$$

If it is assumed that $g_{m1} = 2g_{m2} = g_m$, (4.19) can be simplified as

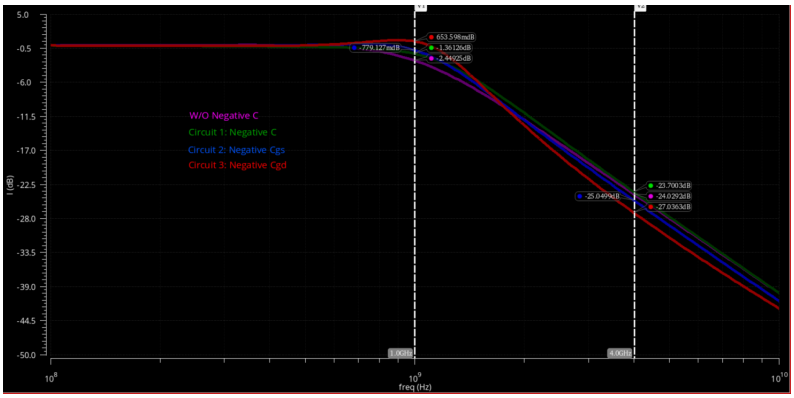
$$Z_{n,Cgd}(s) = \frac{1}{(1 - g_mR_L)sC_{gd}} \frac{\left(1 + \frac{s4C_f}{g_m}\right)(1 + sR_LC_{gd})}{\left(1 + \frac{s4C_f}{g_m}\frac{(1+g_mR_L)}{(1-g_mR_L)}\right)} \tag{4.20}$$

The qualitative frequency behaviour of $Z_{n,Cgd}(s)$ is shown in Figure 4.19(b) . If circuit gain from gate to drain, i.e. g_mR_L is greater than 1, at lower frequencies, it gives a negative in-band capacitance of value $C_{gd}(1-g_mR_L)$. It features

one LHP zero and one RHP pole at higher frequencies, providing a 180° phase shift. From (4.20), it can be noticed that in this case, the pole comes before zero, which can be translated into a higher value of positive capacitor after the phase shift and conseguently higher OOB selectivity in the filter. The positive capacitor value in this case is $C_{gd}(1 + g_m R_L)$. This circuit adds an extra zero at $\omega_z = 1/R_L C_{gd}$ which turns the circuit impedance into resistive at higher frequencies. However, by lowering the value of R_L the zero can be pushed out



(a)



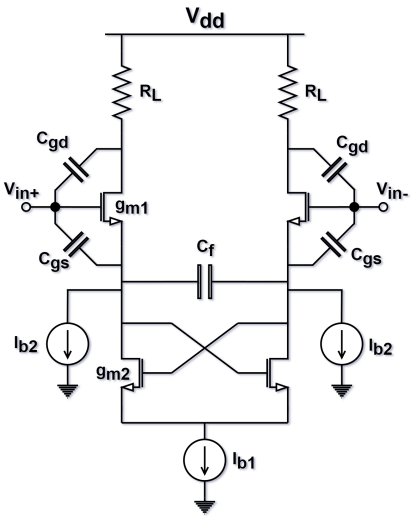
(b)

FIGURE 4.20: (a) input impedance of three different negative capacitance circuit. (b) open loop filter transfer function using different negative capacitance circuits.

of the band of interest.

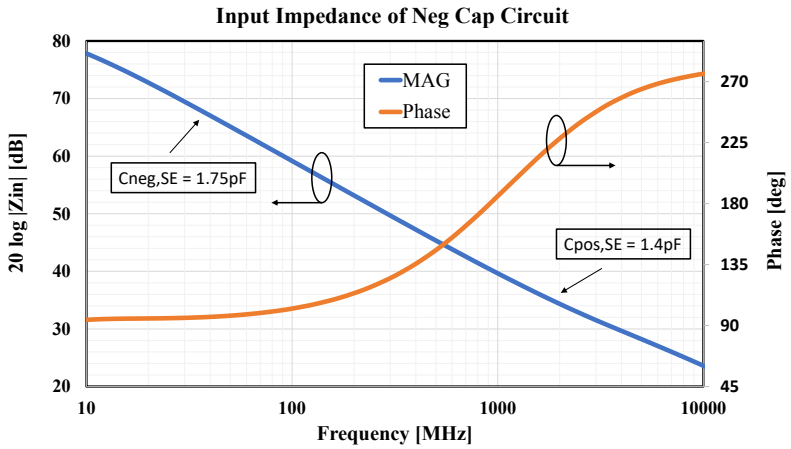
A negative capacitance of 1 pF is implemented for analysis purposes using three different circuits shown in Figure 4.10, 4.18 and 4.19. The input impedance of the three circuits is shown in Figure 4.20a. In all three cases, impedance has a phase shift around 900 MHz. For the case of circuit 1 (see Figure 4.10) the impedance has a phase shift of +90°, causing the negative capacitor of 1 pF to be converted to a negative resistance of -177 Ω. In the case of circuit 2 (Figure 4.18), the impedance has a phase shift of +180°, converting the negative capacitance to +333 fF of positive capacitance. Similarly, impedance has a phase shift of +180° in circuit 3 (Figure 4.19), but it converts into positive capacitance of +1.5 pF in this case. In this example, the zero is pushed to 10 GHz, at which point the impedance eventually becomes resistive (+10 Ω). The open loop filter transfer function for different negative capacitance circuits connected at the input is shown in Figure 4.20b. In comparison to the previous negative capacitance circuit, the new negative capacitance circuit using C_{gd} enhances the filter's OOB selectivity by more than 5 dB.

Eventually, the implemented negative capacitance circuit is a combination of negative C_{gs} and negative C_{gd}, as shown in the Figure 4.21a together with parameter values employed in the circuit. As can be noticed from (4.18) and (4.19) that to achieve negative capacitance at the input both for C_{gs} and C_{gd} it requires to have g_{m1} greater than g_{m2}. To achieve higher $g_{m,1}$ with respect to $g_{m,2}$, the size of the input transistors are doubled as compared to the cross-coupled transistors. Two additional current sources $i_{b,2}$ are connected at the source such that the bias current passes through cross-coupled transistors is lower with respect to the input transistors. The ratio of g_{m2} over g_{m1} in this circuit is set at 0.6. Because of the input transistor's body effect, the effective gain from gate to source is 2, resulting in a negative C_{gs} at the input of -630 fF. Similarly, the gain from gate to drain is +2.7, resulting in a negative C_{gd} at the input of -1.12 pF. As illustrated in Figure 4.21b, the effective single-ended negative capacitance at the input is the sum of the negative C_{gs} and C_{gd} and has a value of -1.75 pF. The implemented positive capacitance after the phase shift is 1.4 pF, with 244 fF attributable to C_{gs} and the remaining capacitance due to C_{gd}.



Parameter	Value
I_{b1}	2.5 mA
I_{b2}	0.5 mA
C_{gd}	630 fF
C_{gs}	630 fF
C_f	400 fF
R_L	60 Ω
g_{m1}	35 mS
g_{m2}	21 mS

(a)



(b)

FIGURE 4.21: (a) implemented negative capacitance circuit with combination of C_{gs} and C_{gd} and parameter values used in the circuit. (b) input impedance of the circuit.

4.1.9 Wideband Output TIA

As previously stated, the HF BB path need to cover bandwidth of up to 1 GHz. Conseguently, the closed-loop bandwidth of the TIA following the open-loop filter should be 1 GHz. The TIA is built around an OTA closed in feedback with a parallel RC network. The OTA is designed to deliver high loop gain and stability over a wide bandwidth. Linearity is ensured over a wider frequency range in this way. The block diagram of the OTA is shown in Figure 4.22.

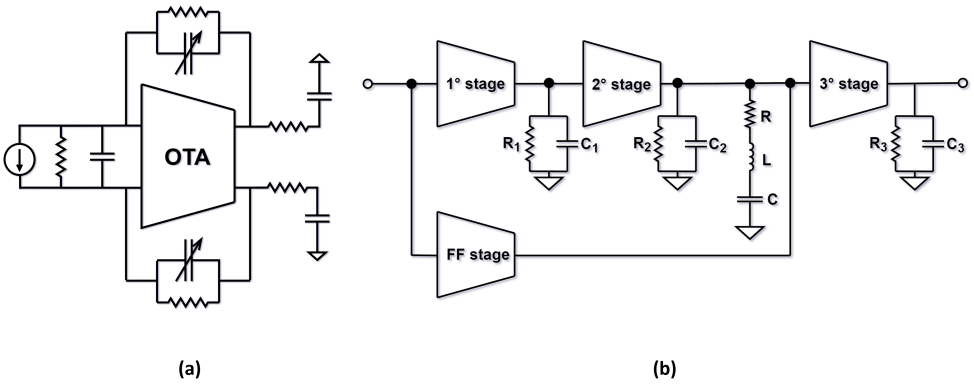


FIGURE 4.22: (a) TIA block diagram. (b) equivalent single-ended representation of the proposed OTA.

The OTA is implemented with three cascaded Gm-stages and a feed-forward stage. The feed-forward topology is capable of achieving both high loop-gain and wide bandwidth. The feed-forward stage creates a left-half plane zero (LHP) in the overall OTA transfer function, compensating for the negative phase shift of the main path's poles and enhancing its phase margin. If the main path contains three stages in a normal FF architecture, two nested FF stages are required, each introducing a zero. However, this would result in a very significant power dissipation, particularly in the external path. In this design, only one FF path is used and a peaking inductor is used to introduce a second zero. The more details about the design can be found in [51].

The circuit schematic of each OTA stage is shown in Figure 4.23. The input stage is a class A complementary p-n structure with high gm. To boost transistor efficiency, the input transistors (M_1^1, M_4^4) operate in sub-threshold mode. To obtain high DC gain, the input differential pairs are cascoded. As a second stage, a class AB low gain wideband amplifier is used. Class AB behaviour enables for the processing of a large input signal without slewing, which would

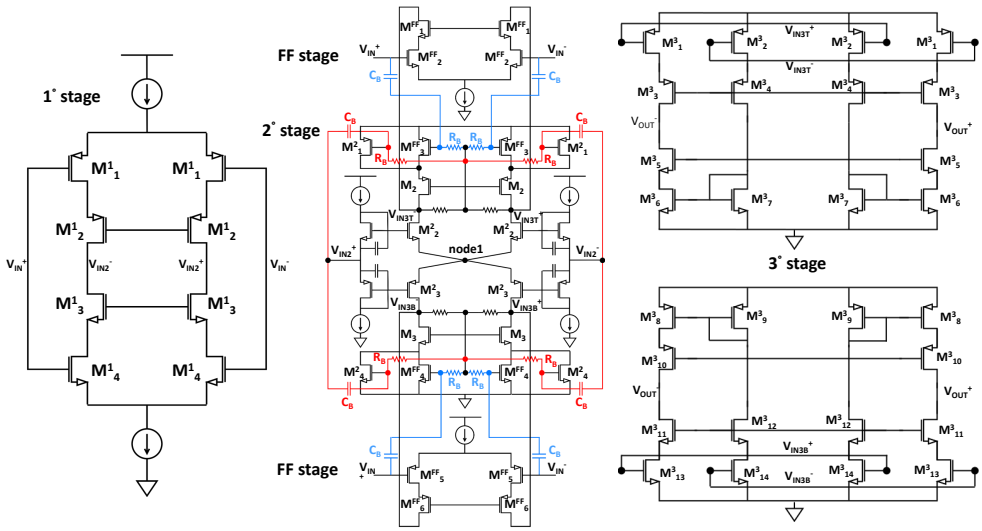


FIGURE 4.23: complete schematic of the OTA (biasing and CMFB circuits are not included).

result in high distortion and early compression. Regarding the second stage, node 1 can be considered as ground for purely differential signal, which results in its small signal voltage gain as

$$A_v = (g_{m2} + g_{m3})(r_{out1}||r_{out2}) \tag{4.21}$$

where g_{m2} and g_{m3} are the tranconductance gain of transistors M_2^2 and M_3^2 respectively and r_{out1} and r_{out2} are the output node impedences. Furthermore, a large boosting capacitor (C_B) from the input node to the gate of the load transistors (M_1^2, M_4^2), which becomes a short at higher frequencies, is used to boost the g_m by approximately a factor of two, as shown in the Figure 4.23 in red. This adds a zero-pole doublet separated by an octave, extending the UGBW and improving the phase margin. The second stage, as illustrated in Figure 4.23, has two pairs of differential outputs, one at the drains of the p-mos load transistors and the other at the drains of the n-mos load transistors. Due to supply constrains, two parallel FF stages are implemented: one with n-mos input transistors (M_2^{FF}) and the other with p-mos input transistors (M_5^{FF}). The loads from the second stage and FF stages are combined and drive the complementary p-n push pull output stage.

The impact of inductive peaking can be seen from the transfer function of the FF stage shown in Figure 4.24. The second/FF stages have a pole at 5

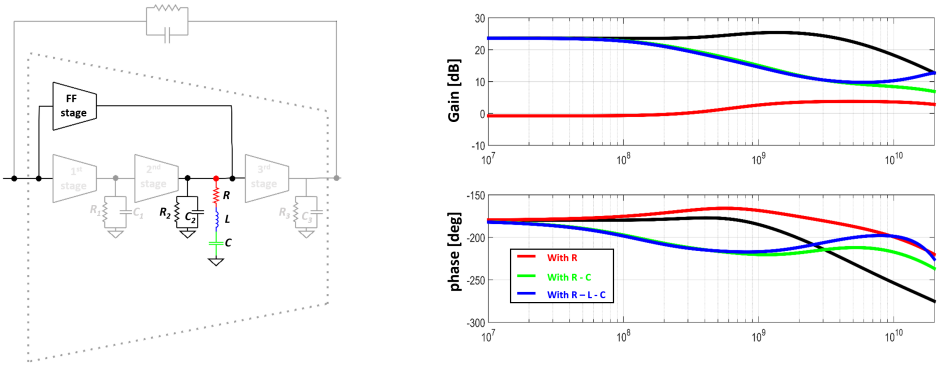


FIGURE 4.24: transfer function of the FF stage.

GHz, resulting in a 64° negative phase shift at unity gain frequency (7.5 GHz). To address this issue, a resistance can be used as the load of the second/FF stage, at the expense of lowering the total DC gain. A capacitor is connected in series with the resistor to maintain the gain up to the filter band edge (e.g., 1.5 GHz). An inductor is connected in series with the resistor to increase the UGBW while simultaneously increasing the phase margin. For an inductor of 1.2 nH and a resistor of 110 Ω, the R-L combination introduces a zero around 14 GHz which improves the phase margin by 20° and increase the UGBW by 1 GHz. It can be demonstrated that having the same phase margin without the inductor would result in a UGBW reduction of more than 40%. To get the same performance without the inductor, multiple FF stages must be used or the FF stage transconductance must be increased. Both scenarios result in a higher power dissipation.

A class AB amplifier is used in the last stage (third stage) to optimize the output driving capabilities. Two parallel output stages with nmos and pmos input transistors are implemented to directly interface with the second/FF stages's two outputs. The wide swing pseudo-differential topology with extremely low common mode gain is one of the main reasons to adopt an n only (p only) output stage. This is necessary to stabilize the FF stage's common mode response, which has a positive common mode feedback. Finally, the quiescent current of the class AB stage can be accurately regulated using a current mirror. Common mode feedback circuits are still required, but only to adjust for current mirror mismatches between p-MOS and n-MOS.

The OTA is employed in the closed loop TIA. The feedback impedance is made up of a 530 Ω resistor connected in parallel with a tunable capacitor that is used to program the TIA bandwidth. At UGBW, the phase shift produced by

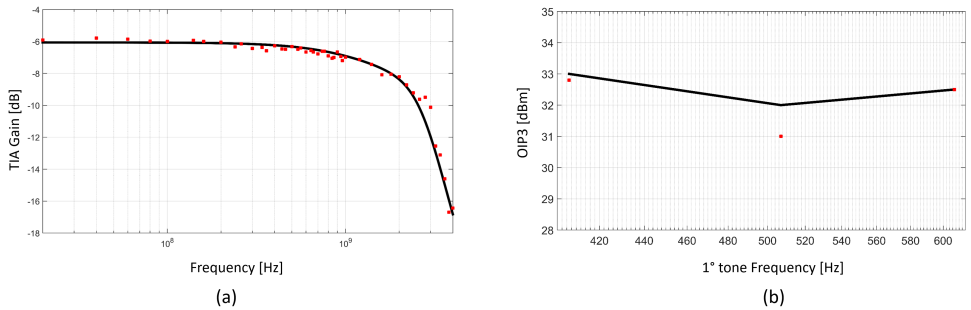


FIGURE 4.25: (a) TIA transfer function. (b) OIP3 vs Ist-tone.

the feedback is negligible (e.g., 2° for 1.5 GHz BW setting).

4.1.9.1 Measurement results

The TIA is fabricated in TSMC 28nm HPC technology and is tested as a standalone block. Figure 4.25(a) depicts the TIA transfer function for the maximum bandwidth. In-band nominal gain of the TIA is -6 dB. The power dissipation of the OTA is 17 mW. To test the linearity, two tones are swept in frequency such that the intermodulation tone, IM3, falls at 314 MHz. The OIP3 vs frequency

	This Work	ISSCC 2003 [52]	ASSCC 2007 [53]	ISSCC 2015 [54]
Technology	28nm CMOS	180nm CMOS	180nm CMOS	28nm FD-SOI
Area [mm^2]	0.06	N/A	1	0.04
Supply[V]	1.5	1.8	1.5	1
$P_{diss.}$[mW]	17	90	175	5.6
BW_{3dB}[MHz]	500-1500	500	1000	459
order	1st	5th	4th	3rd
OP_{1dB}[dBm]	10	N/A	N/A	4.9
Inband OIP3[dBm]	32.9	26.5	17.5	12.1
$V_n[\mu V_{rms}]$	300	402	N/A	120
Inband IMFDR3 [dB]	60.2	55	N/A	53.5
FoM [dBJ^{-1}]	169.7	159.4	N/A	165.7

TABLE 4.4: TIA performance comparison with State-of-the-art.

of the first interferer, together with the simulations, are presented in Figure 4.25(b). The OIP3 is mostly unaffected by the location of the intermodulation tones inside the band of interest, ranges from 32.9 to 31 dBm. The integrated output noise, V_n, up to 1.5 GHz, is 300 μV_{rms}. The corresponding maximum IMFDR3 is 60.2 dB. A tone at 1 GHz is used to test the signal compression, yielding a 10 dBm output referred 1dB compression point. Table 4.4 shows the TIA's overall performance and a comparison to the state-of-the-art. The Figure of Merit, FoM, defined as $FoM = IMFDR3[dB] + 10log\left(\frac{orderBW}{Power}\right)$ is used for comparison. Even with 3 times larger bandwidth, the filter FoM is 10 dB better than [52] and 4 dB better than [54]. The filter area is 1.5 times larger compare to [54], even though the provided filter is first order and the one in [54] is third order. However, since the inductors dominate the filter area, when the UGBW increases, the inductors area reduces substantially.

4.1.10 Complex Feedback in HF BB path

In HF baseband path, complex feedback is employed across the TIA to address upper and lower band mismatches after the downconversion which are due to the parasitic capacitor at the output of the 2° LNTA. In [55], a similar feedback approach is used to provide a complex impedance at the input for matching

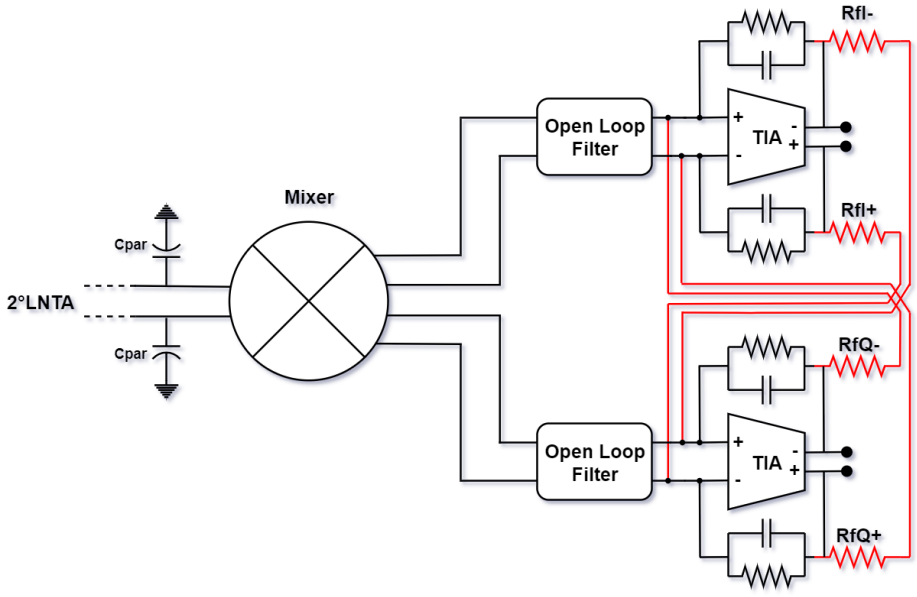


FIGURE 4.26: complex feedback in HF BB path.

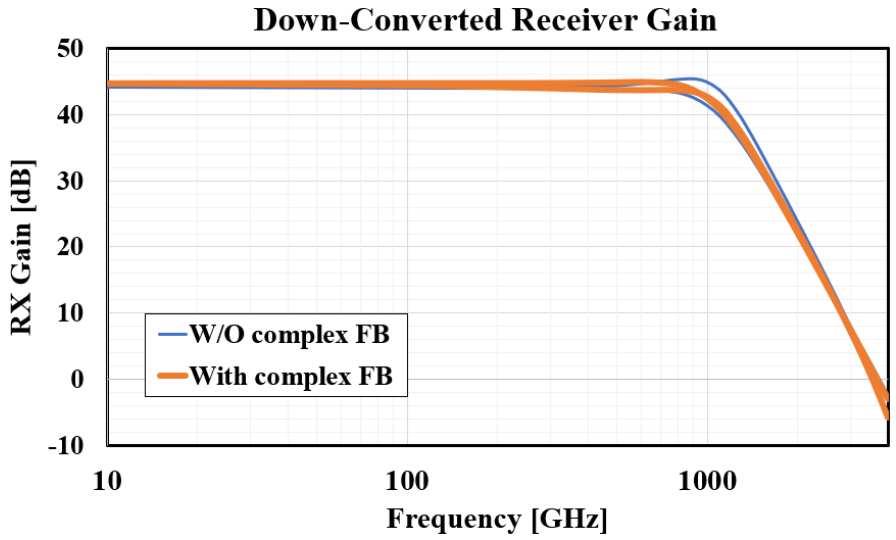


FIGURE 4.27: down-converted receiver gain with and without complex feedback across TIA.

reasons in a mixer first receiver. Figure 4.26 depicts the HF baseband path with complex feedback. The idea is to connect the feedback resistors, $R_{f,x}$, from the output of the I-channel of the amplifier to the input of the Q-channel and vice-versa. These additional feedback paths present a 90° phase-shifted version of the original signals back to the amplifier inputs scaled by $R_{f,x}$. The phase of V_oI+ in the lower band corresponds to the phase of V_oQ- in the upper band, and the phase of V_oI- in the lower band corresponds to the phase of V_oQ+ in the upper band. The complex feedback across TIA can be used to adjust the mismatch between upper and lower band by selecting appropriate value of $R_{f,x}$. The feedback resistor $R_{f,x}$ is implemented as an array with a value range from 1 kΩ to 3.5 kΩ. In order to achieve the same equivalent phase shift, the polarity of the feedback resistors must be switched from the Q-channel to the I-channel due to the relative phases of sine and cosine. The effect of the feedback can be observed in Figure 4.27, which shows the receiver's down-converted transfer function with and without the complex feedback. Around 1 GHz, the mismatch between upper and lower band is more than 3 dB without complex feedback, but with complex feedback, the mismatch is less than 0.5 dB.

4.2 Low Frequency Baseband Path

The Low Frequency Baseband (LF BB) path design is presented here for the purpose of complete receiver architecture design. This section is taken from [56]. The LF BB path is composed of a second-order Rauch filter followed by a first-order TIA, as shown in Figure 4.28. Rauch filter has four stages in the main path and a parallel feed-forward branch (FF) to guarantee stability in the high frequency range. Similarly, TIA has three stages in the main path and a FF path. The gain variability is implemented in the TIA by using variable resistors, R_{var}, and bandwidth is controlled by changing the resistors and capacitors values to cover RF channel bandwidths in four modes: 50 MHz, 100 MHz, 200 MHz and 400 MHz.

As two separate loops are functioning together in both Rauch and TIA, the main challenge is to maintain the stability of the whole chain. To consider the loop stability, each loop is broken into two different loops, as shown in Figure 4.29(a). The main path is dominant in the low-frequency range, whereas the other loop, which passes via the feed-forward circuit, is dominant at higher frequencies. The loop gain of the main path, feed-forward path and the overall loop gain of the Rauch filter are shown in Figure 4.29(b). As can be seen from the Figure 4.29(b), the main path dominates the loop gain at low frequencies, while the FF path controls the G-loop response at higher frequencies around

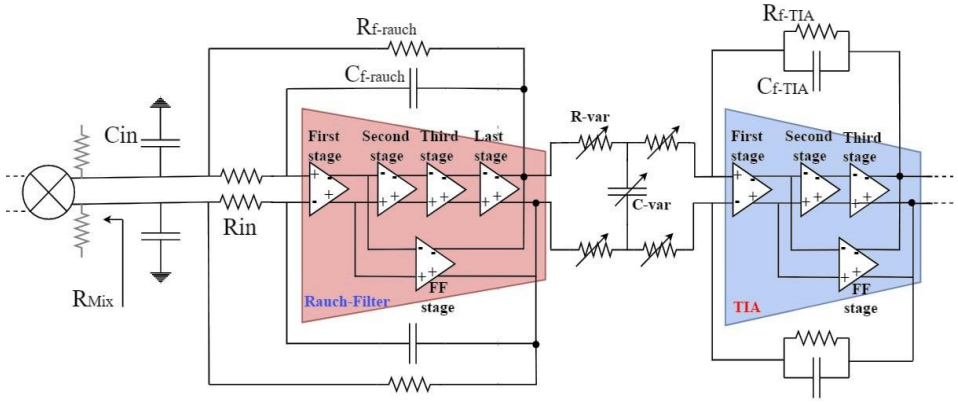


FIGURE 4.28: LF BB path: 2nd-order Rauch filter followed by Ist-order TIA.

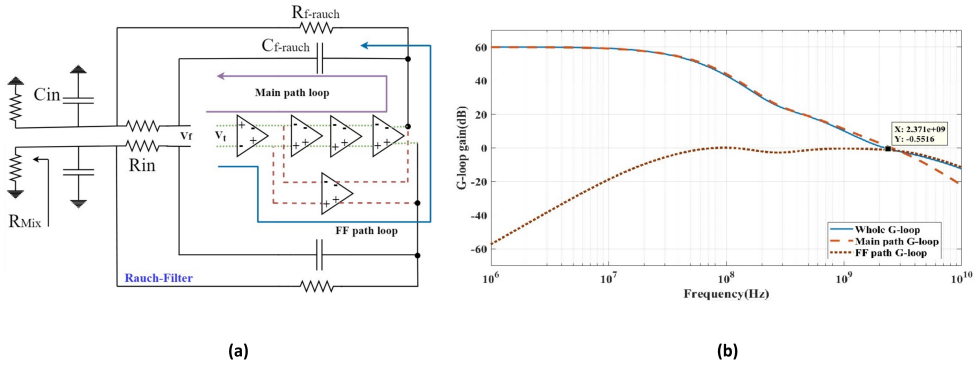


FIGURE 4.29: (a) Rauch filter G-loop. (b) loop gain of main path and FF path.

Parameter	Value
R_{in}	90 Ω
C_{in}	8.5 pF
$R_{f\text{-}rauch}$	2 kΩ
$C_{f\text{-}rauch}$	250 fF
R_{var}	250 Ω
C_{var}	1.5 pF
R_{TIA}	1 kΩ
C_{TIA}	600 fF

TABLE 4.5: Rauch filter and TIA resistors and capactiors values.

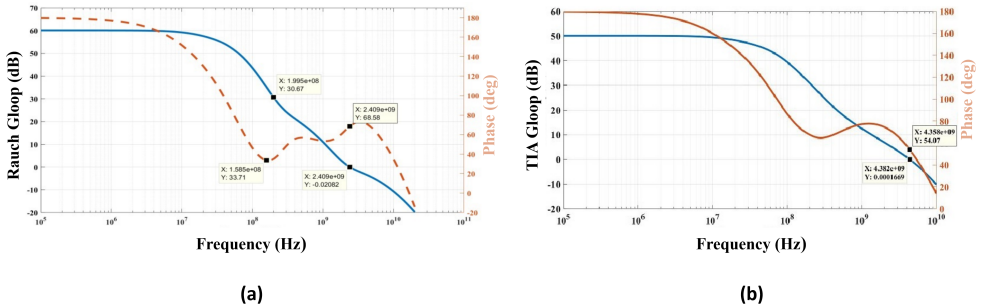


FIGURE 4.30: (a) Rauch filter G-loop. (b) TIA G-Loop.

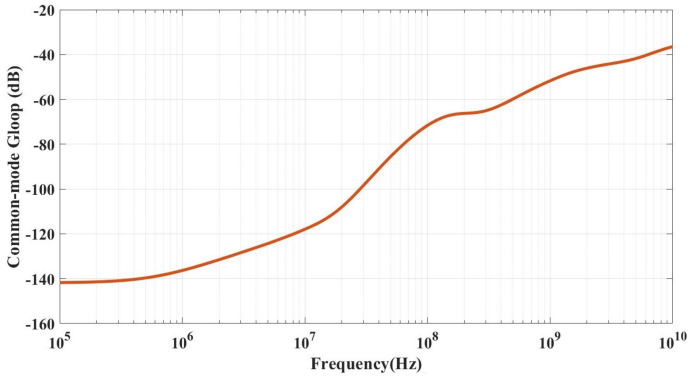


FIGURE 4.31: common-mode Gloop response of Rauch filter.

unity gain bandwidth. The FF path maintains the stability of the system by adding a zero in the transfer function. Figure 4.30(a) and 4.30(b) show the whole G-loop responses for Rauch and TIA filter respectively based on the filter's design parameter value shown in Table 4.5. The UGBW and phase margin for Rauch and TIA are 2.4 GHz, 68°, and 4.3 GHz, 54° respectively.
In addition to differential loops, the common mode stability is also the concern especially in Rauch filter main path as it consists of four stages and gives a positive common mode loop gain. So, to maintain the common mode stability, the common mode gain is kept well below 0 dB so that even with positive feedback the circuit remain stable. Figure 4.31 shows the common-mode G-loop gain which is around -40 dB at 10 GHz.

4.2.1 Rauch filter and TIA Circuit Design

The first stage of both Rauch and TIA is shown in Figure 4.32(a). It is a class A p-n structure to increase the transconductance gain. The output node voltage is fixed through a local CMFB through $M_{p1,3}$ and $M_{p1,4}$. The first stage has a dominant pole at the output node which is cancelled by adding a zero at that node through $R_{z,1}$ and $C_{z,1}$. The second and third stage, shown in Figure 4.32(b) and (c) respectively, play role as the middle stages to boost the gain. The second stage is a simple PMOS differential stage ($M_{p2,1}$, $M_{p2,2}$) with a self-bias NMOS load ($M_{n2,1}$, $M_{n2,2}$). Similarly, like the first stage, the zero is added at the output node through $R_{z,2}$ and $C_{z,2}$ to improve the overall phase behaviour of the system. The third stage is same as the second one except

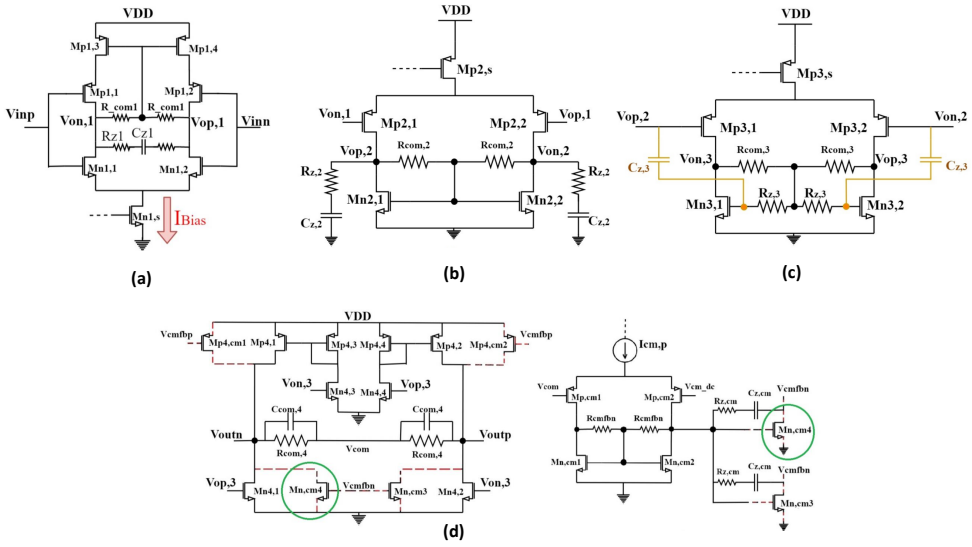


FIGURE 4.32: Rauch filter main path stages schematic: (a) 1st stage. (b) 2nd stage. (c) 3rd stage (d) 4th stage with CMFB circuit.

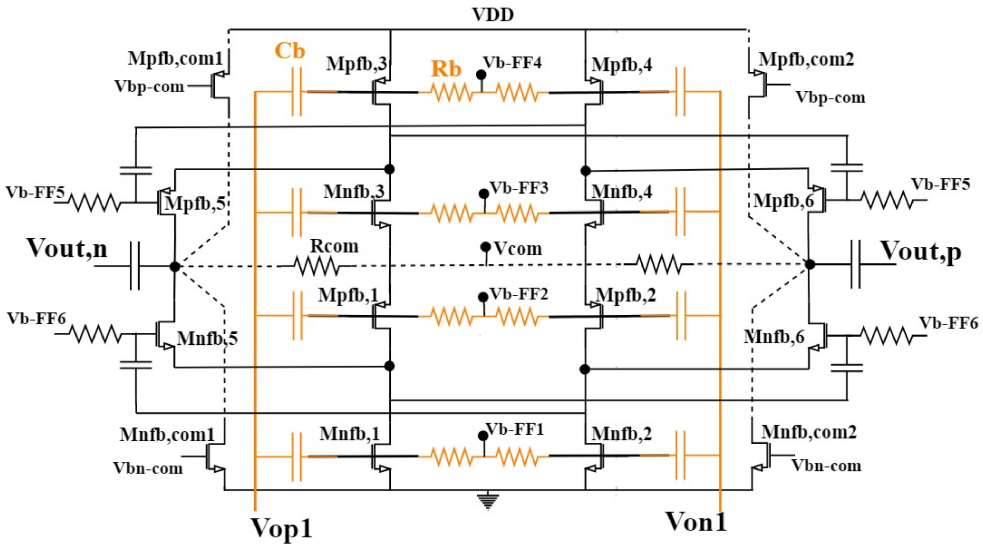


FIGURE 4.33: feed-forward stage of the Rauch filter with folded cascode structure.

here a boosting cap, $C_{z,3}$, is added from the input to the gate of the $M_{n3,1}$

and $M_{n3,2}$. The $C_{z,3}$ becomes short at higher frequencies adding a zero-pole doublet in the circuit, which inceases the gain at the higher frequency. The final stage in the main path is a P-N circuit, as shown in Figure 4.32(d). To ensure common-mode stability, two common mode circuits for the P and N sides are employed to maintain correct symmetry between the top and bottom sides of the final stage. The feed-forward stage with a folded cascode structure, as illustrated in Figure 4.33, bypasses the intermediate and final stages. The total G_m is increased by a factor of four by ac-coupling at the input and output nodes and inserting four transistors in each branch. The combination of the folding cascode and stacked p-n topology results in a power-efficient structure with enough room for a swing at the output node, which is critical for the linearity of the circuit.

The first stage is the most power hungry with 1.5 mA, the last and feed-forward stage burns 1 mA. With a 1.5 V supply, the total current consumption of the Rauch filter is 5.3 mA. The TIA filter features a circuit architecture that is similar to the Rauch filter, with three stages in the main path and a feed-forward stage that links the first stages's output to the last one.

4.2.2 Measurement results

The second-order Rauch filter was fabricated in 28nm TSMC technology and tested as a stand-alone block. Figure 4.34 shows the post-layout simulation

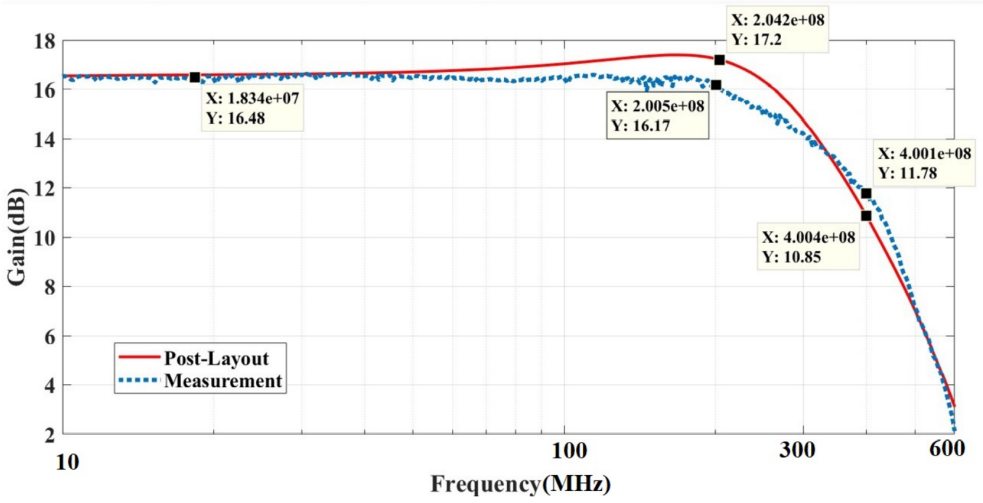


FIGURE 4.34: transfer function of the Rauch filter.

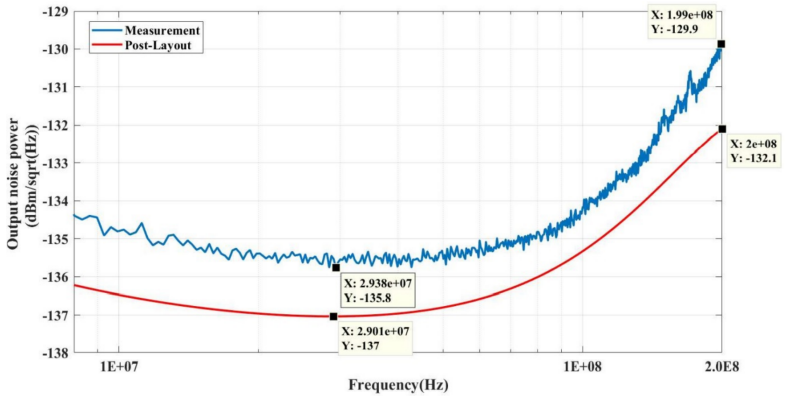


FIGURE 4.35: output noise of the Rauch filter.

and measurement result of the filter transfer function. The filter has an in-band gain of 16.5 dB and -1dB bandwidth of 200 MHz. The measurement results show nearly a flat response in bandwidth with a difference of less than 1 dB. The noise was measured using an AP033 active differential probe. A typical setup for noise measurements include a probe that offers a gain by a factor of 10. Figure 4.35 compares the output noise power of post-layout and measurement results. The measurement and post-layout results reveal a difference of less than 2 dB, which is mostly due to the bias-tee used on the PCB to isolate the DC and RF parts of the circuit and protect it from supply noise.

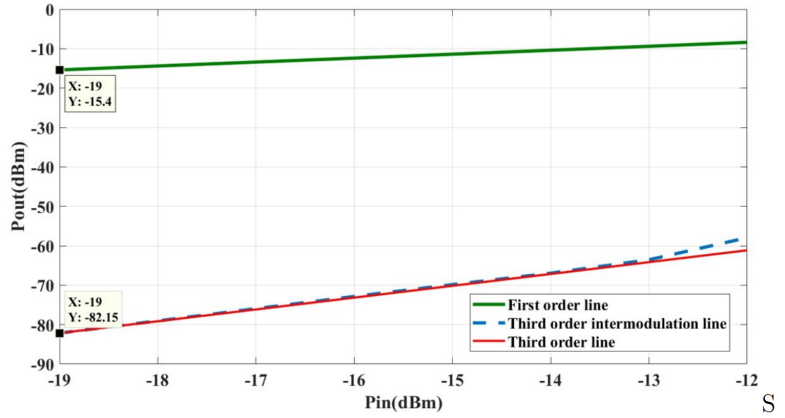


FIGURE 4.36: output intermodulation tone by applying two tones at 180 and 190 MHz.

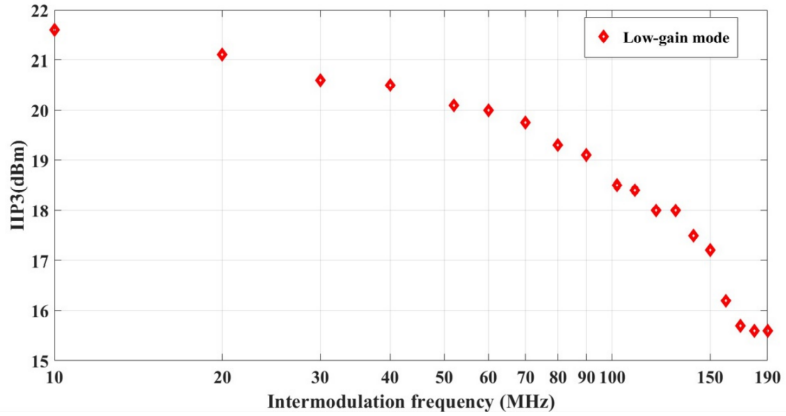


FIGURE 4.37: IIP3 vs intermodulation tone frequency.

To verify the linearity, two tones at 180 and 190 MHz are applied to the input and the output IM3 is measured at 170 MHz. The input-referred IP3 results in +14.3 dBm as illustrated in Figure 4.36, compared to +16.5 dBm computed in post-layout simulation. The measured results show that the filter can meet the receiver requirement of +15 dBm of OIP3. The effect of intermodulation tone's position on linearity is investigated by applying the first tone at 100 MHz and shifting the second tone from 10 MHz to 190 MHz with the step of 10 MHz. Moving the IM3 tone to a higher frequency reduces the measured IIP3, as shown in Figure 4.37. Non-linearity is expected to increase as one approches

	This Work	IEEE Trans. 2012 [57]	IEEE Trans. 2013 [58]	ISSCC 2015 [54]
Technology	28nm CMOS	90nm CMOS	180nm CMOS	28nm FD-SOI
Supply[V]	1.5	1.2	1.8	1
$P_{diss.}$[mW]	7.9	2.28	4.1	5.6
BW [MHz]	200 (-1dB)	255(-3dB)	240(-3dB)	459(-3dB)
order	1^{st}	5^{th}	4^{th}	3^{rd}
IIP3[dBm]	14.3	14	12.5	2.4
$V_n[\mu V_{rms}]$	68	199	203	126
IMFDR3 [dB]	56.5	50	49	45
FoM_{IM3} [dBJ^{-1}]	162.9	162	N/A	157

TABLE 4.6: Rauch filter performance comparison with State-of-the-art.

the band edge and G-loop gain decreases, hence the IIP3 decreases as shown in the plot. The 1 dB compresssion point at input is -3.2 dBm, measured by applying a tone at 100 MHz. Table 4.6. compares the Rauch filter with the state-of-the-art similar research works.

This chapter concludes with the design of two baseband paths. A 1 GHz bandwidth open-loop current mode filter is presented in the HF BB path. The measurement results show that the presented regulated cascode architecture is potentially very linear in comparison to the state-of-the-art Gm-C filters. Different frequency dependent negative capacitance circuits are also presented in order to further improve the filter Q and OOB selectivity. Following the open-loop filter, a wideband TIA is presented, with a closed loop bandwidth of 1 GHz. It is based on an OTA, which has an open-loop bandwidth of 7 GHz and an open-loop gain of 24 dB at 1 GHz, which is high enough to ensure good linearity performance. In LF-BB path a third-order filter is presented made by cascading a second-order Rauch filter and a first-order TIA. The measured Rauch filter shows proper matching with post-layout results. The measured results satisfy the full receiver requirements in terms of noise and linearity. In the next chapter, the measurement results of the full receiver will be presented.

Chapter 5

Full Receiver Experimental Results

Abstract
This chapter presents the entire receiver measurement results, complying with the design specifications. The receiver's measurement setup will be expalined first. The measurement results of the high frequency baseband path will be reported in the first part. The receiver's input matching, transfer function, linearity and noise performance will be evaluated. The measurement results of the low-frequency baseband path will be reported in the subsequent section, assessing the same performance characteristics mentioned before. Finally, the measured receiver performance comparison with the initial specifications will be presented.

5.1 Experimental Setup

The receiver is implemented in TSMC 28nm CMOS technology. Figure 5.1 depicts the layout of the receiver and microphotograph of the chip. The chip size is 1.4 mm $\times$ 1.4 mm and the active area of each block is listed in Table 5.1 together with the area of balun and XMFR. The chip is wire-bonded and mounted on a PCB. The power supply and biasing pads are wire-bonded, while the input and LO signals are applied directly to the pads through single-ended and differential probes, respectively. Two PCB boards have been built for the testing purposes. The test set-up environment is shown in Figure 5.2. One board is used for providing the biasing and digital bits, while the other is used for testing the chip on the probe station.

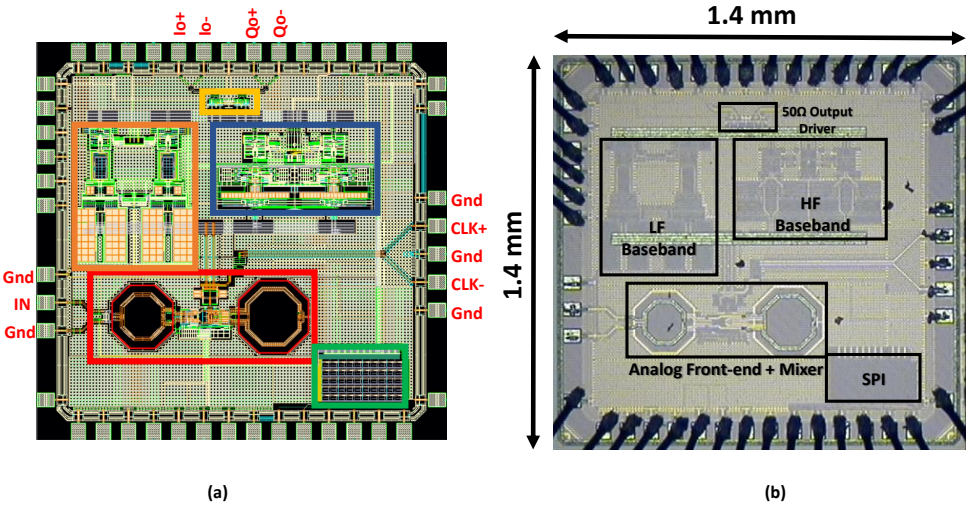


FIGURE 5.1: (a) layout of the receiver. (b) microphotograph of the chip.

Blocks	Active Area
Balun	0.06 mm^2
XMFR	0.08 mm^2
1° LNTA + 2° LNTA	0.02 mm^2
Mixer + Frequency divider	0.003 mm^2
Rauch filter + TIA	0.13 mm^2
Open loop filter	0.09 mm^2
Wideband TIA	0.38 mm^2
Total Active Area	0.763 mm^2

TABLE 5.1: Active area of the receiver blocks.

The measurement setup is shown in Figure 5.3 . The input signal is generated by an *Agilent E8257* signal generator and provided to the chip using a *Cascade Infinity GSG* single-ended probe. The differential LO signal is provided by the *Anritsu MG3692A* signal generator through the *Cascade Infinity GSGSG* differential probe. The outputs are sensed using a *R&S RT-ZD40* probe and measured on a *R&S FSQ8* signal analyzer. Biasing currents and voltages are applied through a *NI cRIO-9014* using a software routine implemented in Labview. Digital bits are provided through a *NI-USB8451* SPI interface.

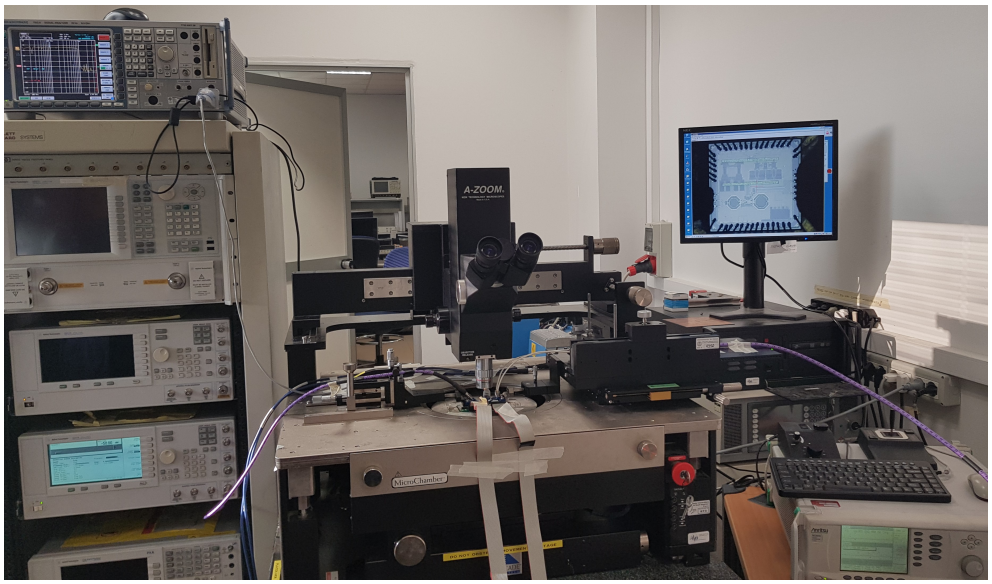


FIGURE 5.2: test-setup environment.

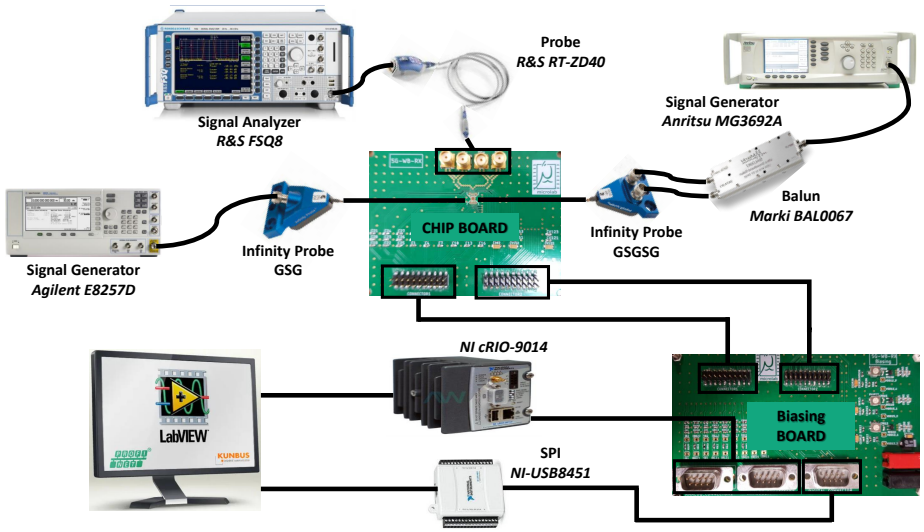


FIGURE 5.3: measurement setup for the characterization of the receiver.

5.2 High Frequency BB path Measurement Results

In this section, the measurement results of the high frequency baseband path will be discussed. The HF-BB path consists of an open-loop current mode filter followed by a wideband TIA. It covers BB bandwidth from 400 MHz up to 1 GHz. In the following subsections, the receiver's input matching, downconverted gain, linearity, and noise performance will be evaluated.

5.2.1 Input matching

Input matching was verified using a S11 measurements on a *Agilent E8361C* PNA network analyzer. The results for the maximum receiver gain are shown in Figure 5.4 (a), while the results for the minimum receiver gain are shown in Figure 5.4 (b). As can be observed, a good matching is established around the carrier frequency of 7 GHz, where a relatively deep notch is obtained. To achieve matching, a digitally controlled variable capacitor is used at the input. The capacitor value is 280 fF for the maximum gain. When the minimum gain is obtained at the balun's input through a voltage divider, the cross-coupled capacitors are disconnected in the LNTA to retain the matching. As a result, the parasitic capacitance reflects back at the balun's primary, shifting the matching at lower frequencies. To achieve the matching at minimum gain, the input capacitor is reduced to the value of 60 fF using digital bits. Input matching better than 12 dB in the case of maximum gain and 15 dB in the case of minimum gain is achieved over the 2 GHz bandwidth around the carrier frequency.

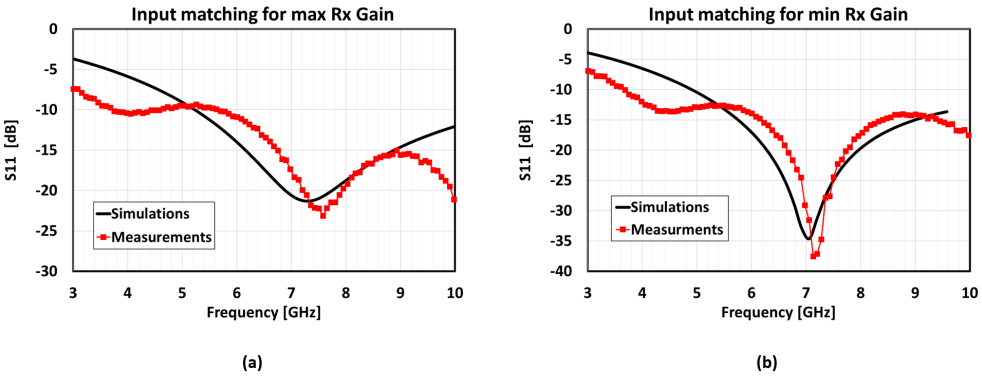


FIGURE 5.4: measurements of S11: (a) for max Rx gain (b) for min Rx gain

5.2.2 Downconverted Receiver Gain

Receiver gain was evaluated using the measurement setup depicted in Figure 5.3 where a frequency sweep is generated from 3 GHz to 11 GHz using a signal generator. Figure 5.5 shows the gain vs IF frequency for the upper and lower band around the 7 GHz LO frequency. At f_{LO} = 7 GHz, the in-band gain is 45

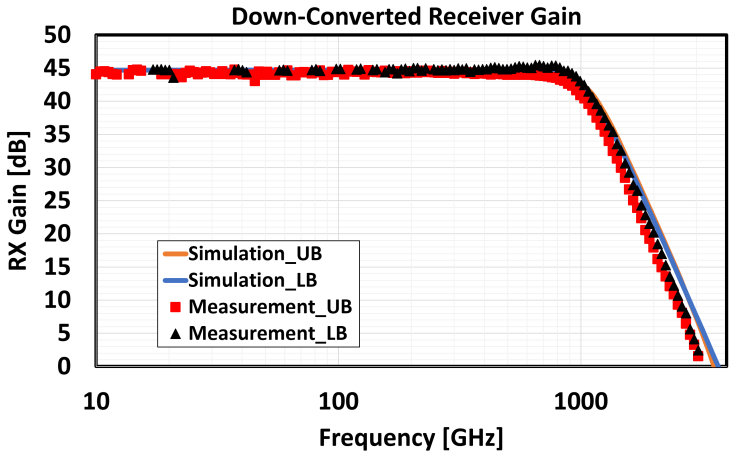


FIGURE 5.5: downconverted receiver gain for lower and upper band.

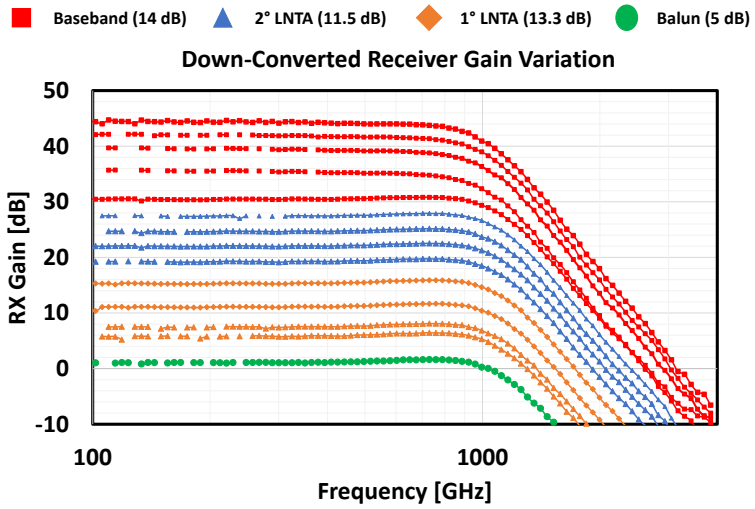


FIGURE 5.6: receiver gain variation.

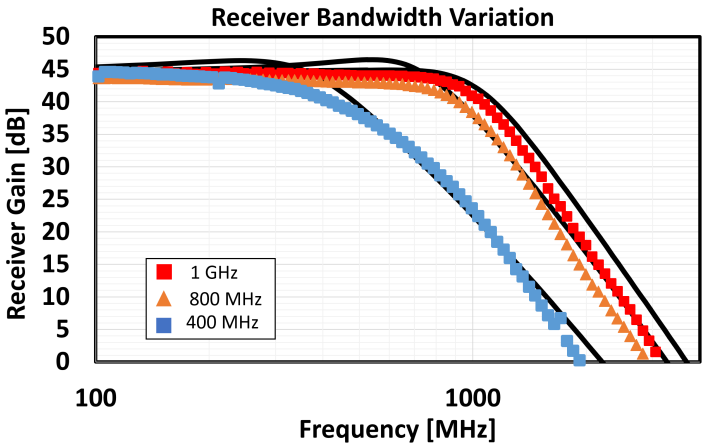


FIGURE 5.7: receiver bandwidth variation.

dB, which is compliant with the requirements. The down-converted gain at 1 GHz maximum baseband bandwidth is just decreased by 1.6 dB for lower band and 2.3 dB for upper band. An equivalent of 4th-order 1 GHz BW Butterworth filter is created by combining an open-loop filter, a negative capacitance circuit, and a wideband TIA. From 1 GHz to 4 GHz, the OOB selectivity is 50 dB, which is well above the specification of 33 dB. Thanks to the complex feedback loop around the output TIA, the upper and lower band have a mismatch of less than 1 dB around 1 GHz. Figure 5.6 shows the measurement results of the receiver chain's gain variation. The gain is varied from 45 dB down to 0 dB. The baseband provides 14 dB of gain variation accomplished by adjusting the current mirror gain in the open-loop filter. The gain is varied in 4 steps using digital bits provided by the SPI interface. The bits connect and disconnect the current-mirror branches in the open-loop filter, causing the current gain to vary. The front-end has a gain variation of 31 dB out of which 25 dB of gain variation is achieved by using the current-steering technique in the two cascaded LNTAs and 6 dB is implemented introducing a passive attenuation at the input of the balun while maintaining the matching. Figure 5.7 shows the receiver transfer function as the cut-off frequency varies from 400 MHz to 1 GHz. The bandwidth variation is performed by changing the capacitors that are implemented as arrays and its values are controlled using the digital bits. In all the channel bandwidths, the measured OOB selectivity from band edge to 4x-band edge is higher than 33 dB meeting the required specifications.

5.2.3 Linearity and Compression Measurements

The receiver's linearity was evaluated using a two-tone test that combined signals from *Agilent E8257* signal generators using a *Suhner-4901* power combiner. OIP3 was tested for various receiver gain configurations. Two tones are injected at offset frequencies of 400 MHz and 500 MHz with respect to f_{LO} - 7 GHz such that IM3 is at 300 MHz (at BB). Figure 5.8 shows the fundamental and IM3 power versus tone power for two tones at 400 and 500 MHz offset from the 7 GHz LO with a maximum receiver gain of 45 dB, exhibiting the predicted IM3 slope (3 dB/dB) in the extrapolation point. For maximum receiver gain, the in-band IIP3 of -18.93 dBm is achieved. Figure 5.9 shows the OIP3 with respect to receiver gain variation for two tones injected at 400 MHz and 500 MHz offset from 7 GHz LO such that IM3 tone is at 300 MHz at baseband. For all gain configrations, OIP3 over +23.5 dBm is measured. As the gain varies in baseband, OIP3 shows opposite behaviour compare to simulated one, however the average value remains around +26 dBm. The receiver satisfies required specifications as the OIP3 remains above +15 dBm for all the gain configurations.

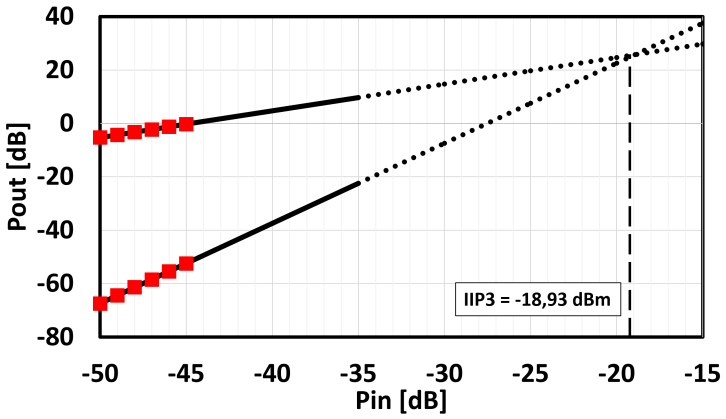


FIGURE 5.8: fundamental and IM3 power vs. tones input power.

Compression performance was examined using the same measurement setup adopted for linearity. Compression measurements are done for maximum and minimum receiver gain for 1 GHz BB bandwidth. For maximum receiver gain, the compression on in-band signal was measured by sweeping the power of the input signal at f_{LO} + 300 MHz and f_{LO} + 700 MHz and seeing the down-

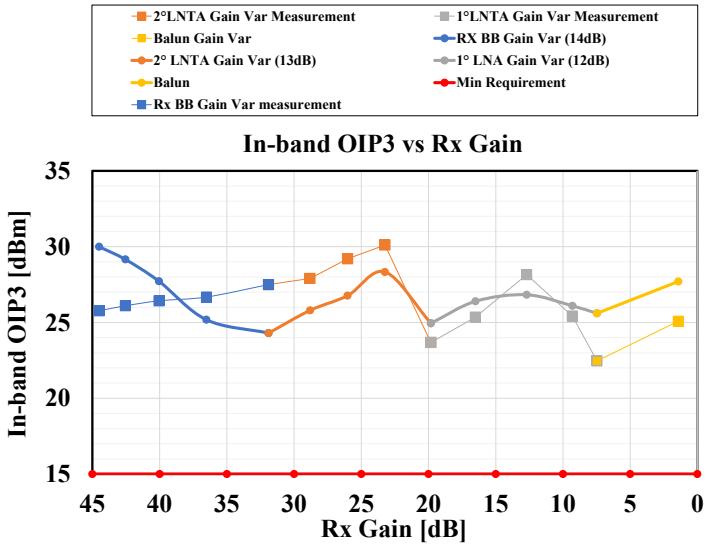


FIGURE 5.9: In-band OIP3 vs. receiver gain.

converted signal at the receiver's output. Figure 5.10 shows that the gain compresses by 1 dB for a -27.5 dBm input signal at 300 MHz and for a -33 dBm input signal at 700 MHz. Figure 5.11 shows the in-band compression for the case of minimum receiver gain. As can be observed, the gain compresses by 1 dB for a +9 dBm input signal at 700 MHz. The receiver statisfy the require-

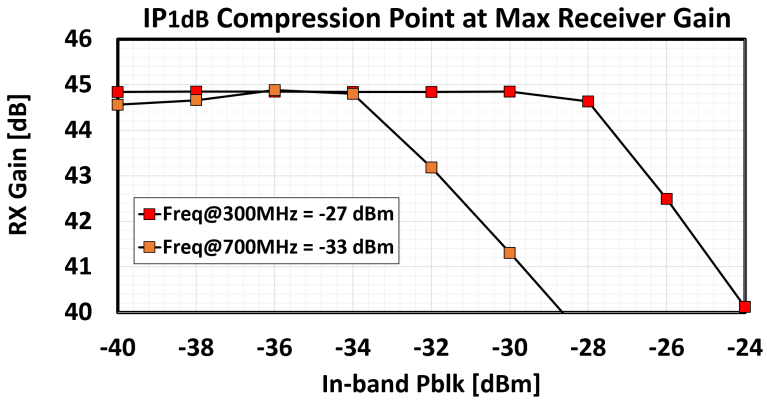


FIGURE 5.10: In-band compression with blockers at f_{blk}=f_{LO}+300MHz and f_{blk}=f_{LO}+700MHz for maximum receiver gain.

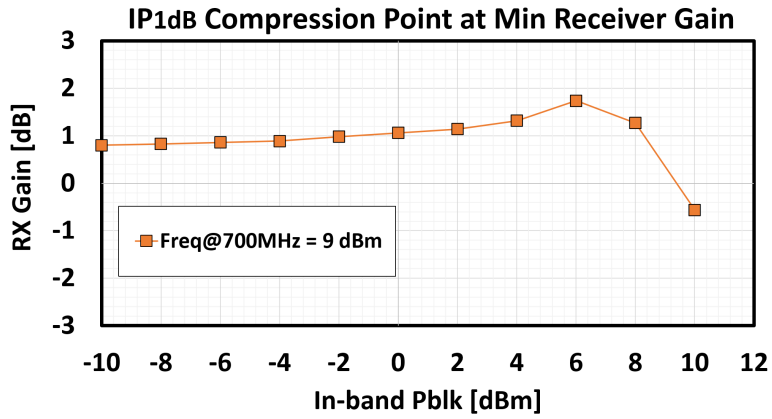


FIGURE 5.11: In-band compression with blocker at f_{blk}=f_{LO}+700MHz for minimum receiver gain.

ments of -39 dBm of 1dB compression point for maximum receiver gain and +6 dBm for minimum receiver gain.

5.2.4 Noise Performance

The plot in Figure5.12 (a) shows the post-layout simulation and measurement results of the NFdsb for the case of maximum receiver gain of 45 dB and maximum bandwidth of 1 GHz. An integrated NFdsb of 5.6 dB is achieved within the bandwidth of 1 GHz in the post layout simulation results. The wide bandwidth probe *R&S RT-ZD40* used to measure the receiver gain has an in-built attenuation of 20 dB which limits the noise measurements because of its high noise floor. A low frequency probe *LeCroy AP033* with a bandwidth of 500 MHz was used. Conseguently, noise measurements are limited up to 500 MHz. The integrated NFdsb measured up to 400 MHz is 5.75 dB. The integrated noise contribution of different receiver blocks at the output is shown in Figure5.12 (b). The total integrated noise at the output over 1 GHz bandwidth is 2.8 $\times$ 10^{-5} V^2_{rms}. The front-end contributes around 48% of the total noise at the output whereas baseband contributes 15% thanks to the high RF gain at the front-end. The 1°LNTA and balun contributes the most noise from the front-end. The open-loop filter contributes 14.46% of total noise in the BB section, whereas the wideband TIA contributes only 0.6%, thanks to the high RF transconductance gain and 14 dB of current gain provided by the open-loop filter. The integrated NFdsb (10MHz - 1GHz) with respect to the receiver gain is shown in Figure 5.13. The NF is 5.6 dB for maximum receiver gain of 45 dB.

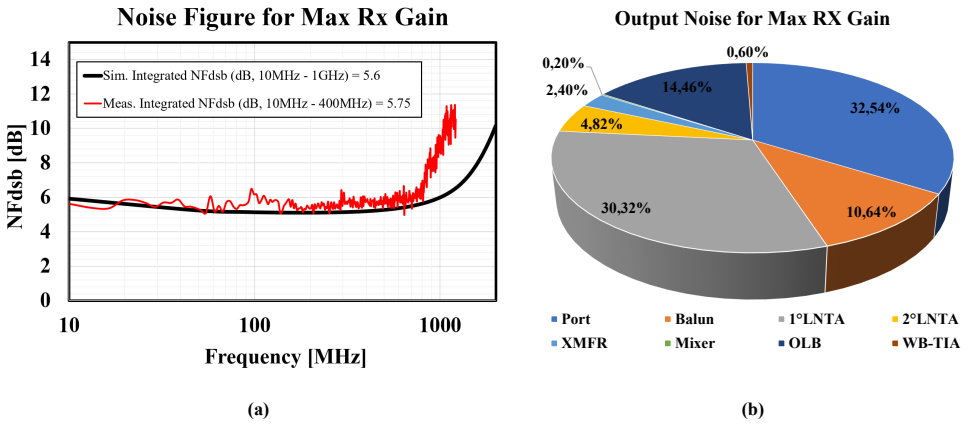


FIGURE 5.12: (a) NFdsb for maximum Rx Gain. (b) output noise contribtution for maximum Rx gain.

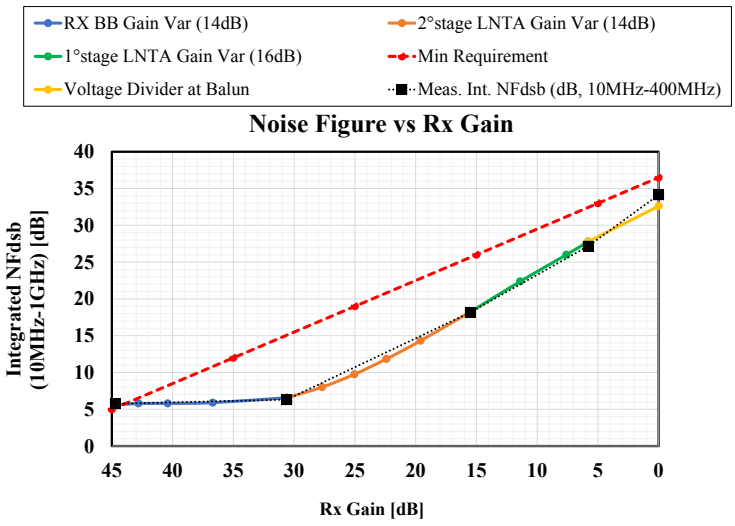


FIGURE 5.13: integrated NFdsb (10MHz - 1GHz) vs Rx Gain.

The NF start to increase as the receiver gain decreases. The receiver gain begin to decrease from the baseband. The NF is only increased by 1 dB for the first

14 dB of gain attenuation in the baseband, leaving enough margin to meet the specification of 0.7 dB of noise figure increase for every dB of gain decrease. The gain in the front-end is reduced using the current-steering method, and as the gain in the LNTAs is reduced, the noise contribution of the cascode and cross-coupled transistor increases. Eventually, 25 dB of gain attenuation at the front-end increases the NF from 6.5 dB to 27.5 dB. The final 6 dB of gain attenuation at the input matching network increases the NF by 5 dB. Due to probe's limited bandwidth, noise measurements are limited up to 500 MHz. The measured NFdsb integrated up to 400 MHz is shown in Figure5.13. The measurements matches well with the post-layout results. The NF slope remain below the minimum requirement of 0.7 db for every dB of gain decrease.

5.2.5 Power Consumption

Figure5.14 (a) shows the dissipated power with respect to the receiver gain. The dissipated power is 68 mW at maximum receiver gain. As the gain decreases, the dissipated power drops to 56 mW. Only when the gain in the BB is reduced does the power decrease. Because the variable current mirror gain in the open loop filter is used to vary the gain in the BB. The current mirror branches are turned off to reduce gain, which saves power dissipation. The gain variation in the front-end, on the other hand, is accomplished using the current-steering method, and power consumption remains constant as the gain decreases. The pie-chart of power distribution for maximum receiver gain is shown in Figure5.14(b). The I-Q BB section dissipates 64 % of the total power. The open-loop filter in the BB section dissipates 40% of the total

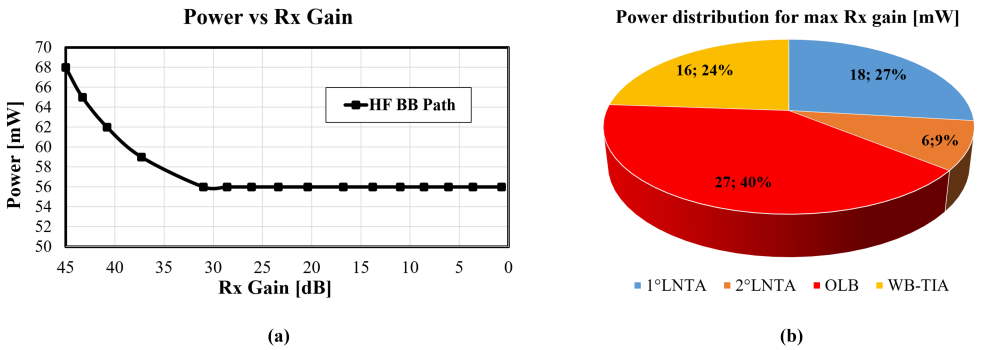


FIGURE 5.14: (a) dissipated power vs Rx gain. (b) power distribution for maximum Rx gain.

power because the cut-off frequency of the filter is determined by the gm of the input transistors, and increasing gm also reduces their noise contribution. To achieve a 1 GHz wide-bandwidth and better noise performance, huge power is required. Furthermore, in an open-loop filter, the negative capacitance circuit requires a large gm to improve its noise contribution and as a result, it dissipates nearly 38% of the power dissipated in the open loop filter. Similarly, the wideband TIA dissipates 24% of total power because it must 1 provide 1 GHz close loop bandwidth and, in order to do so, the required (OTA) bandwidth must be much higher than 1 GHz, which necessitates a large amount of power. The 1° LNTA dissipates 18 mW in front-end because it requires large current to achieve input matching. The 2° LNTA dissipates only 6 mW as gm in 2°LNTA is increased thanks to passive-gate boosting technique which reduces its noise contribution but limits its linearity performance.

5.3 Low Frequency BB path Measurement Results

In this section Low Frequency BB path measurement results will be discussed. The LF BB path is made up of a second-order Rauch filter followed by a first-order TIA. It supports BB bandwidths ranging from 25 to 200 MHz. The same receiver performance characteristics as for the HF BB path will be evaluated in the following subsections.

5.3.1 Downconverted Receiver Gain

The same measurement setup as for the high-frequency BB path is used to evaluate the receiver gain for the low frequency BB path. A frequency sweep is generated at the input from 6.2 GHz to 7.8 GHz. Figure5.15 shows the down-converted receiver gain vs IF frequency for a 7 GHz LO. In-band gain at f_{LO} = 7 GHz is 45.5 dB. In-band gain remain flat up to 200 MHz offset frequency. The difference between upper and lower band gain is less than 2 dB around 200 MHz IF frequency. An OOB selectivity of +34 dB is achieved from 200 MHz to 800 MHz bandwidth. The receiver gain variation is depicted in Figure 5.16. A 14 dB gain variation is implemented in baseband using a variable feedback resistor in the TIA following the Rauch filter. The receiver transfer function is shown in Figure5.17 as the cut-off frequency is changed from 200 MHz down to 25 MHz. The bandwidth is varied by changing the capacitor values in the Rauch filter and TIA. From band edge to 4x band edge, an OOB selectivity of greater than 33 dB is achieved for all channel bandwidths, meeting the required specifications.

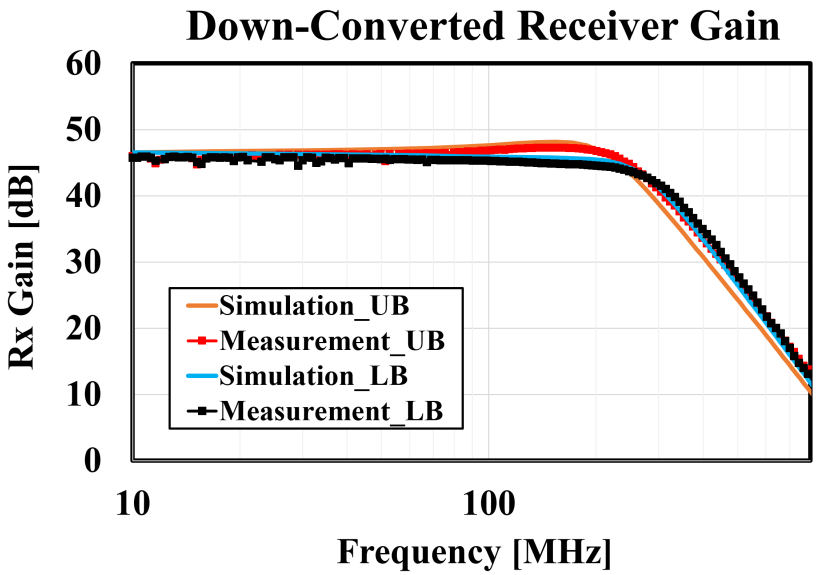


FIGURE 5.15: downconverted receiver gain for lower and upper band.

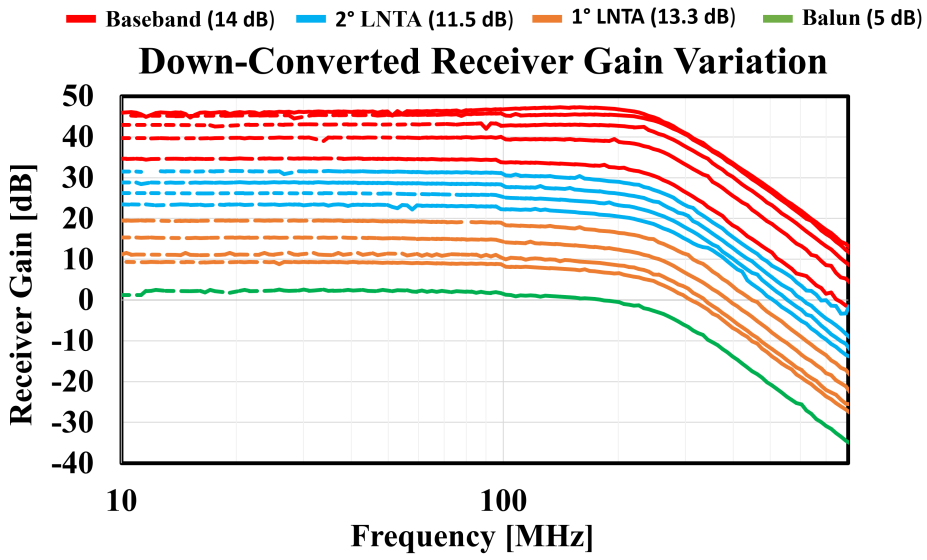


FIGURE 5.16: receiver gain variation.

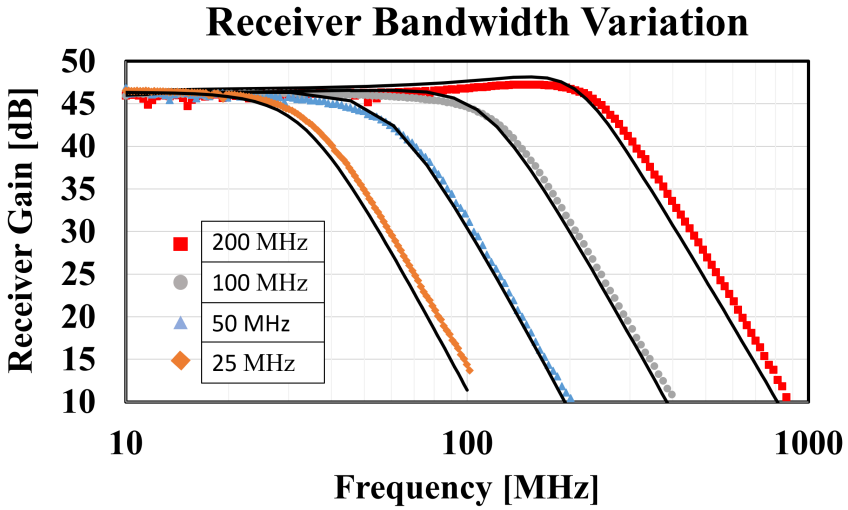


FIGURE 5.17: receiver bandwidth variation.

5.3.2 Linearity and Compression Measurements

Similarly as HF-BB path, OIP3 is measured for different receiver gain configurations. Two tones are injected at offset frequencies of 175 MHz and 180 MHz from f_{LO} - 7 GHz, so that IM3 tone is at 170 MHz (at BB). Figure5.18 depicts the OIP3 with respect to the receiver gain. OIP3 is measured to be greater than +21.4 dBm for all gain configurations, well above the specification of +15 dBm.

Compression measurements are performed in the case of maximum receiver gain for a 200 MHz BB bandwidth. The compression on in-band signal was measured by sweeping the power of the input signal at f_{LO} + 160 MHz and looking at the downconverted signal at the receiver's output. As shown in Figure5.19, the 1dB compression point at the input is -32 dBm. The receiver meets the -39 dBm 1dB compression point requirement at maximum gain. For minimum receiver gain, compression measurements are limited due to the maximum output power of the signal generator (+10 dBm). At minimum gain of 0 dB, the receiver has a 1dB compression point above +10dBm.

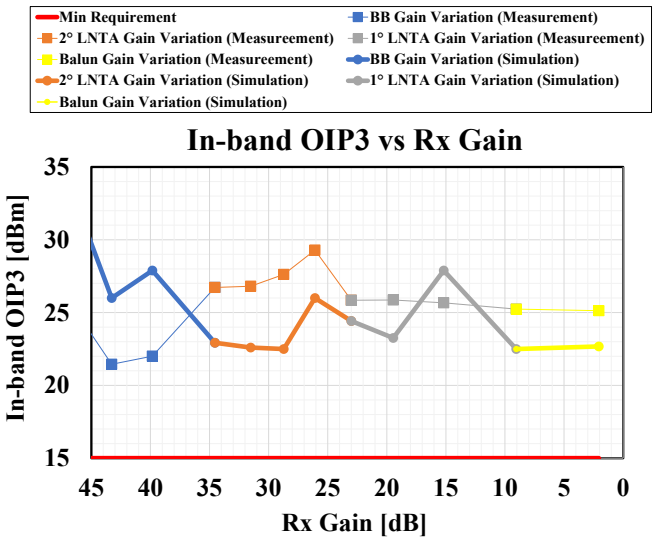


FIGURE 5.18: In-band OIP3 vs. receiver gain.

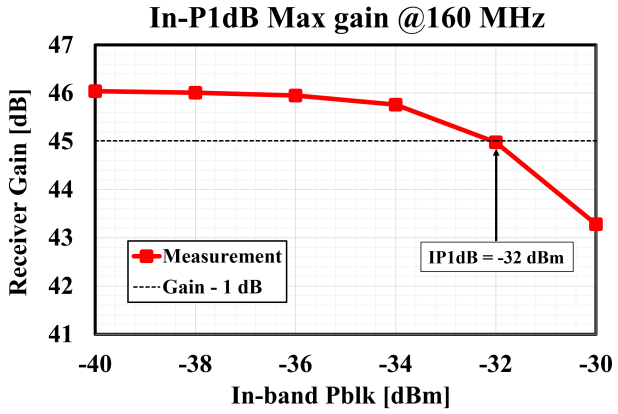


FIGURE 5.19: In-band compression with blocker at $f_{blk}=f_{LO}$ + 160 MHz for maximum receiver gain.

5.3.3 Noise Performance

The post-layout and measurement results of the NFdsb for a maximum receiver gain of 45 dB and bandwidth of 200 MHz are plotted in Figure 5.20(a). Within a bandwidth of 200 MHz, an integrated NFdsb of 5.82 dB is measured. Figure 5.20(b) depicts the pie-chart of the noise contribution of different receiver

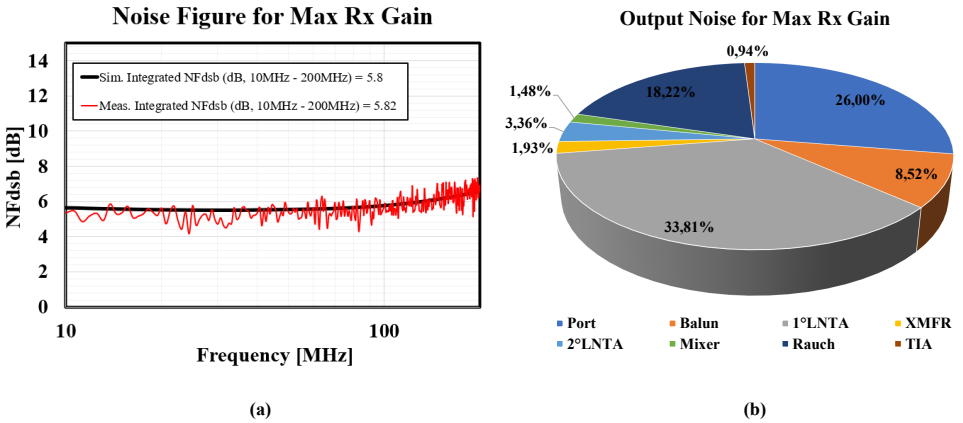


FIGURE 5.20: (a) NFdsb for maximum Rx Gain. (b) output noise contribtution for maximum Rx gain.

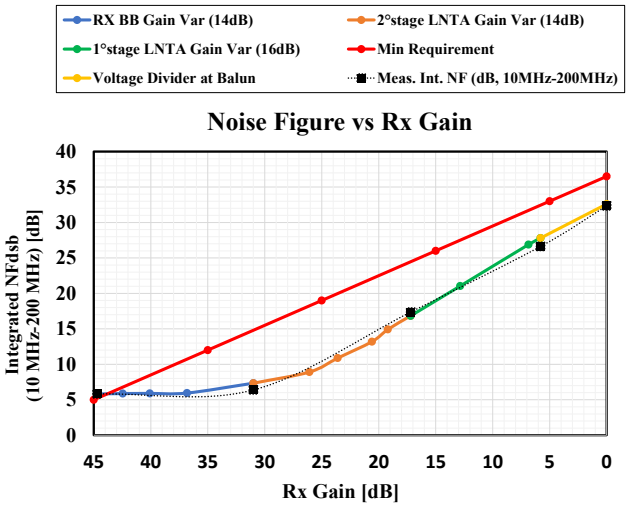


FIGURE 5.21: integrated NFdsb (10MHz - 200MHz) vs Rx Gain.

blocks at the output. The total output integrated noise from 10 MHz to 200 MHz is 7.63×10^{-6} V^2_{rms}. The front-end accounts for 49.1% of the total noise.

In the baseband, the Rauch filter contributes 18.22% of the total noise, whereas TIA following the Rauch filter contributes only 0.94%. Figure5.21 shows the integrated NFdsb (10 MHz - 200 MHz) in relation to the receiver gain. For maximum receiver gain, the NF is 5.85 dB. At minimum receiver gain, NF increases up to 32.35 dB, but its slope remains below the minimum requirement of 0.7 dB for every dB of gain decrease.

5.4 Receiver Performance Summary

Table 5.2 shows the measured receiver performance for the HF and LF BB paths. As shown, the receiver meets all of the critical specifications except for the NF of 5 dB at maximum receiver gain. It supports RF channel bandwidths ranging from 50 MHz to 2 GHz. Input VSWR is 1.32 for maximum receiver gain and 1.04 for minimum receiver gain, both of which are well above the specification. The receiver provide full gain variability from 45 dB down to 0 dB. For all gain steps, the measured in-band OIP3 is greater than 23.5 dBm for the HF BB path and greater than 21.4 dBm for the LF BB path. For maximum receiver gain, the input 1dB compression point is measured -33 dBm for HF BB path at 700 MHz frequency offset from LO and -32 dBm for LF BB path at 160 MHz frequency offset from LO. For minimum receiver gain, input 1dB compression point is measured +9 dBm for HF BB path and it is above 10 dBm for LF BB path since measurements are limited by the maximum output power provided by the signal generator. For all channel bandwidths in both HF and

Item	Condition	Specs	HF BB path	LF BB path	Unit
Carrier Frequency		7000	7000		MHz
RF Channel BW	Mode(50, 100, 200, 400 400,800,1600 and 2000)		400, 800 and 2000	50, 100, 200 and 400	MHz
Input VSWR	in all modes	1.5	1.32 (Max Gain) 1.04 (Min Gain)		
Gain Control Range	Max Gain	45	45		dB
	Min Gain	0	0		dB
Noise Figure	@LNA input max gain	5	5.6	5.8	dB
Noise Figure Slope		0.7	<0.7	<0.7	dB/dB
Input P1dB Input P1dB	Max Gain, inband Min Gain, inband	-39 6	-33 9	-30.3 >10	dBm
OIP3	All gain step, P_{RXOUT}=-8dBm	>15	>23.5	>21.4	dBm
Analog Filter Selectivity	From Bandwidth to 4 × Bandwidth	-33	>33	>33	dB
Inband Flatness	in all modes	1	2	0.5	dB
Power Consumption	Max gain, Max BW		68	51	mW

TABLE 5.2: Full receiver performance summary.

LF BB paths, BB filter selectivity is measured above 33 dB from bandwidth to 4 × bandwidth. In terms of noise performance, post-layout simulations show that the HF BB path provides 5.6 dB of integrated NFdsb (10 MHz - 1 GHz) at maximum receiver gain. Due to probe's limited bandwidth, noise measurements are limited up to 400 MHz. The measurement results match the post-layout simulations very well. The NFdsb (10 MHz - 400 MHz) measured is 5.75 dB. For LF BB path, the measured integrated NFdsb (10 MHz - 200 MHz) at maximum receiver gain is 5.82 dB. For every dB of gain reduction, the noise figure slope remains below 0.7 dB for both HF and LF BB paths. As previously stated, 1°LNTA is the primary source of noise. Future designs can improve noise performance by increasing the gm of the input transistors in 1°LNTA at the expense of increased power consumption. Furthermore, in the HF BB path, the open-loop filter produces 14% of the total noise, which can be improved by increasing the current in the CG branch, as input transistor's noise is the dominant one, or by increasing the transconductance gain at the RF front-end, which reduces the impact of BB noise on the overall noise of the receiver.

Conclusions

In this thesis, a design of wideband direct-conversion receiver is presented as a part of the heterogeneous transceiver architecture for 5G wireless applications. The goal was to design a receiver that covers a wide range of channel bandwidths belong to 5G mm-wave and beyond while meeting the critical noise and linearity requirements of the 5G standard.

A current-mode direct-conversion receiver architecture is opted to achieve good linearity performance. The proposed receiver architecture employs two wideband cascaded LNTAs to achieve high RF transconductance gain and low noise figure. The RF front-end provides 80 mS of transconductance gain which is programmable down to 2 mS, with comparable linearity and noise performance to the state-of-the-art designs. The receiver covers RF channel bandwidths from 50 MHz to 2 GHz. The baseband section is divided into two separate paths for this purpose: the LF BB path (covers RF CH. BW 50 MHz - 400 MHz) and the HF BB path (covers RF CH. BW 800 MHz - 2000 MHz). A 1 GHz BB bandwidth open-loop current mode filter is presented in HF BB path. The filter is based on a regulated cascode architecture. The measurement results shows that the presented architecture is potentially very linear compare to the state-of-the-art Gm-C filters. In addition, different negative capacitance circuits have been studied including a novel frequency dependent negative capacitance circuit that provides negative in-band capacitance and positive out-of-band capacitance. Such a solution further improves the Q and OOB selectivity of the open-loop filter. Following the open-loop filter, a wideband TIA with a closed-loop bandwidth of 1 GHz is presented. It is based on an OTA with an open-loop bandwidth of 7 GHz and an open-loop gain of 24 dB at 1 GHz, which is sufficient for good linearity performance. In comparison to the state-of-the-art, the presented TIA provides OP1dB and inband IMFDR3 that are significantly higher.

The receiver has been fully integrated, and the measurement results are fully complying with the design specifications. The receiver has a gain range of 45 dB to 0 dB that is fully programmable. It has an OOB selectivity of more than 33 dB at a frequency four times the band edge and covers BB bandwidth from 25 MHz to 1 GHz. In all gain configurations, the receiver has a measured inband OIP3 of greater than +23 dBm for the HF BB path and greater than +21 dBm for the LF BB path. It fully complies with the linearity and selectivity requirements for 5G FR2 bands mentioned in 3GPP Release 16. For maximum gain, the receiver has a NF of less than 6 dB and a slope of less than 0.7 dB/dB in the noise increase as the gain decreases.

The measured results show that the receiver is a good candidate for inclusion in a heterogeneous transceiver for 5G wireless applications. The receiver covers channel bandwidths not only belong to 5G FR2 bands (up to 800 MHz using CA) but up to 2 GHz, making it a potential candidate also for future standards as the channel bandwidths increase.

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