

CMOS Vertical Hall Magnetic Sensors on Flexible Substrate

Hadi Heidari, *Member, IEEE*, Edoardo Bonizzoni, *Member, IEEE*, Umberto Gatti, *Member, IEEE*, Franco Maloberti, *Life Fellow, IEEE*, and Ravinder Dahiya, *Senior Member, IEEE*

Abstract—This paper presents the realization of different Vertical Hall Sensors (VHSs) implemented using a 0.18- μm CMOS technology and mounted on flexible substrates. Various geometries of VHS have been studied to obtain the optimum sensor device dimension and shape. COMSOL multiphysics simulation results are validated with respect to the electrical behaviour of an 8-resistor Verilog-A model implemented in Cadence environment. Simulation and measurement results are in good agreement. The use of polymeric foils and current spinning technique compensate for the effects caused by mechanical stress and possible fabrication imperfections. Measurement results for a low-offset *basic* VHS in planar state show a sensitivity of $59 \pm 1 \text{ V(AT)}^{-1}$ in voltage-mode and of $8 \pm 0.1 \text{ \%T}^{-1}$ in current-mode.

Index Terms—Vertical Hall sensor, flexible substrate, mechanical stress, magnetic field, CMOS magnetic sensor.

I. INTRODUCTION

HALL effect sensors have been the workhorse magnetic sensor for a large number of applications including biosensors [1], contactless current sensors [2], and electronic compasses [3]. More recently, they have been used in flexible and wearable electronics and a series of flexible and stretchable sensors have been reported [4]–[6]. These include imperceptible giant magnetoresistive (GMR) and magnetic field sensors using Hall effect and organic field effect transistors (OFETs) [7]–[10]. The application of Hall sensors in wearables is interesting and the field will further benefit if the Hall sensors are based on CMOS technology. With CMOS devices it is easier to meet the high performance requirements such as low-power and high-speed, which are needed in many wearable systems especially for wireless communication. Furthermore, it is possible to obtain conformable and wearable CMOS magnetic sensors system using ultra-thin technology which has been reported recently [11].

This work presents CMOS Vertical Hall Sensors (VHSs) mounted on flexible polymeric substrate (Fig. 1(a)) to allow the structure to conform to curved surfaces such as the finger

or the wrist of a human/prosthetic hand. The performance of VHS in four different geometries has been evaluated with sensors operated in both voltage and current mode. The low-offset *basic* VHS has the sensitivities of $59 \pm 2 \text{ V(AT)}^{-1}$ and $8 \pm 0.1 \text{ \%T}^{-1}$ in voltage and current modes, respectively, for an applied external magnetic field range of 0–5 mT. The presented VHS is sensitive to the in-plane component of the magnetic field, B_y , which allows the sensor to detect a magnetic field in its plane. For better sensitivity and reduced offset, the VHS presented here uses an optimized symmetric 4-folded 3-contact (4F 3C) structure with current-spinning technique. The 4-folded structure has been chosen here as, among several possible geometries [12]–[15], this structure is known to result in high resolution and low offset performance [16], [17]. Extending the preliminary work reported in [18], this paper also presents the results from an extensive physical simulation and behavioural modelling of current-mode VHSs on flexible substrate and provides guidelines for the device size, shape, and performance optimization. The effect of substrate bending on device output has also been studied to investigate the role of piezoresistive effect in the performance of electronics [19], [20].

This paper is organized as follows. The VHS design, the numerical analysis for bendability, and the performance variations under uniaxial mechanical stress are presented in Section II. Section III gives a detailed description of the test-chip architecture and the implementation of multi-sensors. This is followed by the VHS modelling and simulation results in Section IV. The experimental results collected from several prototypes fabricated with a 0.18- μm CMOS technology and integrated on flexible substrate are presented in Section V. Finally, the results and future works are summarized in the concluding Section VI.

II. CMOS VERTICAL HALL SENSORS (VHS)

A. VHS structure

VHS devices with various types and shapes have been reported and analyzed in the past for sensitivity and offset. These include four-contact (4C), five-contact (5C), six contact (6C) and 4F 3C type VHS [16], [21]. The comparison of these structures using 3D COMSOL indicates that the current-mode 4F 3C VHS structure is the best choice and the same has been used in this work. Other architectures such as five contacts (5C) [13], [14] and eight contacts (8C) [12] have limitations such as offset and readout complexity, as summarised in Table I. The structure of the 4F 3C VHS,

Manuscript received YYY, 2016; accepted XXX, 2016. Date of publication QQQ, 2016; date of current version ZZZ. The research leading to these results partly received funding from Engineering and Physical Sciences Research Council (EPSRC) First Grant - FLEXELDEMO (EP/M002519/1). The associate editor coordinating the review of this paper and approving it for publication was Prof. XXXX.

H. Heidari, and R. Dahiya are with Electronics and Nanoscale Engineering Research Division, University of Glasgow, Glasgow G12 8QQ, U.K.

E. Bonizzoni, U. Gatti, and F. Maloberti are with Department of Electrical, Computer and Biomedical Engineering, University of Pavia, 27100, Italy

Correspondence to: Ravinder.Dahiya@glasgow.ac.uk

Digital Object Identifier 10.1109/JSEN.2016.xxxxxxx

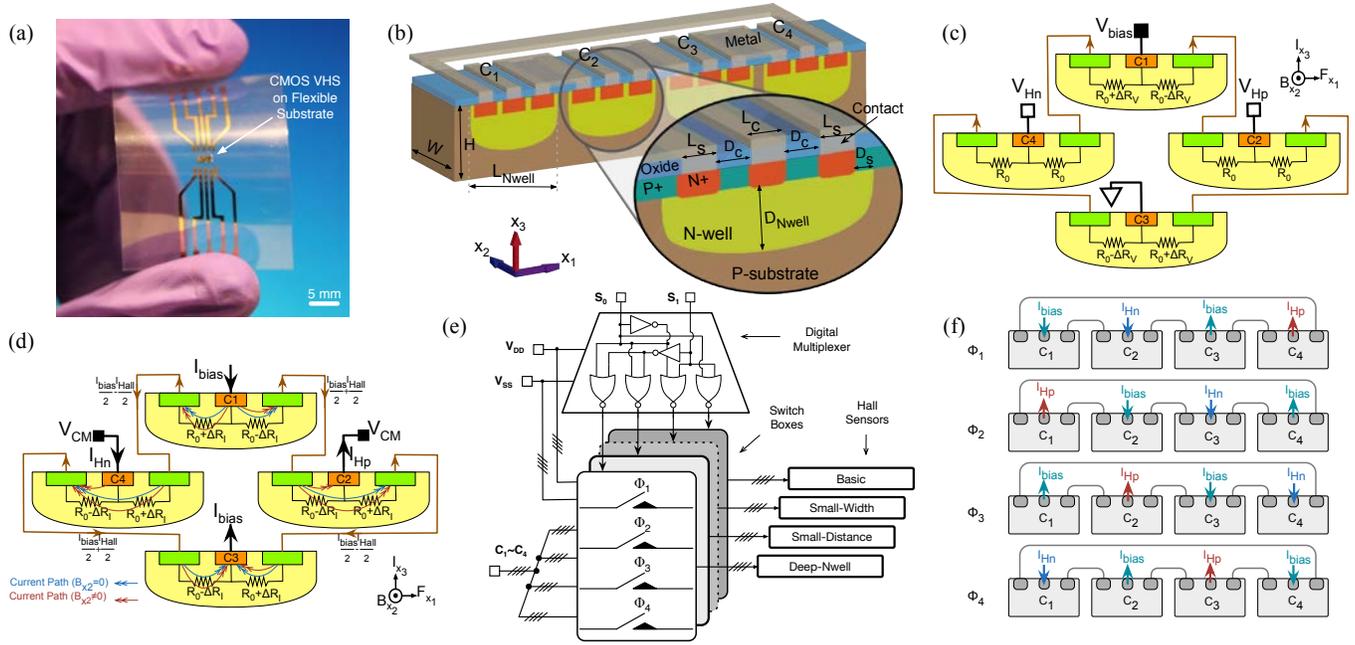


Fig. 1. (a) The VHS chip mounted on a PVC foil. (b) Cross-section of the 4F 3C VHS implemented in a CMOS technology. (c) Voltage-mode configuration. (d) Current-mode configuration with biasing conditions and currents flows. Blue and red lines represent the current paths in the case of zero and non-zero magnetic field, respectively. (e) Block diagram of the test-chip. (f) Sensor configurations in the four current spinning phases.

TABLE I
COMPARISON OF VHSs SENSITIVITY AND OFFSET

Reference	[12]	[13]	[14]	[16]
Geometry	8C VHS	5C VHS	5C VHS	4F 3C VHS
Sensitivity	45 V/AT	1.5 %T ⁻¹	1.525%T ⁻¹	1.16%T ⁻¹
Offset	200 μT	≤1 mT	44 mT	60 μT

shown in Fig. 1(b), has four lined up *n*-wells, each with three *n*+ contacts connected via metal lines as shown in the inset. To reduce the 1/*f* noise and carrier surface losses, the *n*+ diffusions are separated by shallow *p*+ diffusions. The device has four terminals, C₁, C₂, C₃ and C₄. Assuming that a current I_{bias} is entering through the terminal C₁ and is exiting through C₃, the zero current in C₂ and C₄ reflects a zero magnetic field situation. When a magnetic field B_{X_2} is present along x_2 -direction i.e. parallel to the surface, as shown in Fig. 1(b), the current flow paths are altered and a differential current, I_{Hall} , appears at the two output terminals C₂ and C₄. I_{Hall} , B_{X_2} and I_{bias} give a measure of the sensitivity of the Hall devices as:

$$S_I = \left| \frac{I_{Hall}}{I_{bias} \times B_{X_2}} \right| \quad (1)$$

Geometric parameters such as the shape and size of *n*-wells, *n*+, and *p*+ diffusions, the distance between contacts and between contacts and device edges may also influence the device performance. For example, the Hall current, I_{Hall} , (and hence the sensitivity) is inversely proportional to the *n*-well doping concentration and therefore *n*-wells with small width are typically used in VHSs. To understand the effect of

geometry on device performance, VHSs with four geometries are considered in this work. These four versions, namely *basic*, *small-distance*, *small-width*, and *deep n-well*, are given in Table II and explained in following Sections.

B. VHS mode of operation

The VHSs reported in the literature are typically operated in voltage-mode, as shown in Fig. 1(c) [12], [21]. However, they can also be operated in the current-mode, as depicted in Fig. 1(d) [22], [23]. In fact, as explained below, the Hall sensor in current-mode exhibits better sensitivity and therefore the current-mode is preferred in this work. But, for the sake of comparison with Hall sensors reported in the literature, the performance of VHSs has also been evaluated in the voltage-mode.

In voltage-mode (Fig. 1(c)), the terminal C₁ is connected to the bias voltage, V_{bias} , and C₃ is grounded. The remaining two terminals, i.e. C₂ and C₄, give the output voltages V_{Hn} and V_{Hp} . When an external magnetic field is applied, the Lorentz force on the carriers leads to shortening and lengthening of current paths in C₄ and C₂, respectively. Due to the symmetry of the structure, the voltage at the output terminal is in the middle of both C₂ and C₄ (V_{Hn} and V_{Hp}) [24] and, therefore, the shortening/lengthening of the current paths is represented in terms of resistance variations. The equivalent resistances between the pairs of four terminals, $(R_0 - \Delta R_V)$, $(R_0 + \Delta R_V)$ on the top section and $(R_0 + \Delta R_V)$, $(R_0 - \Delta R_V)$ in the bottom section, are shown in Fig. 1(c). R_0 is the initial resistance between the nodes in each section when the magnetic field is zero and ΔR_V is the resistance variation in the presence of a magnetic field. The resistance of interconnections is assumed

negligible. With these values, the differential Hall voltage ($V_{Hp} - V_{Hn}$) is can be expressed as:

$$V_{Hv} = V_{bias} \frac{\Delta R_V}{R_0} \quad (2)$$

In current-mode (Fig. 1(d)), the output terminals C_2 and C_4 are connected to the common mode voltage, V_{CM} . The bias current, I_{bias} , flows in and out of the terminals C_1 and C_3 , respectively. In this case, the differential Hall current, I_{H_I} , can be calculated as:

$$I_{H_I} = 2I_{bias} \frac{\Delta R_I}{R_0} \quad (3)$$

where ΔR_I is the resistance variation with respect to R_0 when a magnetic field is present. From (2) and (3), it can be noted that, for an equal variation in the resistance (i.e. for $\Delta R_V = \Delta R_I$), the sensitivity in current-mode is twice the one achieved in voltage-mode and that is why the current-mode of operation is preferred in this work.

C. CMOS Hall sensors on flexible substrate

In applications such as wearable systems, the sensors often need to conform to the curved surface, which calls for their integration on flexible substrates. The integration of planar chips on flexible substrates comes with new set of challenges. For example, besides bonding of chips on flexible substrates, any deformation or bending can lead to mechanical stress induced performance variations. In the case of VHSs, the mechanical stresses lead to piezo-Hall effect, which can change the magnetic sensitivity [25]. This means that the Hall effect sensor can be used to detect magnetic field as well as the mechanical bending. However, this capability to detect multiple parameters also means that it is difficult to measure the desired parameter when multiple stimuli are simultaneously present. Therefore, the piezoresistive effect must be compensated or accounted for to accurately measure the magnetic field strength when the sensor is mechanically deformed [26], [27].

Assuming the plane-stress (i.e. $\sigma_{33} \cong 0$) the sensitivity variation with mechanical stress can be expressed as [28]:

$$S_I(\sigma, V, T) = S_I(V, T) \cdot [1 + P_{12} \cdot (|\sigma_{11}| + |\sigma_{22}|)] \quad (4)$$

where P_{12} is the piezo-Hall coefficient in (x_1, x_2) -plane ($P_{12} = 40 \times 10^{-11} \text{ Pa}^{-1}$ for a n -well with $n=4 \times 10^{16} \text{ cm}^{-3}$ [25]), and σ_{11} and σ_{22} are the in-plane stress σ components along [100] and [010] axes, respectively (see Fig. 2(e)). In absence of external magnetic field and mechanical stress, all the four resistors in Fig. 1(c) have the same initial value (R_0), which is calculated as

$$R_0 = (q \cdot \mu_n \cdot n \cdot H)^{-1} \quad (5)$$

and can be determined through two steps: (i) the node C_3 is grounded and a driving current is applied to the terminal C_1 ; (ii) the terminal C_1 is grounded and the current is applied to terminal C_3 . In (5) q is the electron charge and μ_n is the electron mobility for n -type doping. To account for the piezo-Hall and piezoresistance induced resistance variation, the value of each resistor can be expressed as:

$$R = R_0(1 \pm \beta|\mathbf{B}| \pm \Pi|\boldsymbol{\sigma}|) \quad (6)$$

TABLE II
GEOMETRY PARAMETERS OF THE FOUR 4F 3C VHSs.

VHS geometries	<i>basic</i>	<i>small-distance</i>	<i>small-width</i>	<i>deep n-well</i>
L_C [μm]	1.71	1.71	1.71	1.71
L_S [μm]	2.65	2.65	2.65	2.65
D_C [μm]	9	6	9	9
D_S [μm]	5	5	5	5
W [μm]	7.44	7.44	6.2	11.6
d [μm]	2	2	2	2

where β is the magnetic resistance coefficient, defined as the average of initial values of resistors R_0 in presence and absence of magnetic field (\mathbf{B}), and Π is the general piezoresistive coefficient for (001) Si-plane [29]. Π can be expressed as a function of fundamental Si piezoresistive coefficients ($\Pi_{11}, \Pi_{12}, \Pi_{44}$) and angles θ and φ as [26]:

$$\begin{aligned} \Pi(\theta, \varphi) = & \Pi_{11} \cdot (\cos^2 \theta \cdot \cos^2 \varphi + \sin^2 \theta \cdot \sin^2 \varphi) \\ & + \Pi_{12} \cdot (\cos^2 \theta \cdot \sin^2 \varphi + \sin^2 \theta \cdot \cos^2 \varphi) \\ & + 2 \cdot \Pi_{44} \cdot \sin \theta \cdot \cos \theta \cdot \sin \varphi \cdot \cos \varphi \quad (7) \end{aligned}$$

For resistors oriented at $\theta = 45^\circ/135^\circ$ and uniaxial stress applied at $\varphi = 0^\circ/180^\circ$, (7) becomes:

$$\Pi(45^\circ, 0^\circ) = \frac{\Pi_{11} + \Pi_{12}}{2} \quad (8)$$

The stress tensor $\boldsymbol{\sigma}$ is expressed as a function of its in-plane components as:

$$|\boldsymbol{\sigma}| = \sqrt{|\sigma_{11}|^2 + |\sigma_{22}|^2} \quad (9)$$

The above expressions have been used to setup the COMSOL simulator and to describe in Verilog-A the eight-resistor VHS model (discussed shortly) simulated in Cadence. Simulation results are presented in the following Section IV.

III. SYSTEM ARCHITECTURE

As mentioned in Section II-A, four versions of VHSs have been implemented on a single test chip. They are selectable through a multiplexer and dedicated switches, as shown in Fig. 1(e). Terminals $C_1 \sim C_4$ are connected to each sensor depending on the value of the two digital inputs, S_0 and S_1 .

A. VHSs implementation

The four variants of VHS presented here were designed and fabricated in a 0.18- μm CMOS technology. The design parameters (Fig. 1(b)) include L_C , L_S , D_C , D_S , W and d , which stand for centre contact length, side contact length, distance between centre and side contact, distance side contact from border of sensor, width and distance between the folds, respectively. The centre contacts are used for biasing and measurements while the side contacts connect the four folds of the device. The values of L_C , L_S , D_C , D_S , W and d used for the four realisations (namely, *basic*, *small-distance*, *small-width*, and *deep n-well*) are summarised in Table II. The *basic* sensor integrated on the chip acts as a reference. The *small-distance*

and *small-width* sensors are scaled version of the *basic* device. The distance centre contact from side contact (D_C) and sensor width (W) have been modified, respectively. In the *deep n-well* sensor, the *n-well* active region has been replaced with a deep *n-well*.

B. Offset Reduction

A possible offset, which could occur due to mask misalignment during fabrication or mechanical stresses, can be reduced significantly by using the current spinning technique [30]. However, for voltage-mode driven Hall sensors, even after the current spinning operation, a small residual offset is still possible because of the junction field effect and the carrier velocity saturation, which may cause some non-linearity. This residual offset can be suppressed by the orthogonal coupling of four identical Hall sensors [17]. It may be noted that in the current mode, the voltage at the output terminals (common-mode voltage) remains constant. This means that the parasitic capacitances have little or no influence and, accordingly, the sensors show better linearity. This enables the current spinning technique to completely cancel any offset. A well laid out geometry of the Hall device can greatly decrease the offsets and improve the performance. For a 4F 3C VHS, the spinning circuitry design for two-phases operation has been reported in [31]. This design uses four phases, as shown in Fig. 1(f). The current spinning periodically interchanges the output and supply terminals of the VHS and allows rotation of the bias current injection and sink points in each state, while the offset appears at the output terminals. For instance, during Φ_1 of Fig. 1(f), the bias current, I_{bias} , is injected into the terminal C_1 and the same bias current is drawn from another non-adjacent terminal, C_3 . The two output currents, I_{Hp} and I_{Hn} , are available at the other two terminals. Their difference gives the Hall current, I_{Hall} . During Φ_2 , the injection and sink terminals are C_2 and C_4 , respectively, and C_1 and C_3 become the output terminals. At the end of the four phases, the offset is eliminated.

IV. SIMULATION AND MODELING

An eight-resistor Verilog-A compact model has been implemented to simulate the Hall sensor in Cadence environment together with the bias and the readout circuits. The model includes parameters to account for the sensor physical and mechanical properties estimated by means of FEM simulations. Accordingly, this Section presents the numerical results obtained by 3D simulations in COMSOL Multiphysics and compares them with those obtained in Cadence Spectre.

A. COMSOL simulations

A 3D model of the current-mode VHS, based on the *basic* geometry described in Table II, has been implemented and simulated in COMSOL Multiphysics. Fig. 2(a) shows the configuration of the model geometry and the total displacement surface of VHS with substrate bending radii of 10 mm, when a magnetic field of 5 mT is applied. It can be noted that the maximum sensor displacement is less than 7.83 μm . This

displacement changes the piezoresistivity of the sensor and appears as an offset at the output of the sensor.

To dynamically compensate for the offsets, mismatches due to substrate bending and possible masks misalignment during fabrication, the current-spinning technique has been used as described in Section III-B. The four configurations foreseen by the current-spinning technique (Fig. 1(f)) and the surface electrical distribution of the 4F 3C VHS with substrate bending are shown in Fig. 2(b). The applied magnetic field in this case is 5 mT. The simulation uses a nominal bias current of 10 μA . Fig. 2(c) shows the simulated current-mode sensitivity of the VHS when the magnetic field changes in the 0–5 mT range after the four current spinning phases and substrate bending radii in 10–25 mm range. The maximum differential output current (Hall current) is almost 4 nA for a magnetic field equal to 5 mT, as shown in the inset of Fig. 2(c). These current levels can be transformed into suitable voltages by integrating the current signal over a chosen period of time. A detailed description of the readout interface for magnetic sensors is given elsewhere [32]. Fig. 2(d) shows the simulated sensor output currents (Hall current) as a function of the magnetic field with 10 μA bias current after four current-spinning phases. In this case, the magnetic field varies from 0 to 5 mT with steps of 1 mT. The output offset of VHS due to substrate bending during these four phases can also be seen in Fig. 2(d).

B. Verilog-A model

The COMSOL simulation of magnetic sensors by considering physics, geometry and technological constraints is the important first step for a system design. However, it is difficult to include in COMSOL simulations the secondary effects such as the presence of noise effects, parasitic capacitances, and electronics non-idealities, [33]. In this regard, Cadence environment is better as it allows optimization of the electronic front-end by considering non-idealities and sensor versus electronics interference. From a system viewpoint, these secondary effects should be considered in sensor modelling for better analyses of the overall performance. This is also needed to prepare a custom tool for the analog circuit design. The Verilog-AMS, a derivative of Verilog hardware descriptive language, which includes analog and mixed signal extensions to describe the behaviour of devices, is used here for further analysis. Specifically, the Verilog-A, which is a continuous time subset of Verilog-AMS, has been used here.

The VHS is simplified into a series of eight resistors, as shown in Fig. 2(e). Each contact terminal has two resistors, one on the left (R_L) and another on the right (R_R). At zero magnetic field, all resistors have the same initial value (R_0). The Wheatstone bridge structure includes four electrical terminals (C_1 , C_2 , C_3 and C_4) and eight resistors (four R_L and four R_R). As per (6), the value of each resistor is a function of five parameters ($R_0, \beta, |\mathbf{B}|, |\sigma|, \Pi$). Furthermore, thanks to the device symmetry and to the fact that the sensor operates in current-mode, the effect of the junction field effect and of the carrier velocity saturation is considered negligible. Consequently, the PN junction effect is not included in this

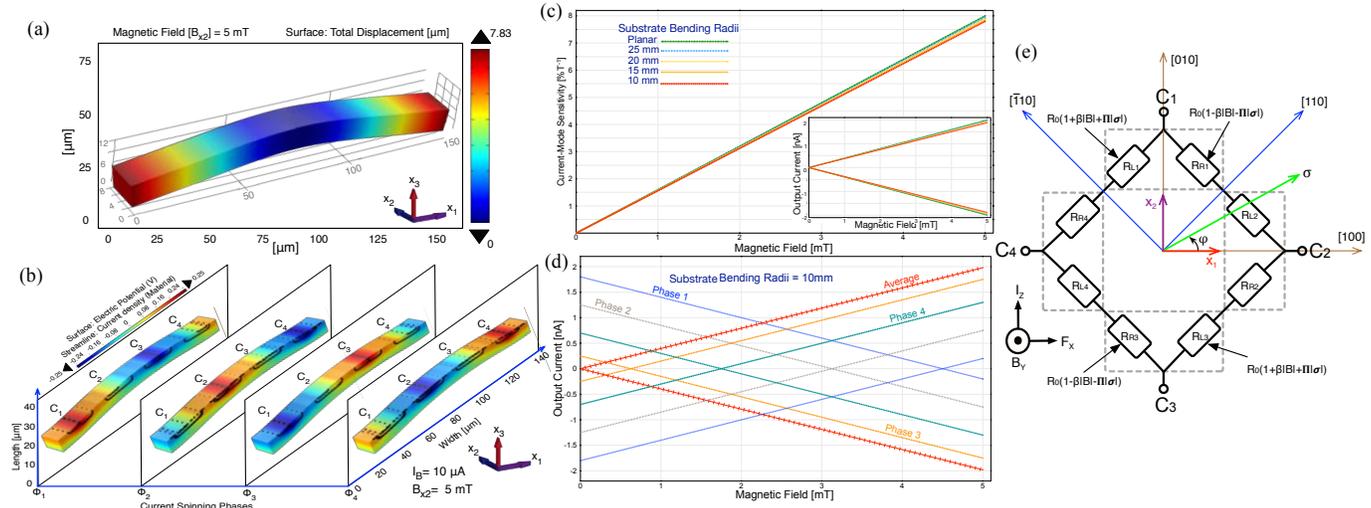


Fig. 2. Simulation of the 4F 3C VHS in COMSOL environment. (a) Surface total displacement of the VHS with substrate bending and 5-mT magnetic field. (b) Electric potential surface and current streamlines for the four current-spinning phases in current-mode. (c) Simulated current-mode sensitivity variation upon substrate bending. Inset: variation of the Hall current as a function of the magnetic field for defined substrate bending curvatures. (d) Simulated sensor output currents (Hall currents) as a function of the magnetic field with 10 μA bias current after four phases. (e) The equivalent 8-resistor model implemented in Verilog-A using Wheatstone bridge depiction.

Verilog-A 8-resistors model.

The simulations were performed in Cadence using 10 μA input bias current and magnetic field in 0 to 5 mT range. To evaluate the accuracy of Verilog-A model, the simulation results have been compared with those obtained using COMSOL model for the *basic* VHS geometry. The Hall current can be obtained from differential current outputs at 5 mT as:

$$I_{Hall} = I_{Hp} - I_{Hn} \quad (10)$$

For a 5-mT magnetic field, the simulated I_{Hall} values in COMSOL and Cadence are 4.20084 nA and 4.20036 nA, respectively. These values are in excellent agreement. Using (1), the sensor sensitivity at a bias current of 10 μA is 8.4 [% T^{-1}]. This value is better than the range of sensitivity i.e. 1.5 – 4.3 [% T^{-1}] [14] reported in the literature for other VHSs [15], [16], [21].

V. MEASUREMENT RESULTS

The experimental results of the four different VHSs are discussed in this Section. First the design of the testing board and measurement setup are explained and then the measurement results are described. The prototype of the multi 4F 3C VHS was fabricated in a standard 0.18- μm CMOS technology. Fig. 3(a) shows the microphotograph of the chip with pads. The four sensors (*basic*, *small-distance*, *small-width* and *deep n-well*) and the multiplexer block are magnified. The whole chip occupies an area of 788 \times 740 μm^2 .

The prototype has 10 pins connected directly to the printed circuit board (PCB). Custom PCBs designed to test the prototype include a motherboard and a baby board. Fig. 3(b) shows the fabricated board with soldered components to test the prototypes in planar state. To prevent interference between the digital and analog parts, the motherboard uses two different power supplies, VDD and DVDD. These voltages are provided to the chip by means of two voltage regulators (LM4120)

on the PCB. The PCB top and bottom plates are connected to VDD and to GND, respectively. The inject and drain bias current sources were provided by means of two current generators (LM234) on the motherboard. Two toggle switches are used as selectors. The main parts of the designed board e.g. current generators, voltage regulators and selectors have been highlighted in Fig. 3(b). The baby board uses a 80-pin socket (10 pins are connected to the chip) to hold the chip and for fast replacement of other samples during measurement. To generate a wide range of magnetic field, a Helmholtz coil with dimensions of 20 \times 36 \times 38 cm^3 is also used.

The measurements were performed in voltage and current modes, as shown in Fig. 3(c)-(d). In voltage-mode the sensor was biased by a current generator. The Hall voltage ($V_{Hall} = V_{Hp} - V_{Hn}$) was obtained from the voltages V_{Hp} and V_{Hn} , which appear at the two terminals shown in Fig. 3(c) when the external magnetic field is present. Fig. 3(d) shows the current-mode bias configuration of the sensor. For this measurement, two current generators (LM234) are used for obtaining the bias currents. Two off-chip low offset operational amplifiers (LF412) were used to fix the constant voltages V_{CM} at the output terminals.

For reliable operation of the sensor on flexible substrates, it is essential to examine the effect of bending on the failure limits of bonds with interconnects. In this regard, the limits of mechanical failure of VHS chip samples were investigated via experimental bending analysis. The experimental analysis was supported with the theoretical analysis using a finite element method, which was implemented in COMSOL and Verilog-A. For this purpose, the VHS chips were mounted and wire bonded on a 150- μm -thick double layer polyimide based flexible printed circuit (FPC) board. In fact, the sensors chip was also mounted on different flexible substrates i.e. a poly(vinyl chloride-co-vinyl acetate-co-maleic acid) (PVC), as shown in Fig. 1(a). Toward bending analysis of the chip on

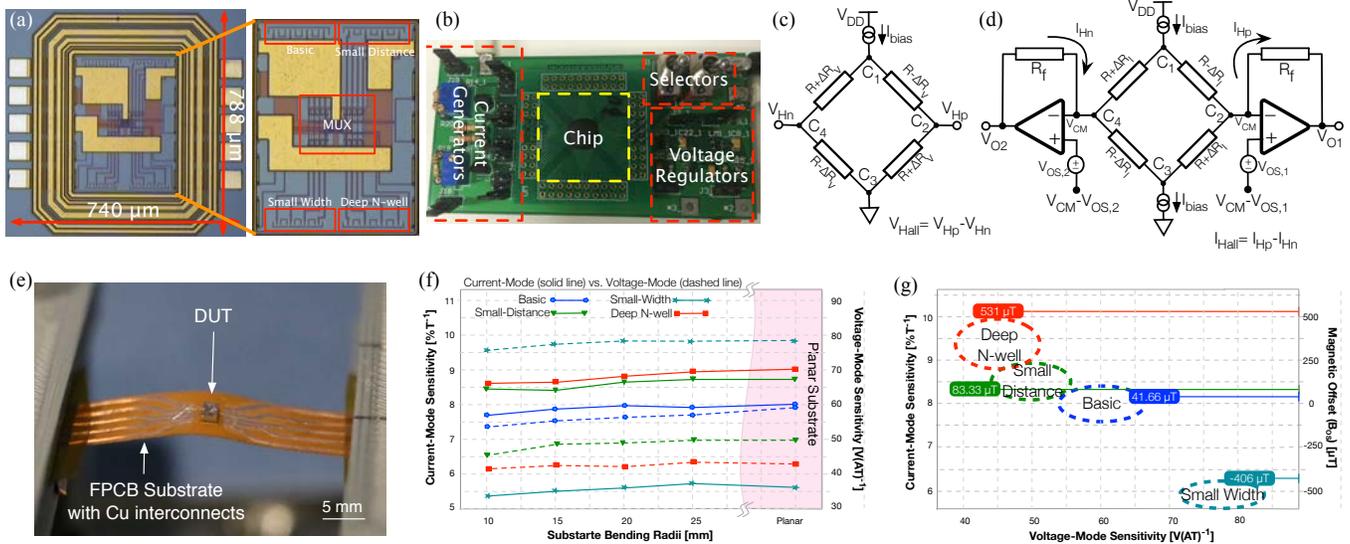


Fig. 3. (a) Chip microphotograph and magnified chip core showing the sensors placement. (b) Fabricated test board with components soldered for measurements in planar state. (c) Configuration of the tested chip in voltage-mode and (d) in current-mode. (e) Chip under test mounted on 150- μm -thick flexible polyimide-based FPC. (f) Measured sensitivity of each VHS as a function of bias current in both current and voltage modes. (g) Comparison of four different VHS geometries in terms of current-mode sensitivity, voltage-mode sensitivity and magnetic field equivalent offset (B_{OS}) with annotated average measured offset.

flexible substrate, the samples were fixed on clamps attached to a micrometer positioning system having movable ends. The substrate undergoes bending when the movable ends are slowly moved towards each other, simultaneously, as shown in Fig. 3(e). Fig. 3(f) shows the current-mode and voltage-mode sensitivities versus substrate bending for different VHSs. A magnetic field of 5 mT was used with substrate bending radii ranging from 10 mm to 25 mm, in steps of 5 mm. The solid lines illustrate the sensitivity of the current-mode configuration, whereas the dashed lines show the one of the voltage-mode configuration. The measurement results for the *basic* VHS show that the performance worsens by 5% when compared to the values achieved by COMSOL simulations in terms of Hall current and current-mode sensitivity.

Table III summarizes the measured performance of the four different VHSs. From the measurement results, it is clear that the offset and sensitivity vary with geometry. The information for the current-mode and voltage-mode sensitivities are altered by changing the distance between contact terminals (D_C) and *n*-well width (W). To get a better voltage-mode sensitivity, the sensor width can be decreased. The *small-width* sensor device has the best voltage-mode sensitivity. In current-mode, the sensitivity can be improved by decreasing the contacts distances, and, with deeper *n*-well diffusion, this value will be ameliorated. The *deep n-well* and *small-distance* sensor devices prove to have the best performance in terms of current-mode sensitivity.

The residual offset, as per the current spinning technique described in Section III-B, can be calculated as:

$$V_{OS,T} = \frac{V_{OS,\Phi_1} + V_{OS,\Phi_2} + V_{OS,\Phi_3} + V_{OS,\Phi_4}}{4} \quad (11)$$

where $V_{OS,\Phi_{1,2,3,4}}$ are the voltage offsets of the four current spinning phases. The magnetic field equivalent offset is defined

as:

$$B_{OS} = \frac{V_{OS,T}}{S_A} \quad (12)$$

where S_A is the absolute sensor sensitivity, which is obtained by dividing the Hall voltage by the magnetic field ($S_A = I_{Hall}/B [A(T)^{-1}]$). The offset measurements were performed in the absence of magnetic field after four phases of current spinning and have been evaluated at room temperature. The magnetic field for calculation of Hall voltage and absolute sensitivity is considered equal to 5 mT. Fig. 3(g) compares experimental results of the VHS devices in terms of current-mode and voltage-mode sensitivities and the magnetic equivalent offset (B_{OS}). The average measured offset values are also annotated for each VHS. Among the four versions of VHS, the *basic* device presents the lowest magnetic field equivalent offset, $41.66 \pm 8 \mu\text{T}$. The highest offset is related to the *deep n-well* device with more than 500 μT . The substrate for the VHSs was bent to a maximum radius of curvature of 10 mm. The results indicate degradation of performance by up to 2.5% due to piezoresistance effect on the sensors. A resolution (minimum detectable magnetic field) of 10 μT has been obtained for the *basic* device.

Table IV summarises the VHS performance for a bias current of 10 μA and also provides a comparison of *basic*

TABLE III
CHARACTERISATION AND COMPARISON OF FOUR VHSs

VHS	S_I [%/T]	S_V [V(AT) $^{-1}$]	$V_{OS,T}$ [μV]	B_{OS} [μT]
Basic	8 ± 0.1	59 ± 1	0.05 ± 0.01	41.66 ± 8
Small-Distance	8.7 ± 0.2	50 ± 1	0.075 ± 0.015	83.33 ± 17
Small-Width	5.6 ± 0.4	78 ± 2	0.65 ± 0.01	-406 ± 6
Deep N-well	9 ± 0.1	43 ± 1	0.425 ± 0.02	531 ± 15

TABLE IV
 SUMMARY OF THE PERFORMANCE OF SENSORS AND COMPARISON WITH RECENT
 WORKS ON MAGNETIC SENSORS ON FLEXIBLE SUBSTRATES

Reference	[6]	[9]	[10]	This Work
Year of Publication	2014	2015	2015	2016
Sensor Type	Hall	GMR	OFET	Hall
Functional Material	Cr/Bi	Co/Cu	AgNWs	CMOS
Substrate Material	Polyimide	PVC	PDMS	FPC
Sensitivity [T^{-1}]	N/A	0.93	115.2%	8%
Sensitivity [$V(AT)^{-1}$]	2.3	N/A	N/A	59
Residual Offset	N/A	N/A	N/A	41.66 μ T
Sensor Bias	50 mA	100 μ A	60 V	10 μ A
Power Consumption	N/A	N/A	N/A	1 μ W

geometry device in this work with other recently published non-CMOS technology based flexible magnetic sensors.

VI. CONCLUSION

A magnetic sensors chip having four different VHSs and mounted on flexible substrates is presented in this work. The chip has been fabricated in a standard 0.18- μ m CMOS process and mounted and wire bonded on two different polymeric substrates including PVC and polyimide-based FPC board. The optimal geometry of the Hall sensors on the chip has been investigated through simulations, which also consider the effect of mechanical stress on sensor performance. The results indicate degradation of performance by up to 2.5% when bending radius of curvature of the substrate changes from 10 to 25 mm. The measurement results from more than 10 prototypes show that the *basic* VHS achieves a sensitivity of more than 8 % T^{-1} over magnetic field range of 0-5 mT. The power consumption is in the range of μ W. The use of the symmetric 4F 3C VHS and a current-mode approach allow offset cancellation with the current spinning technique.

Future work will involve thinning down the chip to 20 μ m and integrating the sensor with a readout circuit in a single chip to increase the magnetic sensitivity. With integration of ultra-thin CMOS Hall sensors on a polymeric substrate, these sensors could find an attractive application in electronic skin and wearable electronics.

REFERENCES

- [1] D. Hall, R. S. Gaster, K. Makinwa, S. X. Wang, and B. Murmann, "A 256 Pixel Magnetoresistive Biosensor Microarray in 0.18 μ m CMOS," *IEEE J. of Solid-State Circuits*, vol. 48, no. 5, pp. 1290–1301, 2013.
- [2] A. Ajbl, M. Pastre, and M. Kayal, "A fully integrated Hall sensor microsystem for contactless current measurement," *IEEE Sensors J.*, vol. 13, no. 6, pp. 2271–2278, 2013.
- [3] C. Schott, R. Racz, A. Manco, and N. Simonne, "CMOS single-chip electronic compass with microcontroller," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2923–2933, 2007.
- [4] I. J. Monch *et al.*, "Flexible Hall Sensorics for Flux Based Control of Magnetic Levitation," *IEEE Trans. Magnetism*, vol. PP, no. 99, pp. 1–4, 2015.
- [5] H. Heidari, N. Wacker, S. Roy, and R. Dahiya, "Towards Bendable CMOS Magnetic Sensors," in *IEEE Conf. Ph.D. Res. Microelectr. and Electron. (PRIME)*, 2015.
- [6] M. Melzer *et al.*, "Wearable Magnetic Field Sensors for Flexible Electronics," *Advanced Materials*, vol. 27, no. 7, pp. 1274–1280, 2015.

- [7] M. Melzer *et al.*, "Imperceptible Magnetolectronics," *Nature communication*, vol. 6, 2015.
- [8] M. Melzer *et al.*, "Direct Transfer of Magnetic Sensor Devices to Elastomeric Supports for Stretchable Electronics," *Advanced Materials*, vol. 27, no. 8, pp. 1333–1338, 2015.
- [9] D. Karnaushenko and *et al.*, "High-Performance Magnetic Sensorics for Printable and Flexible Electronics," *Advanced Materials*, vol. 27, no. 5, pp. 880–885, 2015.
- [10] Y. Zang, F. Zhang, D. Huang, C.-a. Di, and D. Zhu, "Sensitive Flexible Magnetic Sensors using Organic Transistors with Magnetic-Functionalized Suspended Gate Electrodes," *Advanced Materials*, vol. 27, no. 48, pp. 7979–7985, 2015.
- [11] N. Wacker, H. Richter, T. Hoang, M. Schlze, E. Angelopoulos, M. Hassan, and J. Burghartz, "Stress Analysis of Ultra-Thin Silicon Chip-on-Foil Electronic Assembly Under Bending," *Semiconductor Sc. and Tech.*, vol. 29, no. 9, pp. 1–12, 2014.
- [12] M. BANJEVIĆ, "High Bandwidth CMOS Magnetic Sensors Based on the Miniaturized Circular Vertical Hall Device," Ph.D. dissertation, EPFL, 2011.
- [13] T. Kaufmann, M. Vecchi, P. Ruther, and O. Paul, "A Computationally Efficient Numerical Model of the Offset of CMOS-integrated Vertical Hall Devices," *Sens. and Actuat. A: Physical*, vol. 178, pp. 1–9, 2012.
- [14] O. Paul, R. Raz, and T. Kaufmann, "Analysis of the offset of semiconductor vertical Hall devices," *Sensors and Actuators A: Physical*, vol. 174, pp. 24–32, 2012.
- [15] G.-M. Sung and C.-P. Yu, "2-D differential folded vertical Hall device fabricated on a p-type substrate using CMOS technology," *IEEE Sensors J.*, vol. 13, no. 6, pp. 2253–2262, 2013.
- [16] C. Sander, R. Raz, P. Ruther, O. Paul, T. Kaufmann, M. Cornils, and M. Vecchi, "Fully Symmetric Vertical Hall Devices in CMOS Technology," in *IEEE Sensors Conf.*, 2013, pp. 1–4.
- [17] C. Sander, M.-C. Vecchi, M. Cornils, and O. Paul, "From Three-Contact Vertical Hall Elements to Symmetrized Vertical Hall Sensors with Low Offset," *Sensors and Actuators A: Physical*, vol. 240, pp. 92–102, 2016.
- [18] H. Heidari, E. Bonizzoni, U. Gatti, F. Maloberti, and R. Dahiya, "Optimal Geometry of CMOS Voltage-Mode and Current-Mode Vertical Magnetic Hall Sensors," in *IEEE Sensors Conference*, 2015, pp. 1–4.
- [19] R. Dahiya and S. Gennaro, "Bendable Ultra-Thin Chips on Flexible Foils," *IEEE Sensors J.*, vol. 13, no. 10, pp. 4030–4037, 2013.
- [20] S. Khan, L. Lorenzelli, and R. S. Dahiya, "Technologies for Printing Sensors and Electronics over Large Flexible Substrates: A Review," *IEEE Sensors J.*, vol. 15, no. 6, pp. 3164–3185, 2015.
- [21] E. Schurig, "Highly Sensitive Vertical Hall Sensors in CMOS technology," Ph.D. dissertation, EPFL, 2005.
- [22] H. Heidari, U. Gatti, E. Bonizzoni, and F. Maloberti, "Low-Noise Low-Offset Current-Mode Hall Sensors," in *9th IEEE Conf. Ph.D. Res. Microelectr. and Electron. (PRIME)*, 2013, pp. 325–328.
- [23] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A Current-Mode CMOS Integrated Microsystem for Current Spinning Magnetic Hall Sensors," in *Int. Symp. on Circ. and Sys. (ISCAS)*, 2014, pp. 678–681.
- [24] H. Heidari, U. Gatti, and F. Maloberti, "Sensitivity Characteristics of Horizontal and Vertical Hall Sensors in the Voltage- and Current-Mode," in *IEEE Conf. Ph.D. Res. Micro. and Elec. (PRIME)*, 2015, pp. 330–333.
- [25] B. Hag, "Piezo-Hall coefficients of n-type silicon," *J. Appl. Phys.*, vol. 64, no. 1, pp. 276–282, 1988.
- [26] C. S. Smith, "Piezoresistance Effect in Germanium and Silicon," *Phys. Rev.*, vol. 94, no. 1, p. 42, 1954.
- [27] M. Paun, J. Sallase, and M. Kayal, "Hall Effect Sensors Design, Integration and Behavior Analysis," *J. Sensor and Actuator Networks*, vol. 2, no. 1, pp. 85–97, 2013.
- [28] J. Gere and S. Timoshenko, "Mechanics of materials brooks," *Cole, Pacific Grove, CA*, pp. 815–39, 2001.
- [29] N. Wacker, H. Richter, M. Hassan, H. Rempp, and J. N. Burghartz, "Compact modeling of CMOS transistors under variable uniaxial stress," *Solid-State Electronics*, vol. 57, no. 1, pp. 52–60, 2011.
- [30] P. Munter, "A Low-Offset Spinning-Current Hall Plate," *Sensors and Actuators A: Physical*, vol. 22, no. 1, pp. 743–746, 1990.
- [31] K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, and R. P. Martins, "A handheld 50pM-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2016, pp. 474–475.
- [32] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS Current-Mode Magnetic Hall Sensor With Integrated Front-End," *IEEE Trans. Circ. and Syst. I: Regular Papers*, vol. 62, no. 5, pp. 1270–1278, 2015.
- [33] C. Buffa, "Design of MEMS magnetic field sensors and readout electronics," Ph.D. dissertation, Politecnico di Milano, 2013.



Hadi Heidari received BSEE and MSEE degrees in 2005 and 2008, respectively. He subsequently completed his Ph.D. in Microelectronics at the University of Pavia, Italy in 2015, where he worked on Integrated CMOS Sensor Microsystems. In past, he worked at Hamrah-e-Avval (Mobile Telecommunication Company of Iran) and Azad University, Iran. Presently, he is a Postdoctoral Research Assistant at the Electronics and Nanoscale Engineering division of the University of Glasgow, UK. He served on the local organizing committee for the IEEE PRIME

2015 conference, organizer of a special session on the IEEE ISCAS 2016 conference and social media chair of the IEEE Sensors 2016 conference. He is a member of IEEE, Circuits and Systems Society (CASS), and a committee member of IEEE Sensors Council UKRI Chapter. He has authored or co-authored over 30 peer-reviewed publications in international journals or conference proceedings and acts as a reviewer for several journals and conferences. He received honorary mention paper award at the IEEE ISCAS 2014 and gold leaf award at IEEE PRIME 2014 conferences. He was Visiting Scholar at the University of Macau, China, and McGill University, Canada.



Edoardo Bonizzoni was born in Pavia, Italy, in 1977. He received the Laurea degree (summa cum laude) in Electronic Engineering from the University of Pavia, Italy, in 2002. From the same University, he received in 2006 the Ph.D. degree in Electronic, Computer, and Electrical engineering. In 2002 he joined the Integrated Microsystems Laboratory of the University of Pavia as a Ph.D. candidate. During his Ph.D., he worked on development, design and testing of non-volatile memories with particular regard to phase-change memories. From 2006 his

research interests are mainly focused on the design and testing of DC-DC and A/D converters. In this period he worked on single-inductor multiple-output DC-DC buck regulator solutions and on both Nyquist-rate and oversampled A/D converters. Recently, his research focuses on the design of high precision amplifiers and ultra-low voltage reference circuits as well. Presently, he is a Senior Assistant Professor at the Department of Electrical, Computer, and Biomedical Engineering of the University of Pavia. Dr. Bonizzoni has authored or co-authored more than 90 papers in international journals or conferences (with published proceedings) and two book chapters. He is co-recipient of the IEEE ISCAS 2014 Honorary Mention Paper Award of the Sensory Systems Track, of the IEEE/IEEJ Analog VLSI Workshop (AVLSIWS) 2010 best paper award, of the IEEE European Solid-State Circuits Conference (ESSCIRC) 2007 best paper award and of the IEEE/IEEJ Analog VLSI Workshop (AVLSIWS) 2007 best paper award. From 2011 to 2015 he served the IEEE Circuits and Systems Society as an Associate Editor of the IEEE Transactions on Circuits and Systems - Part. II and, since 2016, he is an Associate Editor of the IEEE Transactions on Circuits and Systems - Part. I.



Umberto Gatti received the Laurea degree (summa cum laude) in Electronic Engineering and the Ph.D. in Electronics and Information Engineering from the University of Pavia, Italy, in 1987 and 1992, respectively. From 1993 to 1999, he worked in the Central RD Lab of Italtel, Italy, and then in the RD Lab of Siemens, Italy, as Sr. ASIC Engineer. Besides developing analog and mixed analog-digital CMOS/BiCMOS ICs for telecom (data converters, base-band wireless transceivers, burst mode PON interfaces), he was the coordinator of funded projects

under the frameworks of FP and Eureka, focused on high-speed Nyquist rate and sigma-delta converters. In 2007 he joined Nokia Siemens Networks, Italy, where he was a Sr. Power Supply Architect for telecom equipment (both at rack and boards level). Currently he is member of the Executive Staff of RedCat Devices, Italy, and also holds cooperation with the University of Pavia. His present research interests are in the area of CMOS mixed-signal ICs, in particular in rad-hard digital libraries and SRAMs, data converters, power management and testing techniques under irradiations. He holds 2 international patents, is co-author of more than 60 papers and co-recipient of the IEEE ISCAS 2014 honorary mention paper award of the Sensory Systems Track. He is IEEE member since 1991.



Franco Maloberti received the Laurea degree in physics (summa cum laude) from the University of Parma, Parma, Italy, in 1968, and the Doctorate Honoris Causa in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996. He was a Visiting Professor at The Swiss Federal Institute of Technology (ETH-PEL), Zurich, Switzerland and at the EPFL, Lausanne, Switzerland. He was the TI/J.Kilby Chair Professor at the AM University, Texas and the Distinguished Microelectronic Chair Professor at the University of

Texas at Dallas. Presently he is Professor of Microelectronics and Head of the Micro Integrated Systems Group, University of Pavia, Italy. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications, mainly in the areas of switched-capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A/D design. He has written more than 500 published papers on journals or conference proceedings, four books, and holds 30 patents. Dr. Maloberti was the recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production, in 1992. He was co-recipient of the 1996 Institute of Electrical Engineers Fleming Premium, the best Paper award, ESSCIRC-2007, and the best paper award, IEEJ Analog Workshop-2007 and 2010. He was the President of the IEEE Sensor Council from 2002 to 2003 and Vice-President, Region 8, of the IEEE CAS Society from 1995 to 1997 and an Associate Editor of IEEE TCAS-II. He was serving as VP-Publications of the IEEE CAS Society 2007-2008. He was distinguished lecturer of the IEEE Solid State Circuits Society 2009-2010 and distinguished lecturer of the Circuits and Systems Society 2012-2013. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the 2000 IEEE Millennium Medal. He received the IEEE CAS Society 2013 Mac Van Valkenburg Award. He is an IEEE life Fellow. In 2009 he received the title of Honorary Professor of the University of Macau and he is currently the chairman of the Academic Committee of the Microelectronics Key-Lab of Macau. He is President of the IEEE Circuits and Systems Society.



Ravinder Dahiya is Reader and EPSRC Fellow in the School of Engineering at University of Glasgow, UK. He is the Director of Electronics Design Centre at University of Glasgow. He graduated in Electrical Engineering from Indian Institute of Technology Delhi, India in 2001 and completed Ph.D. at Italian Institute of Technology, Genoa (Italy) in 2009. In past he worked at Delhi University (India), Italian Institute of Technology, Genoa (Italy), and Fondazione Bruno Kessler, Trento (Italy). He has held visiting positions at Universiti Teknologi Malaysia,

and University of Cambridge (UK). His multidisciplinary research interests include Flexible and Printable Electronics, Electronic Skin, Tactile Sensing, Robotics, and Wearable Electronics. His Bendable Electronics and Sensing Technologies (BEST) group conducts fundamental research on flexible and printable electronics using high-mobility materials. He has published more than 150 research articles, 6 books (including 5 at various stages of publication) and 9 patents (including 7 submitted). He has worked on and led many international projects funded by European Commission and EPSRC (Engineering and Physical Sciences Research Council). He is Distinguished Lecturer of IEEE Sensors Council (2016-2018) and senior member of IEEE. Currently he is serving on the Editorial Boards of IEEE Transactions on Robotics and IEEE Sensors Journal and has been guest editor of 4 Special Journal Issues (3 published in IEEE Journals). He represents the IEEE Robotics and Automation Society in the AdCom of IEEE Sensors Council. He is founding chair of the IEEE UKRI sensors council chapter. He was General Chair of IEEE PRIME 2015 and is the Technical Program Chair (TPC) of IEEE Sensors 2017 and TPC co-chair of IEEE Sensors 2018. He holds prestigious EPSRC Fellowship and received in past the Marie Curie Fellowship and Japanese Monbusho Fellowship. He was awarded with the University Gold Medal and received best paper awards 2 times and another 2 second best paper awards (where he was co-author) in the IEEE international conferences. He is also the recipient of the International Association of Advanced Materials Medal for the year 2016.