

# A Voltage-Time Model for Memristive Devices

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**Abstract**—A novel electrical model that describes the time evolution of oxide memristive devices is proposed. Starting from some considerations about the physical characteristics of the resistance change in the active layer of these devices, the traditional model based on a resistor series has been improved and extended, solving some limitations pending in the classical interpretation. The low complexity of the proposed model is very profitable for the resistive memory designers as it is easy to be integrated in the traditional design flows. Experimental results for HfO<sub>2</sub> devices implemented in a 250-nm BiCMOS process show an excellent match with the simulations achieved by using the proposed model and validate its effectiveness.

**Index Terms**—Memristor, resistive memories, oxide memories, electrical model.

## I. INTRODUCTION

IN 1971 Leon Chua in his famous article, [1], theorized the existence of a new passive two-terminal circuit element having as characteristic a function of the charge  $q$  and the flux-linkage  $\varphi = \int_{-\infty}^t v(\tau) d\tau$ . The existence of this novel element was hypothesized on the basis of the Maxwell's equations symmetry, but, at that time, no physical element with a  $f(\varphi, q) = 0$  characteristic had been discovered yet. A first physical memristor evidence was finally proved in 2008 by Hewlett Packard Labs, with the discovery of the non-volatile behavior of the TiO<sub>2</sub> films, [2].

Since then, the interest in these devices has suddenly arisen, mainly in the area of non-volatile memories (NVMs) as an alternative to Flash memories, the undisputed dominant solution for solid-state NVMs in the last decades. Many technological solutions have sprout in the last years. Among them, the resistive RAMs (ReRAMs), and in particular the transition-metal-oxides-based devices, achieved a good fortune attributed to their high CMOS back-end-of-line (BEOL) compatibility.

Memory applications need reliable analog device models in order to be effectively designed at the circuit and the transistor level. While many physical and chemical models attempting to describe the mechanisms involved at the molecular level in the memristive devices have been developed so far, the almost totality of the electrical models that have been proposed are based on the approach that Strukov presented in [2]. The successive contributions to the model, [3]–[6], have been mainly focused in improving the mathematical and numerical issues, keeping unchanged the physical idea originally introduced.

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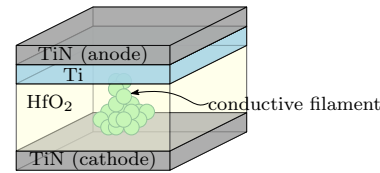


Fig. 1. Scheme of the MIM stack of the resistive device.

This paper proposes an electrical model that describes the time evolution of the device, extending the generality of the classical model.

Hafnium-Oxide-based 1-Transistor/1-Resistor (1T-1R) devices have been manufactured in a 250-nm BiCMOS technology and their experimental characterization data, in both *set* and *reset* operation, have been compared with the results achieved from simulations based on the proposed model. The obtained matching is excellent for both *set* and *reset*, thus successfully validating the electrical model.

The paper is organized as follows: in Section II the physical mechanisms involved in the resistance change of resistive devices are discussed. After a brief overview of the existing models discussed in Section III, Section IV presents the proposed electrical model. The implemented memory cell and the measurement results are then shown and discussed in Section V.

## II. RESISTANCE SWITCHING IN HFO<sub>2</sub> DEVICES

### A. Resistance Change Mechanism in Oxide ReRAMs

ReRAMs, also referred to as Oxide RAMs, are metal-insulator-metal (MIM) structures manufactured with a stack of a transition metal oxide layer sandwiched into two metal electrodes. Typically used oxides are TiO<sub>2</sub> or, more recently, HfO<sub>2</sub>, while Platinum and Titanium are the most employed metals due to their chemical compatibility with the red-ox process involved. A sketch of a HfO<sub>2</sub> device stack is illustrated in Fig. 1, [7].

The main physical mechanism leading to the resistance change is related to the formation and transport of oxygen vacancies inside the oxide: while the oxide shows an intrinsic insulator behavior, the defects introduced by oxygen vacancies create a conductive path in the compound.

At room temperature, the number of the oxygen vacancies and their mobility are too small to possibly allow any charge transport. However, under the action of an electric field, oxygen atoms migrate inside the stack (ionic migration) drifting toward the anode, piling up the vacancy defects. Since it is necessary to accumulate these oxygen ions so that the new crystalline structure modified by the defects has room and time to build up, at the anode, a Ti layer between the HfO<sub>2</sub>

and TiN is commonly used (Fig. 1), as titanium oxidation can accommodate oxygen ions without inhibiting the further vacancies motion.

### B. Electroforming, Set and Reset

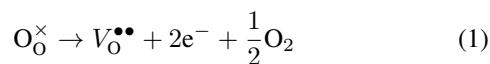
The Titanium acts as a scavenging layer for the oxygen ions and it is oxidized to  $TiO_{2-x}$  during an annealing step at 400 °C. Therefore, there is a strong gradient of oxygen vacancies in the  $HfO_2$  layer from the top electrode to the bottom electrode. A first step, commonly named *electroforming* (or simply *forming*), is necessary to create the first conductive filament (CF) and is quite critical, as it influences the dislocation of the vacancies defects inside the oxide. Many studies as [8] have been performed in order to understand how the voltage waveform applied in the forming steps can influence the CF evolution and the successive reliability.

After the constitution of the first CF, the successive conductive material buildups occur faster as the structure of the compound has been affected by the new location of the vacancies. The filament reconstitution is defined as *set* phase.

In bipolar resistive switching (BRS), when a reverse voltage is applied to the stack, it is possible to have the rupture of the CF. In the so called *reset* process, a reverse electric field moves the oxygen ions toward the filament where they oxidize the conductive Hf in  $HfO_2$  and disrupt the conductive path. However, the conductive behavior of the filament decreases the electric field intensity and the reset process slows down.

### C. Phases of the Conductive Filament Growth

As soon as a direct electric field is applied, oxygen ions migrate toward the anode with vacancies moving toward the cathode. At the cathode interface, in some localized points where interface defects lower the Schottky barrier, electrons flow into the oxide facilitating, in those regions, the creation of positive charged oxygen vacancies, according to the following red-ox reaction [9], [10]:



An initial cluster of vacancies starts growing with a quasi-isotropic initial expansion, as depicted in Fig. 2(a).

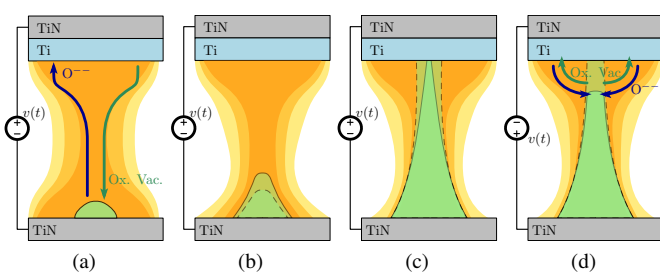


Fig. 2. Evolution of the CF. The oxygen dislocation follows the intensity of the electric field (as schematized in the pictures). In some areas, the injection of electrons establishes an early CF (a). As it grows, the electric field localizes where there is a higher current density, promoting the filament growth along one direction (b), until reaching the anode (c). The electric field intensity curvature has been intentionally emphasized. When a reverse bias is applied, the CF is worn out and decreases (d).

With the growth of the first vacancies, the electric field concentrates around the early-formed CF and the current density in that point increases, localizing in that region the red-ox reaction and forming a conductive wire as the process goes on – Fig. 2(b).

The filament grows along the device length until reaching the anode – Fig. 2(c). At this point, the red-ox reactions keep on going, widening the filament size and, consequently, decreasing its resistance value. The longer a direct voltage is applied, the lower is the final filament resistance value obtained, so that different Low Resistive States (LRSs) can be achieved.

In Fig. 2(d), the *reset* process is shown. Reciprocally to the *set* process, when an inverse electric field is applied, oxygen ions start to oxidize the CF that wears thinner and thinner until reaching a rupture. After the first rupture, the filament is consumed along the vertical direction, until reaching the High Resistive State (HRS) resistance.

## III. EXISTING MEMRISTOR MODELS

When the first concrete memristor device was presented, a simple linear approach for the I-V model was proposed by Strukov [2]. In this Section, a brief overview of that model and its improvements are discussed.

The basic assumption of the Strukov model considers the oxide layer resistance as a series of two contributions: the first associated to the intrinsic insulator layer, characterized by a high resistivity; the second related to the oxygen-vacancies-doped layer, characterized by a low resistivity. Fig. 3 conceptually depicts the model.

By defining  $R_u$  and  $R_d$  the resistances associated to the intrinsic part (un-doped) and to the doped one, respectively, the overall memristor resistance,  $R_M$ , is given by:

$$R_M(w) = R_d(w) + R_u(w) \quad (2)$$

where  $w$  is the thickness of the doped layer.

It is assumed that  $R_{off}$  is the value of the resistance associated to the pristine material ( $w = 0$ ) and, reciprocally,  $R_{on}$  is the resistance of the device fully formed ( $w = D$ , where  $D$  is the thickness of the oxide layer).

The memristance,  $R_M$ , can be rewritten as:

$$R_M(w) = R_{on} \frac{w}{D} + R_{off} \frac{D-w}{D} = R_{off} - \frac{\Delta R}{D} w \quad (3)$$

where  $\Delta R = R_{off} - R_{on}$ .

The voltage-time behavior of the device depends on the relations describing the memristive device:

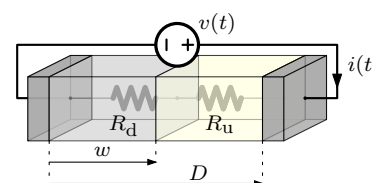


Fig. 3. Representation of the model proposed by Strukov, [2]. The global resistance is the series of the doped and undoped layers' resistances.

$$\begin{cases} v(t) = R_M(w, t)i(t) & (4.a) \\ \dot{w}(t) = f(w, i) & (4.b) \end{cases}$$

where the length  $w$  is the state variable of the dynamic system representing the memristor,  $v$  and  $i$  are the voltage across the memristor and the current flowing through it, respectively, while  $f(w, i)$  is a function describing the kinetics of the red-ox reaction leading to the filament growth. Different assumptions on (4.b) lead to either linear or non-linear models.

### A. The Linear Model

The linear model basically considers the growth of the doped layer directly proportional to the current flowing through the device:

$$\dot{w}(t) = K_I i(t) \quad (5)$$

Such hypothesis basically states that the speed of the red-ox that generates the oxide vacancies is proportional to the carriers fed by the current flow. Using this hypothesis, the system (4) becomes:

$$\begin{cases} R_M(w, t) = R_{\text{off}} - \frac{\Delta R}{D} w(t) & (6.a) \\ v(t) = R_M(w, t)i(t) & (6.b) \\ \dot{w}(t) = K_I i(t) & (6.c) \end{cases}$$

where the constant  $K_I$  accounts for physical and technological aspects, such as the oxygen-vacancies mobility and the oxide resistivity.

The solution of (6), assuming  $R_0 = R_M(0)$ , is:

$$R_M(t) = \sqrt{R_0^2 - 2K_I \frac{\Delta R}{D} \Delta\varphi(t)} \quad (7)$$

where  $\Delta\varphi(t)$  is the flux-linkage equal to  $\int_0^t v(\tau) d\tau$ , [3].

A further consideration, as it can be derived from (6.a) and (6.c), is that the resistance change for the linear model depends on the charge  $Q$  gathered (dispersed) during the *set* (*reset*) phase:

$$R_M(Q) = R_0 + R(Q) = R_0 - K_q Q \quad (8)$$

where  $K_q = -K_I \Delta R / D$  takes into account the technological aspects and  $R_0 = R_{\text{off}} - w(0) \Delta R / D$ .

Fig. 4 shows transients of the memristance during a *set* process for memristor devices driven with voltage double ramp sweeps of different duration and slope. As it can be seen, the resistance change depends on the area under the voltage curve: for a slope  $\Delta V / \Delta t$  equal to  $5 \text{ V s}^{-1}$ , the resistance change is minimal, while for a lower slope (and longer duration),  $\Delta V / \Delta t = 2.5 \text{ V s}^{-1}$ , the LRS is achieved during the decreasing phase of the voltage sweep. When  $\Delta V / \Delta t = 1.25 \text{ V s}^{-1}$ , the resistance change saturates during the rising slope.

Thanks to its low complexity, the above model can easily compute the memristive time behavior. However, the achievable accuracy is limited, as it can be noticed from Fig. 5: the simulated curve weakly matches the experimental time behavior of a 1T-1R  $\text{HfO}_2$  cell during the *set* process.

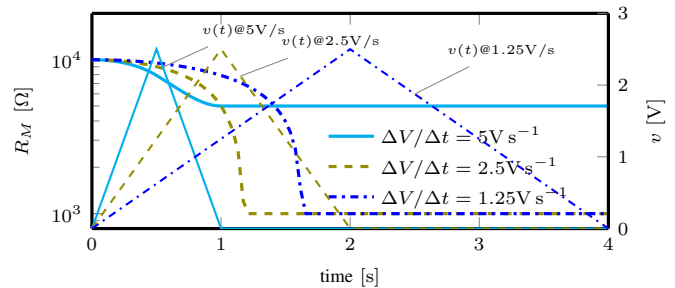


Fig. 4. Examples of resistance-time behavior for a linear memristor with  $R_M(0) = R_{\text{off}} = 10 \text{ k}\Omega$ ,  $R_{\text{on}} = 1 \text{ k}\Omega$  and  $K_I = 3 \times 10^{16} \text{ nm C}^{-1}$ . The voltage is applied by mean of double ramps with different slopes  $\pm \Delta V / \Delta t$ . The three situations, depicted for decreasing slopes, correspond, respectively, to: incomplete resistance switch, resistance switch in the falling slope, and resistance switch in the rising slope.

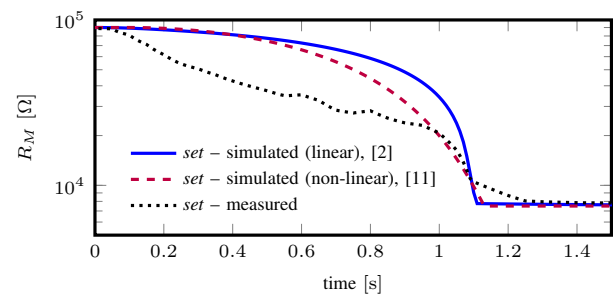


Fig. 5. Transient simulations of the memristance modeled with the linear, [2], and non-linear, [11], model compared with experimental data for a 1T-1R  $\text{HfO}_2$ . The description of the devices and the measurement setup will be discussed in Sections V-A and V-B, respectively.

### B. Non-Linear Models

The linear assumption of the Strukov model, [2], loses validity at the boundary states (HRS at  $w = 0$  and LRS at  $w = D$ ) where the discontinuities can determine issues for the numerical solvers. In the last years, various alternatives to the linear assumption, taking into account the non-linear nature of the dopant kinetics, have been presented, [3]–[6]. The common approach of these models is to weight the function  $f(w, i)$  with a *window* function,  $g(w)$ , of the state variable  $w$  so that:

$$f(w, i) = K_I g(w) i(t) \quad (9)$$

The complexity introduced by these models does not excessively affect the computational time. However, the simple addition of the window functions is not sufficient to obtain a suitable match with the real cell behavior, [12].

An improved modeling approach for  $\text{TiO}_2$  devices has been proposed by Pickett in [13], where the non-ohmic behavior of the undoped part of the device has been accounted for. Pickett's analysis considers the ohmic resistor of the doped region in series to an electron potential barrier and develops the Simmons' equations, [14], to achieve a solution for  $f(w, i)$ :

$$\dot{w} = \frac{f_{\text{on/off}} \sinh\left(\frac{i}{i_{\text{on/off}}}\right)}{\exp\left[\exp\left(\mp \frac{w - a_{\text{on/off}}}{w_c} - \frac{|i|}{b}\right) + \frac{w}{w_c}\right]} \quad (10)$$

with  $f_{on/off}$ ,  $i_{on/off}$ ,  $a_{on/off}$ ,  $b$  and  $w_c$  fitting parameters to be used, respectively, for *reset* and *set*.

Even if this model ensures a good match with measured I-V curves, the achievable time behavior of  $R_M$  is not very accurate, as the Pickett's model is affected by serious computational issues and convergence problems depending on the choice of the input signal [15], [16].

A group of modeling solutions presented in literature, [11], [17]–[19], considers empirical window functions and proposes a discrete algorithm each for the numerical solution. These models are highly technology-specific and, even if they ensure a good fitting, this is obtained at the cost of a high computational effort and limited generality. As an example, a very complex solution is proposed in [11], where the following a discrete window function is introduced to evaluate the memristance discrete increment:

$$\frac{\Delta R_M}{\Delta t} = f(R_M, v, t) = \frac{\mp C_x \left[ \frac{v(t) - V_t}{V_t} \right]^{P_x}}{1 + e^{\mp \frac{R_M(t) - \Theta_x R_x}{\beta_x (R_{off} - R_{on})}}} \quad (11)$$

where the fitting parameters  $V_t$ ,  $C_x$ ,  $P_x$ ,  $\Theta_x$  and  $\beta_x$  assume different values for *set* or *reset* and  $R_x$  is, respectively,  $R_{off}$  or  $R_{on}$ . The model fitting parameters have been set for the available 1T-1R HfO<sub>2</sub> devices. Fig. 5 shows the result for the *set* phase that, as it can be noticed, weakly matches the experimental results.

#### IV. PROPOSED SERIES/PARALLEL MODEL

The Strukov's two-resistors model schematized in Fig. 6(a) assumes an uniform growth of the conductive layer. On the contrary, as also proved by experimental evidences, [20], [21], the conductive volume is highly localized and has the form of a filament. Moreover, the dependance of the LRS value on the duration of the driving voltage, [22]–[24], and the memristive behavior during the *reset* phase, [25], suggest a dependency on the filament cross section. This aspect has also been pointed out by some works that have studied the quantic [26] or thermo-chemical [27] processes involved in the evolution of the conductive filament.

Thus, an electrical model that properly describes the physics of the device should replace the element  $R_0$  of the traditional series model with a more complex network capable to account for the physical transformations of the CF during the *set* and *reset* phases.

The proposed network is shown in Fig. 6(b). The contribution of the filament cross section is modeled by mean of a parallel of two conductances: a constant conductance,  $G_2$ , associated to the minimum filament section, and a second one  $G(Q)$ , variable, depending on the accumulated charge. When the device is a low resistive state,  $G(Q)$  is very small, but it becomes significant as the filament widens.

The overall resistance change process is, hence, equivalent to the sum of two contributions: a resistance,  $R_s$  (filament lengthwise growth), plus a parallel of conductances,  $R_p$  (filament widening), compared with the traditional series model in Fig. 6(a).

Similarly to what expressed in (8), the global memristance can be expressed as a function of the net charge,  $Q$ , accumulated (subtracted) during the red-ox processes. According to the scheme in Fig. 6(b), the memristance can be written as:

$$R_M(Q) = R_s(Q) + R_p(Q) \quad (12)$$

where:

$$\begin{cases} R_s(Q) = R_1 + R_2(Q) \\ R_p(Q) = \frac{1}{G_2 + G(Q)} \end{cases} \quad (13)$$

The sum of the terms  $R_1$  and  $R_2 = \frac{1}{G_2}$  represents the initial memristance value  $R_M(0) = R_{off} = R_1 + R_2$ , associated to the HRS.

If the linear hypothesis is maintained, the terms in (13) are linearly depending on the charge  $Q$ :

$$R_M(t) = R_1 - K_1 Q(t) + \frac{1}{G_2 + K_2 Q(t)} \quad (14)$$

where  $K_1$  and  $K_2$  are constants depending on the oxide technological and physical parameters such as temperature, mobility, resistivity, and thickness of the insulator layer. The signs chosen for the addends are such that for a positive charge (accumulated), a memristance decrease is achieved.

By differentiating (14), a dependency on the current  $i$  flowing through the memristor is obtained:

$$\dot{R}_M(t) = \dot{R}_s(t) + \dot{R}_p(t) = -K_1 i(t) - K_2 R_p^2(t) i(t) \quad (15)$$

The two contributions can be treated separately. For the series resistance:

$$\dot{R}_s(t) = -K_1 \frac{v_s(t)}{R_s(t)} \quad (16)$$

being  $v_s(t)$  the voltage across the series of  $R_1$  and  $R(Q)$  as shown in Fig. 6(b). By integrating (16) and considering  $R_s(0) = R_1$ , it is obtained:

$$R_s(t) = \sqrt{R_1^2 - 2K_1 \Delta\varphi_1(t)} \quad (17)$$

with  $\Delta\varphi_1(t) = \int_0^t v_s(\tau) d\tau$ .

For the parallel resistance, it results:

$$\dot{R}_p(t) = -K_2 v_p(t) R_p(t) \quad (18)$$

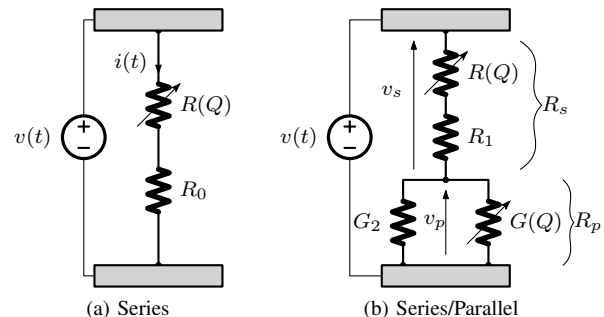


Fig. 6. Series/parallel models of the CF. Traditional series model (a) and series/parallel model (b). The filament stretching is described by the series, while the filament widening is modeled by the parallel.

where  $v_p(t)$  is the voltage across the parallel of  $G_2$  and  $G(Q)$ , as schematized in Fig. 6(b). By integrating with  $R_p(0) = R_2$ :

$$R_p(t) = R_2 e^{-K_2 \Delta \varphi_2(t)} \quad (19)$$

$$\text{with } \Delta \varphi_2(t) = \int_0^t v_p(\tau) d\tau$$

The terms  $v_s(t)$  and  $v_p(t)$  can be simply calculated as:

$$\begin{cases} v_s(t) = \frac{R_s(t)}{R_s(t) + R_p(t)} v(t) \\ v_p(t) = \frac{R_p(t)}{R_s(t) + R_p(t)} v(t) \end{cases} \quad (20)$$

The voltage-memristance relation expressed as a function of the time is finally:

$$R_M(t) = \sqrt{R_1^2 - 2K_1 \Delta \varphi_1(t)} + R_2 e^{-K_2 \Delta \varphi_2(t)} \quad (21)$$

and it can be numerically determined by the following relations:

$$\begin{cases} R_s(t) = \sqrt{R_1^2 - 2K_1 \Delta \varphi_1(t)} \\ \Delta \varphi_1(t) = \int_0^t \frac{R_s(\tau)}{R_s(\tau) + R_p(\tau)} v(\tau) d\tau \\ R_p(t) = R_2 e^{-K_2 \Delta \varphi_2(t)} \\ \Delta \varphi_2(t) = \int_0^t \frac{R_p(\tau)}{R_s(\tau) + R_p(\tau)} v(\tau) d\tau \end{cases} \quad (22)$$

By defining the ratio  $\alpha$  as:

$$\alpha = \frac{R_2}{R_1} \quad (23)$$

(21) can be accordingly rewritten as:

$$R_M = R_0 \left[ \sqrt{\frac{1}{(1 + \alpha)^2} - \frac{2K_1}{R_0^2} \Delta \varphi_1} + \frac{\alpha e^{-K_2 \Delta \varphi_2}}{1 + \alpha} \right] \quad (24)$$

The ratio  $\alpha$  is supposed to be constant, but with different values for the *set* and *reset*, as the drift process in the two phases is strongly asymmetrical.

Fig. 7(a) shows simulated results of the series/parallel model versus the traditional. As  $\alpha$  increases, by keeping constant  $K_1$  and  $K_2$ , the contribution to the resistive change depends more on the filament widening, i.e. on the parallel behavior.

With decreasing  $\alpha$ , the model tends to fit the traditional series interpretation. As it will be shown in Section V, for both *set* and *reset* phases, estimated values of  $\alpha > 0$  are necessary to match the experimental curves, testifying the significance of the parallel behavior in real memristive devices.

The ratio between  $K_1$  and  $K_2$  determines the time evolution of the CF. As the ratio  $K_1/K_2$  increases, the filament growth is predominant with respect to its widening. In Fig. 7(b) some results have been shown. As it can be noticed, when  $K_1/K_2$  is particularly large, the resistance drop is mainly determined by the square root law (series equivalent), until the CF length reaches the memristor thickness  $D$ , saturating. At this point, the remaining resistance drop is due to the CF widening (parallel equivalent).

A benefit of the proposed model is the low computational complexity introduced (only four fitting parameters) with respect to the high flexibility and the good matching that can be achieved.

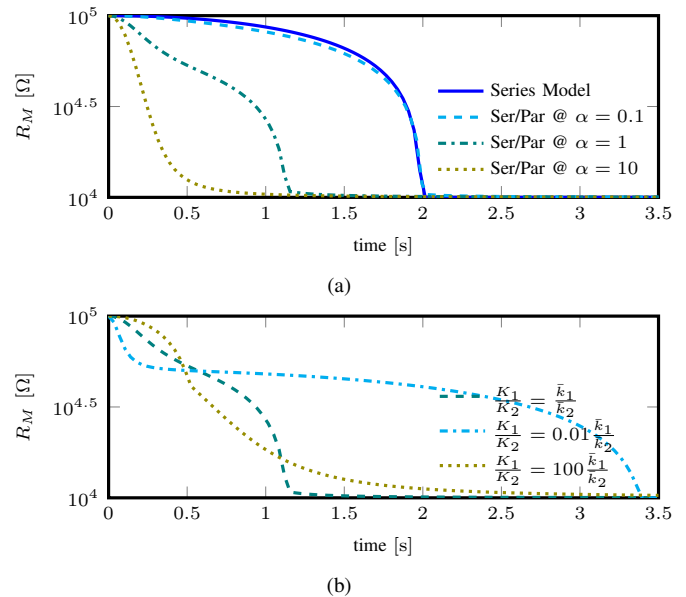


Fig. 7. Simulated curves for the series/parallel model of the memristor described in (22) in comparison with the traditional model. The curves in (a) have been evaluated with different values of  $\alpha$  and constant values for  $K_1 = 2.1 \text{ G}\Omega \text{ C}^{-1}$  and  $K_2 = 60 \text{ S C}^{-1}$ , while in (b) different ratios of  $K_1$  and  $K_2$  with  $\alpha = 1$  have been used. The used values for  $R_M(0) = R_{\text{off}}$  and  $R_{\text{on}}$  are  $100 \text{ k}\Omega$  and  $10 \text{ k}\Omega$ , respectively. A voltage double ramp with  $\Delta V/\Delta t = 1 \text{ V s}^{-1}$  has been used.

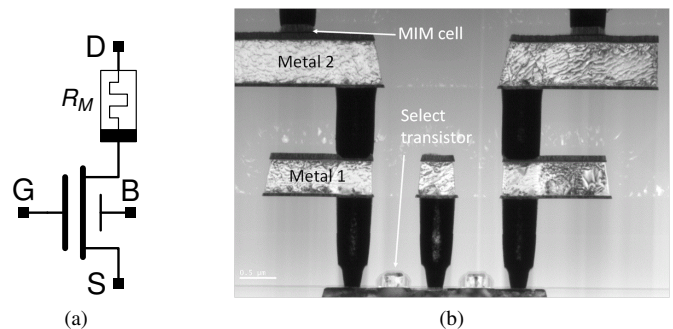


Fig. 8. Schematic diagram of the 1T-1R ReRAM cell (a) and cross-sectional TEM image of two 1T-1R ReRAM cells (b).

## V. MEASUREMENTS AND MODEL VALIDATION

### A. The $\text{HfO}_2$ ReRAM Cell

Fig. 8(a) shows the schematic diagram of the available 1T-1R memory cell. The memory element,  $R_M$ , is at the drain of an nMOS transistor (whose  $W/L$  ratio is  $1.14 \mu\text{m}/0.24 \mu\text{m}$ ) which acts as a cell selector and sets the current compliance. The memory cell is manufactured in a 250-nm BiCMOS process, [7].

A 1T-1R cell TEM image, in which the memristor MIM stack is recognizable, is shown in Fig. 8(b). The MIM area is equal to  $0.4 \mu\text{m}^2$ . Metal 1 as well as metal 2 are metallic layer stacks, consisting of Ti/TiN/Al/TiN/Ti. The MIM integrated on the metal line 2 of the BiCMOS process is composed by 150-nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 7-nm Ti layer, and a 8-nm  $\text{HfO}_2$  layer were grown by atomic vapor deposition (AVD) using a metal organic TEMAH precursor.

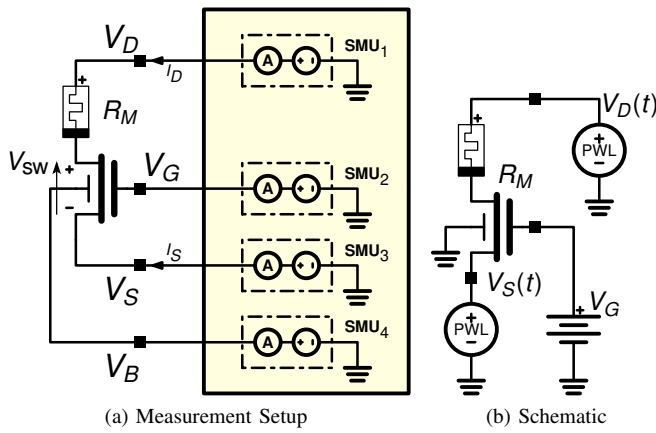


Fig. 9. Scheme of the measurement connection (a) and schematic used for the circuit simulations (b).

### B. Experimental Results

Measurements have been performed on 1T-1R devices and carried out with the characterization system Keithley 4200-SCS. The 1T-1R devices have been implemented with independent and separately accessible terminals. The characterization curves have been obtained by driving the devices with rising and falling voltage sweeps in the range  $[0, 3.5]$  V (compatible with the voltage limits of the used 250-nm technology), with a slope of around  $1 \text{ V s}^{-1}$ . Each terminal of the 1T-1R device (drain/memristor, source, gate and bulk) has been driven with a dedicated Source Measurement Unit (SMU) channel. Constant gate voltage values of 1.3 V and 2.8 V for *set* and *reset* have been respectively used. The higher gate voltage during the *reset* process is necessary to keep the transistor as much as possible in the linear region. The measurements setup is shown in Fig. 9(a).

Devices have been stimulated with 100 *set* and *reset* cycles. The mean value of the measured curves related to the 100 cycles has been then calculated. Fig. 10 and Fig. 11 show the simulated and measured data comparison for *set* and *reset* operations, respectively.

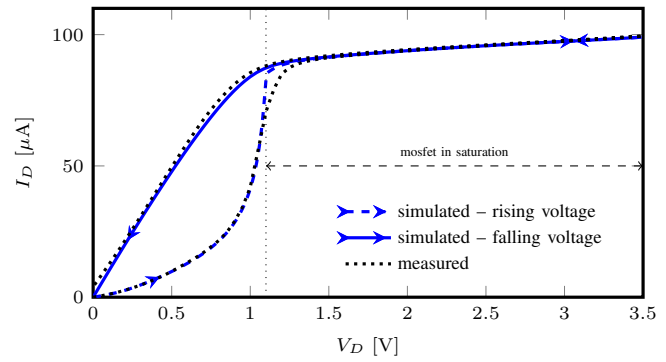
The extrapolated resistance values in Fig. 10(b) and Fig. 11(b) for the *set* and *reset* phases, respectively, have been evaluated by:

$$R_{M, \text{set}} = \frac{V_D - |V_{\text{sw}}|}{I_D} \quad (25)$$

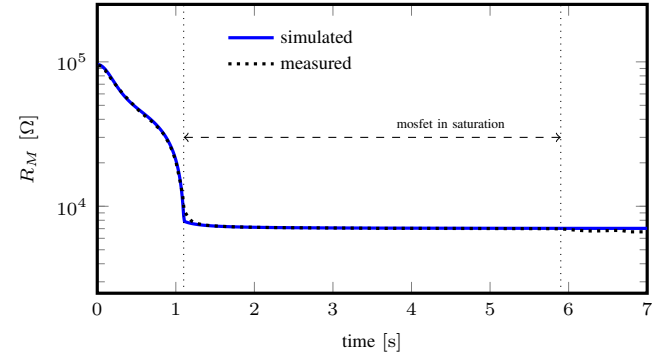
$$R_{M, \text{reset}} = \frac{V_S - |V_{\text{sw}}|}{I_S} \quad (26)$$

as the actual *set/reset* voltage supplied by the SMU has to be evaluated by subtracting the voltage  $V_{\text{sw}}$  across the transistor, whose value has been calculated by mean of simulations.

The simulations have been carried out performing transient analysis with common BSIM models for the selector transistor of the cell and a Verilog-A model for the memristor, according to the schematic shown in Fig. 9(b). The voltage stimuli used during the measurement cycles have been externally recorded and used as input vectors in the simulations by mean of piecewise linear (PWL) voltage sources.

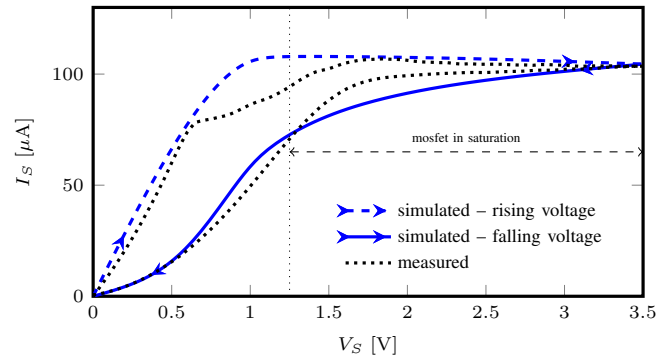


(a) Set - I-V characteristic

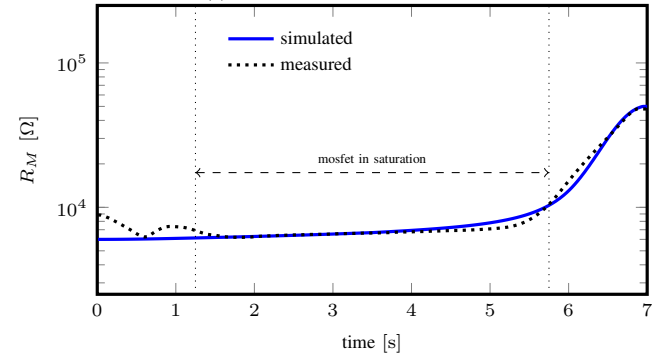


(b) Set - Memristance as a function of the time

Fig. 10. Set - Simulated and measured I-V characteristic (a) and memristance time behavior (b) for  $\alpha = 1.083$ ,  $R_M(0) = R_{\text{off}} = 96 \text{ k}\Omega$ ,  $R_{\text{on}} = 7.5 \text{ k}\Omega$ ,  $K_{1\text{set}} = 2.1 \text{ G}\Omega \text{ C}^{-1}$ ,  $K_{2\text{set}} = 120 \text{ S C}^{-1}$ .



(a) Reset - I-V characteristic



(b) Reset - Memristance as a function of the time

Fig. 11. Reset - Simulated and measured I-V characteristic (a) and memristance time behavior (b) for  $\alpha = 0.05$ ,  $R_M(0) = R_{\text{on}} = 7.5 \text{ k}\Omega$ ,  $R_{\text{off}} = 96 \text{ k}\Omega$ ,  $K_{1\text{reset}} = 0.5 \text{ M}\Omega \text{ C}^{-1}$ ,  $K_{2\text{reset}} = 12.95 \text{ S C}^{-1}$ .

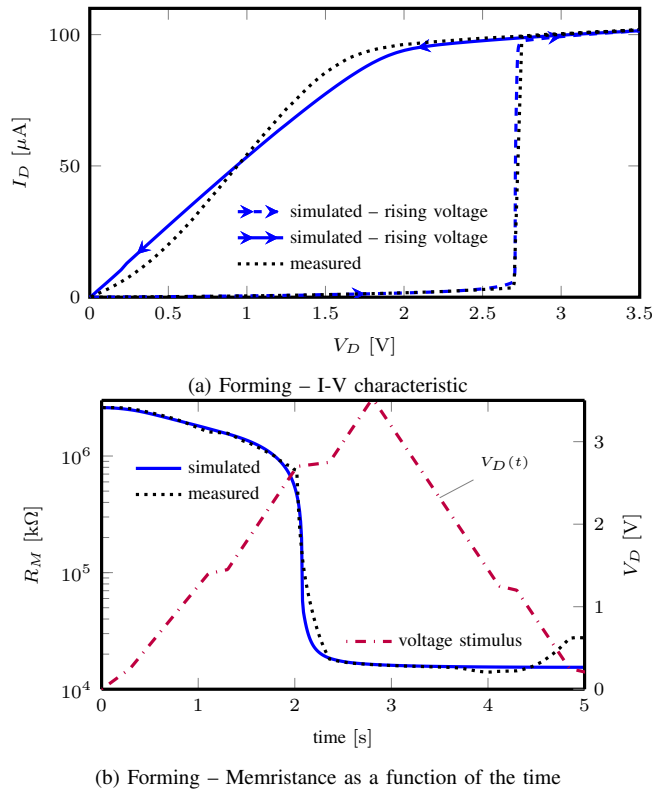


Fig. 12. Forming – Simulated and measured I-V characteristic (a) and memristance time behavior (b) for  $\alpha = 0.5$ ,  $R_M(0) = R_{\text{off}} = 2.6 \text{ M}\Omega$  (pristine state),  $R_{\text{on}} = 14 \text{ k}\Omega$ ,  $K_{1\text{form}} = 650 \text{ G}\Omega \text{ C}^{-1}$ ,  $K_{2\text{form}} = 20 \text{ S C}^{-1}$ .

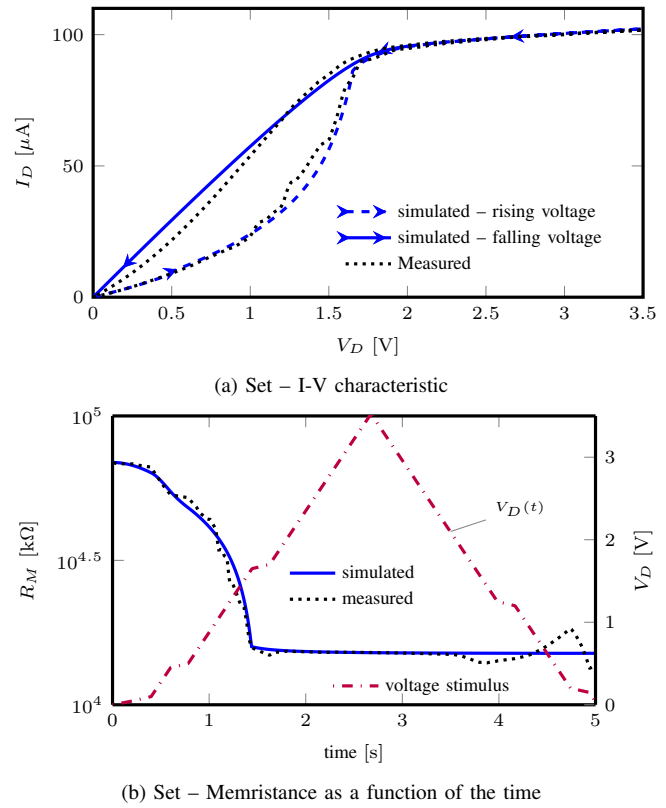


Fig. 14. Set – Simulated and measured I-V characteristic (a) and memristance time behavior (b) for  $\alpha = 0.5$ ,  $R_M(0) = R_{\text{off}} = 65 \text{ k}\Omega$ ,  $R_{\text{on}} = 14 \text{ k}\Omega$ ,  $K_{1\text{set}} = 1.3 \text{ G}\Omega \text{ C}^{-1}$ ,  $K_{2\text{set}} = 90 \text{ S C}^{-1}$ .

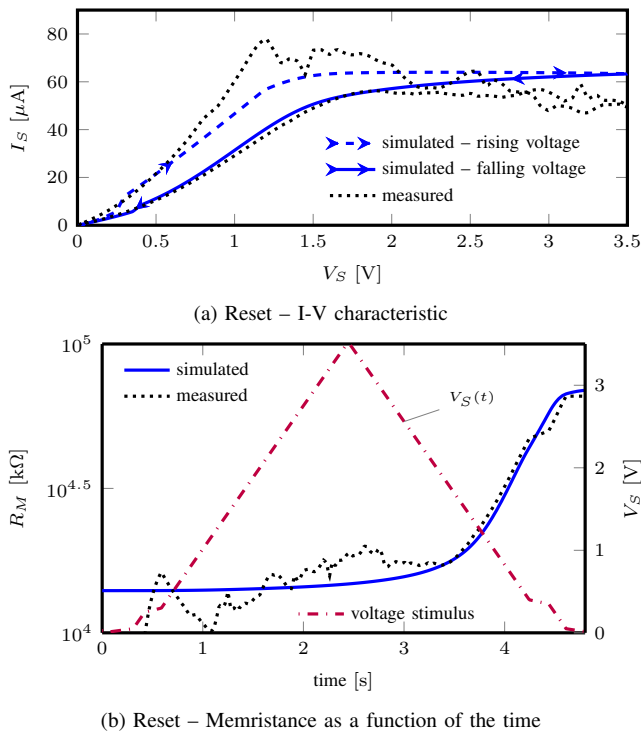


Fig. 13. Reset – Simulated and measured I-V characteristic (a) and memristance time behavior (b) for  $\alpha = 0.05$ ,  $R_{\text{off}} = 65 \text{ k}\Omega$ ,  $R_M(0) = R_{\text{on}} = 14 \text{ k}\Omega$ . For the simulated values, the parameter are  $K_{1\text{reset}} = 0.75 \text{ M}\Omega \text{ C}^{-1}$  and  $K_{2\text{reset}} = 15.45 \text{ S C}^{-1}$ .

### C. Discussion of the Results

Simulated *set* curves in Fig. 10(a) show a very good match when compared with the measured ones. In the first part of the I-V curve, it is possible to recognize the increasing slope of the current, due to the resistance decrease. At around 1.1 V, the cell selector transistor leaves the triode region and operates in saturation region, limiting the current increase. In the last part of the curve, as the resistance change has reached a low resistive state, the current decreases with a constant slope.

Fig. 10(b) shows the memristance  $R_M$  behavior as a function of time. The matching of simulated and measured curves is very good, differently from the cases reported in Fig. 5, in which both the linear and non-linear models are not capable to give a proper description of the phenomenon. By the observation of the time evolution of the memristance, it can be noticed how the extension and widening of the CF (i.e. series and parallel resistance contributions) occur at the same time with a comparable magnitude.

In the case of the *reset* simulations in Fig. 11, a very good match is achieved as well. In particular, as it can be seen by the I-V representation in Fig. 11(a), the current slope in the first portion of the curve is essentially constant until the switch transistor saturates. A noticeable resistance increase can be seen in the last portion of the curve, when the cell selector transistor returns to the triode region. Such a *reset* behavior is coherently described in Fig. 11(b). During the rising slope of the driving voltage and, later, during the saturation of the

TABLE I  
PARAMETERS VALUES

parameter	sample 1		sample 2		
	<i>set</i>	<i>reset</i>	<i>form</i>	<i>set</i>	<i>reset</i>
$R_{\text{off}}$ [k $\Omega$ ]	96		65		
$R_{\text{on}}$ [k $\Omega$ ]	7.5		14		
$\alpha$	1.11	0.05	0.5		0.05
$K_1$ [M $\Omega$ C $^{-1}$ ]	$2.1 \times 10^3$	0.50	$650 \times 10^3$	$1.3 \times 10^3$	0.75
$K_2$ [S C $^{-1}$ ]	120	12.95	20	90	15.45

transistor that limits the current through the memristor, the memristance keeps its value almost unvaried.

A considerable increase of the memristance value can be appreciated only for  $t > 5.8$ s, when the decrease of the voltage stimulus is such that the transistor returns in the triode region. As it can be noticed, the resistance exponentially rises, confirming the important contribution of the parallel conductance variation.

Additional experimental results are shown in Fig. 12, Fig. 13 and Fig. 14. The plots depict *forming*, *reset* and *set* curves for a 1T-1R cell from a different sample, forced by voltage stimuli having arbitrary shapes, with slopes varying in time. The waveforms have been conveniently recorded in a stimuli file used for the computer simulations.

Also in this case, a very good matching between simulated and measured data is obtained. The device, initially having a pristine resistance of 2.6M $\Omega$  is formed, reaching a resistance of around 14k $\Omega$  and successively reset, bringing its resistance to a high resistive state of 65k $\Omega$ . Then, with a *set* cycle, the device reaches again a low resistance value.

A remarkable aspect of these curves is that the *reset* process is much slower than the *set* one: an appreciable resistance increase occurs only in the final part of the process. Moreover, the curves clearly exhibit how the predominant mechanism during the *reset* phase is the tapering of the filament.

Table I summarizes the parameter values used in the simulations. The values of  $R_{\text{off}}$  and  $R_{\text{on}}$  represent the initial values for the *set* and *reset* operation, respectively.

As it can be noticed, in the *reset* phase the contribution of the parallel switching behavior is more significant. This is numerically expressed by the fact that the ratio  $(K_1/K_2)_{\text{reset}}$  ( $38.6 \times 10^3 \Omega^2$  and  $48.5 \times 10^3 \Omega^2$  for the first and second sample, respectively) is much larger than  $(K_1/K_2)_{\text{set}}$  ( $17.5 \times 10^6 \Omega^2$  for the first sample and  $14.4 \times 10^6 \Omega^2$  for the second one). Thus, even if a lower value for  $\alpha$  has been evaluated for the *reset* operation ( $0.05 \leq \alpha_{\text{reset}}/\alpha_{\text{set}} \leq 0.1$ ), a larger value for  $K_{2\text{reset}}$  determines the exponential addendum to dominate in the expression.

## VI. CONCLUSIONS

In this paper a new electrical model for Oxide Resistive RAMs has been presented. The traditional series model has been extended, exploiting considerations on the filamentary behavior and keeping the assumption of a linear kinetics.

The model considers two contributions to the resistance change inside the device: the filament extension and the filament widening. The former shows a square-root behavior with the flux, while the latter an exponential one. The combination of the parameters  $\alpha$ ,  $K_1$  and  $K_2$  define a precise filament time evolution: for a dominant square-root-law contribution, the resistance change is mainly due to the filament extension; on the other hand, if the exponential law is predominant, the width of the filament matters in the resistance switch.

The used approach allows an excellent fitting of experimental results while keeping the physics of the process into account.

Experimental data collected on 1T-1R cells integrated in a 250-nm BiCMOS process have proven the consistency of the assumption. In particular, it has been possible to observe that in the filament creation/reconstitution the prevalent phase is, coherently, the filament stretching. The reset phase, on the other hand, has prevalently shown an exponential evolution, suggesting that the filament volume is worn out by the oxidation until its rupture.

The model is easily implementable in traditional circuit simulator integrated environments, representing a fast and strong tool for a reliable and fast design of resistive memories.

## REFERENCES

- [1] L. Chua, "Memristor –the missing circuit element," *IEEE Transactions On Circuits Theory*, vol. 18, pp. 507–519, Sept. 1971.
- [2] D. Strukov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.
- [3] Y. Joglekar and S. Wolf, "The elusive memristor: Properties of basic electrical circuits," *European Journal of Physics*, vol. 30, pp. 661–675, May 2009.
- [4] Z. Birolek, D. Birolek, and B. Biolková, "Spice model of memristor with nonlinear dopant drift," *Radio Engineering*, vol. 18, pp. 210–214, June 2009.
- [5] S. Benderli and T. Wey, "On spice macromodelling of TiO<sub>2</sub> memristors," *IEEE Electronic Letters*, vol. 45, pp. 377–379, Mar. 2009.
- [6] T. Prodromakis, B. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with non-linear dopant kinetics," *IEEE Transactions On Electron Devices*, vol. 59, pp. 3099–3105, Sept. 2011.
- [7] D. Walczyk, C. Walczyk, T. Schroeder, T. Bertaud, M. Sowińska, M. Lukosius, M. Fraschke, B. Tillack, and C. Wenger, "Resistive switching characteristics of CMOS embedded HfO<sub>2</sub>-based 1T1R cells," *Microelectronic Engineering*, vol. 88, pp. 1133–1135, July 2011.
- [8] A. Grossi, D. Walczyk, C. Zambelli, E. Miranda, P. Olivo, V. Stikanov, A. Feriani, J. S. né, G. Schoof, R. Kraemer, B. Tillack, A. Fox, T. Schroeder, C. Wenger, and C. Walczyk, "Impact of intercell and intracell variability on forming and switching parameters in RRAM arrays," *IEEE Transactions On Electron Devices*, vol. 62, pp. 2502–2509, Aug 2015.
- [9] D. S. Jeong, H. Schroeder, U. Breuer, and R. Waser, "Characteristic electroforming behavior in Pt/TiO<sub>2</sub>/Pt resistive switching cells depending on atmosphere," *Journal of Applied Physics*, vol. 104, Dec. 2008.
- [10] K. Kim, D. Jeong, and C. Hwang, "Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook," *Nanotechnology*, vol. 22, June 2011.
- [11] S. Amer, S. Sayyaparaju, G. Roseand, K. Beckmann, and N. Cady, "A practical hafnium-oxide memristor model suitable for circuit design and simulation," in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems (ICECS'17)*, pp. 1–4, 2017.
- [12] E. Linn, A. Siemon, R. Waser, and S. Menzel, "Applicability of well-established memristive models for simulations of resistive switching devices," *IEEE Transactions on Circuits and Systems-I*, vol. 61, pp. 2402–2410, Aug. 2014.
- [13] M. Pickett, D. Strukov, J. Borghetti, J. Yang, G. Snider, D. Stewart, and R. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal Of Applied Physics*, vol. 106, p. 074508, Oct. 2009.



- [14] J. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," *Journal of Applied Physics*, vol. 34, pp. 1793–1803, June 1963.
- [15] A. Ascoli, F. Corinto, V. Senger, and R. Tetzlaff, "Memristor model comparison," *IEEE Circuits and Systems Magazine*, vol. 13, pp. 889–105, May 2013.
- [16] Z. Kolka, D. Birolek, and V. Biolková, "Improved model of TiO<sub>2</sub> memristor," *Radioengineering*, vol. 24, pp. 378–383, June 2015.
- [17] N. McDonald, R. Pino, P. Rozwood, and B. T. Wysocki, "Analysis of dynamic linear and non-linear memristor device models for emerging neuromorphic computing hardware design," in *Proceedings of IEEE International Joint Conference on Neural Networks (IJCNN'10)*, pp. 1–5, 2010.
- [18] R. Pino, J. Bohl, N. McDonald, B. Wysocki, P. Rozwood, K. Campbell, A. Oblea, and A. Timilsina, "Compact method for modeling and simulation of memristor devices: Ion conductor chalcogenide based memristor devices," in *Proceedings of the 2010 IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 1–4, 2010.
- [19] M. Uddin, M. Majumder, G. Rose, K. Beckmann, H. Manem, Z. Alamgir, and N. C. Cady, "Techniques for improved reliability in memristive crossbar puf circuits," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI'16)*, pp. 212–217, 2016.
- [20] B. Choi, D. Jeong, S. Kim, C. Rohde, S. Choi, J. Oh, H. Kim, C. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO<sub>2</sub> thin films grown by atomic-layer deposition," *Journal of Applied Physics*, vol. 98, Aug 2005.
- [21] D. Kwon, K. Kim, J. Jang, J. Jeon, M. Lee, G. Kim, X. S. Li, G. Park, B. Lee, S. Han, M. Kim, and C. Hwang, "Atomic structure of conducting nanofilaments in TiO<sub>2</sub> resistive switching memory," *Nature Nanotechnology*, pp. 148–153, Feb 2010.
- [22] A. Grossi, C. Zambelli, P. Olivo, E. Miranda, V. Stikanov, T. Schroeder, C. Walczyk, and C. Wenger, "Relationship among current fluctuations during forming, cell-to-cell variability and reliability in RRAM arrays," in *Proceedings of IEEE International Memory Workshop (IMW'15)*, 2015.
- [23] E. Pérez, A. Grossi, C. Zambelli, P. Olivo, R. Roelofs, and C. Wenger, "Reduction of the cell-to-cell variability in Hf<sub>1-x</sub>Al<sub>x</sub>O<sub>y</sub> based RRAM arrays by using program algorithms," *IEEE Electron Device Letters*, vol. 38, pp. 175–178, Feb. 2017.
- [24] E. Pérez, A. Grossi, C. Zambelli, P. Olivo, R. Roelofs, and C. Wenger, "Impact of the incremental programming algorithm on the filament conduction in HfO<sub>2</sub>-based RRAM arrays," *IEEE Journal of the Electron Devices Society*, vol. 5, pp. 64–68, Jan. 2017.
- [25] S. Long, X. Lian, C. Cagli, X. Cartoixa, R. Rurali, E. Miranda, D. Jiménez, L. Perniola, M. Liu, and J. S. né, "Quantum-size effects in hafnium-oxide resistive switching," *Journal of Applied Physics*, vol. 102, May 2013.
- [26] E. A. Miranda, C. Walczyk, C. Wenger, and T. Schroeder, "Model for the resistive switching effect in HfO<sub>2</sub> MIM structures based on the transmission properties of narrow constrictions," *IEEE Electron Device Letters*, vol. 31, pp. 609–611, June 2010.
- [27] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," *IEEE Transactions on Electron Devices*, vol. 58, pp. 4309–4317, Dec. 2011.



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