Substrate Integrated Waveguide E-plane 3-dB Power Divider/Combiner Based on Resistive Layers

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***Abstract* — Several different microwave circuits, including beam-forming networks and balanced amplifiers, make use of 3-dB power dividers and combiners. A well known architecture able to work over large bandwidths, a critical request for many applications, is based on E-plane three-port waveguide structures, where a lossy element is added to overcome the inherently poor isolation given by lossless three-port junctions.**

While a standard implementation based on normal rectangular waveguides often results in large and heavy structures, an implementation based on substrate integrated waveguide (SIW) technology, offers advantages in terms of compactness, weight reduction, cost minimization, and integration possibilities with active stages.

This paper presents the design, fabrication, and characterization of two SIW E-plane 3-dB power divider/combiners where the lossy element is realized using a resistive layer. The prototypes cover the entire X band from 8 GHz to 12 GHz and the resistive layers are realized according to two different manufacturing techniques to investigate the potentials of both approaches.

The optimization of the resistive layer geometry and resistivity, a critical aspect for low-profile SIW circuits, is discussed in detail. In particular, an analytical formula is derived, which allows to determine the optimum values for the resistive layers principal parameters, namely the length and resistivity, without the use of full-wave numerical solvers.

***Index Terms* — E-plane circuit; power combiner; power divider; resistive septum, card, paste; substrate integrated waveguide; thick film resistor, wideband.**

I. Introduction

SEVERAL circuits at microwave and mm-wave frequencies require the use of power dividing and combining techniques. Some of the most typical applications include beam-forming networks, used for example to feed antenna arrays, and balanced mixers and amplifiers, used for example to increase the output power and/or the reliability of amplifying stages [1, 2]. The most common architectures used to realize power dividing/combining networks can be divided into three different categories according to the layout topology, namely tree, N-way, and chain structures, reported in Fig. 1 [3]. Tree structures rely on the use of a number of 3-dB dividers/combiners cascaded to achieve the required power fractioning/multiplying on the basis of a binary scale. The main advantage of this solution is the design flexibility and the overall performance, as long as the number of stages to achieve the required power fractioning/multiplying does not exceed a critical threshold (depending on fabrication technology, application, etc.), beyond which the losses along a single path and the overall volume and/or mass are not longer tolerable. A variation implements dividers/combiners with unequal power division/combination, allowing for arbitrary power laws not restricted to the binary scale.

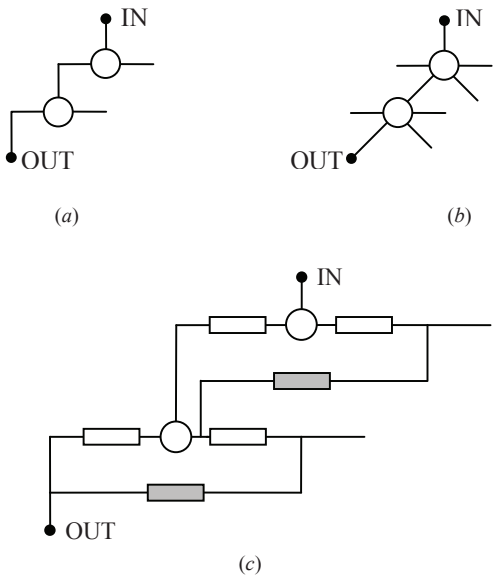

Fig. 1. Schematic layout for different types of power dividing/combining networks, where the white circle represents the single power divider: (*a*) tree; (*b*) N-way, in this example N = 4; (*c*) chain, where white and grey rectangles represent propagations lines and resistive elements, respectively.

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N-way structures can partially overcome the disadvantages of tree structures providing more than two branches, at the cost of increased complexity. Chain structures, also known as travelling-wave structures, based on the use of propagation lines, are sometimes implemented for broadband (typically more than one octave) applications where high isolation between output ports is achieved by means of resistive elements, at the cost of an even more increased complexity.

Regardless of the network architecture, it is often desirable to have a power divider/combiner able to cover large bandwidths and as compact as possible (thus minimizing device losses, volume, and mass). A well known solution to achieve these requirements is represented by waveguide E-plane T-junctions, which comes at the cost of a limited isolation between the output ports [4]. To improve the latter, approaches based on resistive losses between output ports have been proposed, including solutions based on a coupling slot and a lumped resistor [5], finlines [6], and resistive cards (also known as septums) [7–9]. In particular, E-plane T-junctions using resistive layers, which require the introduction of a dissipative layer in between the upper and lower waveguide, are attractive for an implementation based on printed circuits manufacturing techniques, most notably Substrate Integrated Waveguides (SIWs). While mimicking the propagation properties of standard waveguides, SIWs represent a valid alternative offering, according to the application and to the operation frequency, extra advantages for one or more of the following aspects, stemming from the use of printed circuits manufacturing techniques: compactness, weight reduction, cost minimization, and integration possibilities with active stages [10, 11]. In addition, SIWs have been already used to implement power dividers and combiners according to different approaches, including solutions based on surface mounted (SMD) resistors [12, 13], which however require a slot in the metalization of the SIW and cannot be easily integrated inside a multilayer printed circuit board.

This paper addresses the design of 3-dB E-plane T-junctions based on resistive layers. Starting from the preparatory work presented in [14, 15], in this paper for the first time the optimization of the resistive layer geometry and resistivity is discussed in detail, and an analytical formula that permits to calculate the optimum ratio between the resistive layer length and resistivity for rectangular-shaped layers is derived. While these results are applicable to any E-plane T-junctions based on resistive layers, regardless of the fabrication process, this paper is then focused on an SIW implementation, designing, manufacturing and testing two demonstrators working from 8 GHz to 12 GHz. With the aim of investigating two different manufacturing techniques for the resistive layer, two approaches are exploited. The first prototype, presented in this paper for the first time and developed on the grounds of the preliminary simulations shown in [14], is realized using a flexible resistive card and milling technique. The second prototype is realized using a resistive thick film and screen-printing [16], thus with a different manufacturing technique with respect to photolithography, adopted for the prototype shown in [15].

SIW implementation represents a particularly interesting case because of the extreme ratio between the waveguide width and height (dictated by the dielectric substrate). In addition, the SIW implementation, based on a stack-up composed by two identical dielectric substrates, naturally leads to a 3-dB power division/combination. This feature, most often not present for standard waveguides [7–9], represents the solution-of-choice for balanced amplifiers, where power dividers/combiners are often cascaded.

The paper is organized as follows. In Sec. II the structure of the 3-dB E-plane power divider/combiner is presented, and an analytical formula that permits to calculate the optimum ratio between the resistive layer length and resistivity for rectangular-shaped layers is presented. Sec. III discusses the parametric design of the resistive layer for different values of the layer length and resistivity. Sec. IV presents the analysis, fabrication, and testing of the two SIW demonstrators, introducing design criteria for non-rectangular layers.

II. Design Formulas for 3-dB E-plane Power Divider/Combiners

The working principle of a 3-dB E-plane power divider/combiner based on resistive layers can be discussed regardless of the manufacturing technique, either using standard waveguides or SIWs. However, since the final aim of this paper is to design, fabricate, and test an SIW implementation, the following discussion refers to this type of structure. A typical SIW permits the propagation of the electromagnetic field along a dielectric slab of thickness b where the confinement is achieved using a top and bottom metal layer and two rows of metalized vias. The propagation of the electromagnetic field is similar to standard waveguides, and it can be studied using the normal theory of TE_{n0} modes (in particular the fundamental TE_{10} mode), after calculating the equivalent waveguide width a from the SIW geometrical parameters, namely the via spacing s, the via diameter d, and the rows separation w [17, 18]. However, the lateral confinement is not perfect and in principle it leads to a certain amount of leakage [19–21] (apart from the case of a continuous wall, where $s = d$ [22]), which it can be accurately calculated [23, 24] and minimized controlling the SIW geometrical parameters [25, 26].

The structure of the 3-dB E-plane power divider/combiner is shown in Fig. 2, where the upper dielectric layer is shown separated from the lower dielectric layer. Along the right part of the structure these two layers are contiguous, forming a single SIW excited by port 1, while along the left part they are separated by a central metallic plane that creates two separate SIWs, excited by port 2 (upper SIW) and port 3 (lower SIW), respectively. As anticipated in the previous section, resistive losses are introduced to improve the isolation between port 2 and port 3. In particular, in the central part of the power divider/combiner the separation between the upper and lower SIW is not provided by a metallic plane. Instead, a rectangular-shaped resistive layer (width x, length y) is used, which provides a coupling region between the two SIWs.

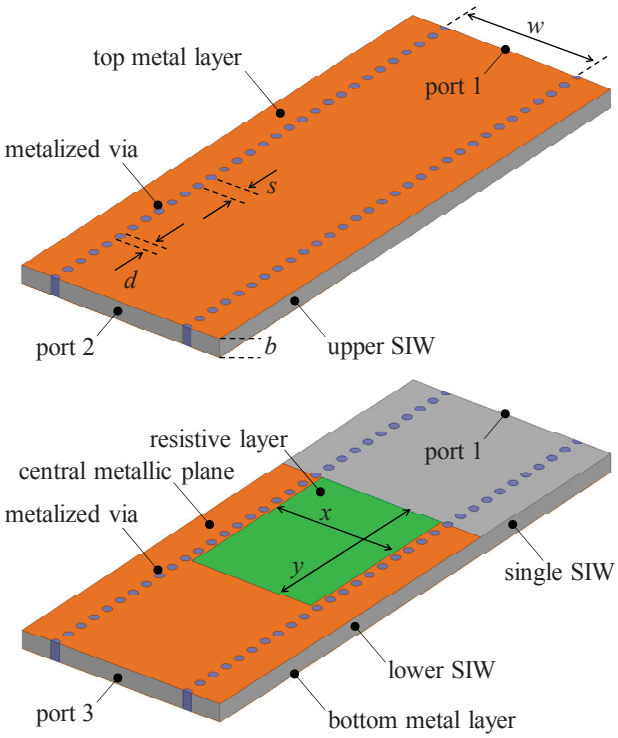


Fig. 2. Schematic of the 3-dB E-plane Power Divider/Combiner showing the upper dielectric slab, with the upper SIW and half of the single SIW (top) and the lower dielectric slab with the lower SIW, half of the single SIW, the central metallic plane and the resistive layer (bottom).

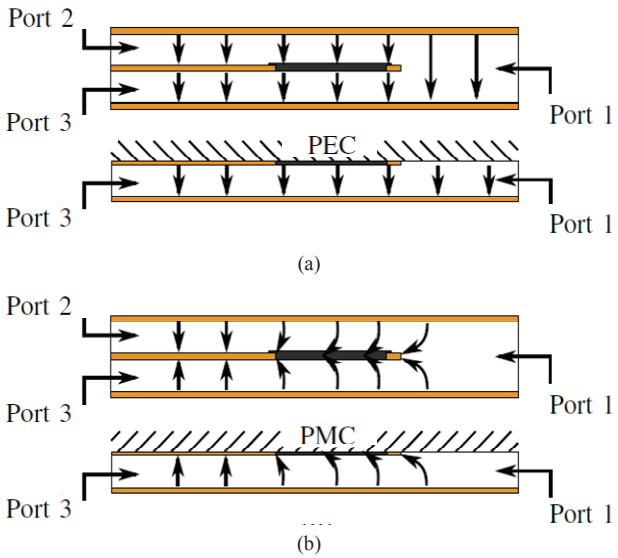


Fig. 3. Schematic representation for the working principle of the 3-dB E-plane Power Divider/Combiner: (a) the balanced (even) mode (PEC symmetry); (b) the unbalanced (odd) mode (PMC symmetry).

The working principle can be discussed as follows, and it is schematically depicted in Fig. 3. When the input signal is launched at port 1 (device operating as divider), the symmetrical structure of the power divider (i.e., substrate slabs with equal thickness) provides a natural 3-dB division of the input power with ideally perfect magnitude and phase balance.

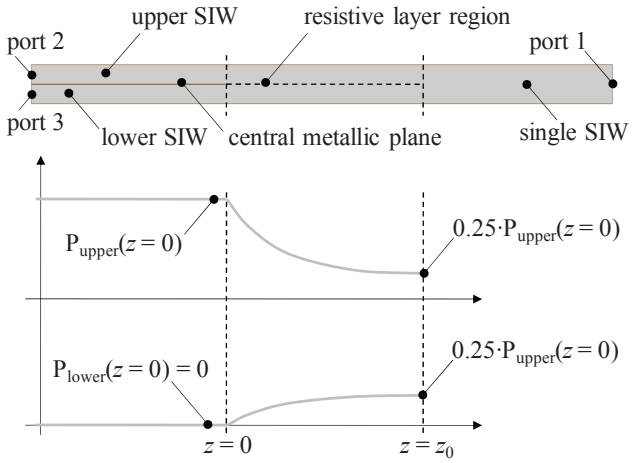


Fig. 4. Side view of the schematic of the 3-dB E-plane Power Divider/Combiner (top) and schema of the power propagation within the upper and lower SIW (bottom) when port 2 is excited.

In addition, the E-plane implementation guarantees the correct power division at all operation frequencies, being the only frequency limitation provided by the bandwidth of the fundamental TE_{10} mode. Moreover, it is important to observe that in this case the resistive layer does not dissipate power. This is because the current density on the resistive layer associated to the fundamental TE_{10} mode of the upper SIW is equal in magnitude and opposite in phase with respect to the current density associated to the fundamental TE_{10} mode of the lower SIW. Therefore, the total net current density on the resistive layer is null.

When the input signal is launched using port 2 and/or port 3 (device operating as combiner), any difference in magnitude and/or phase between the signal at port 2 and the signal at port 3 generates a net current density on the resistive layer. Therefore, the resistive layer dissipates the power associated to the unbalanced mode, for which the symmetry plane appears like a perfect magnetic conductor (PMC). This mode corresponds to a net power flow from port 2 to port 3, or vice-versa, and the resistive layer thus improves the isolation. Whereas the balanced mode, for which the symmetry plane appears like a perfect electric conductor (PEC), corresponds to the power flow from port 2 and port 3 to port 1. Two extreme cases are worth special consideration to better understand the working principle. First, when port 2 and port 3 are excited with signals equal in magnitude and phase (i.e., perfect balance), all the input power is combined in port 1, and no current is generated on the resistive layer. Thus, this situation is exactly the reciprocal case of the case discussed before, when the port 1 is excited. Second, when only port 2 or port 3 is excited (i.e., total un-balance) the current generated on the resistive layer is maximum. This case is schematically depicted in Fig. 4 where port 2 is excited, with the ideal assumption of perfect input matching for all ports and perfect isolation between port 2 and port 3. The coupling region defined by the resistive layer provides a decay of the power propagating in the upper SIW, which is partially coupled to the lower SIW, and partially dissipated by the resistive layer.

When the power propagating in the lower SIW is equal to the power propagating in the upper SIW, the net current on the resistive layer is null, and no further power dissipation occurs. Regardless of the resistive layer length and/or resistivity, the merging of the upper and lower SIW into a single SIW at $z = z_0$, which turns into the merging of the fundamental TE_{10} modes propagating in the upper and lower SIW into the TE_{10} mode propagating in the single SIW, always provides a boundary condition at $z = z_0$ that forces the magnitude and phase of the field propagating in the upper SIW to be identical to the magnitude and phase of the field propagating in the lower SIW. Consequently:

$$P_{upper}(z = z_0) = P_{lower}(z = z_0) \tag{1}$$

where P_{upper} is the power propagating in the upper SIW and P_{lower} is the power propagating in the lower SIW. Exploiting the reciprocity of the device, which imposes:

$$|S_{21}| = |S_{12}| = \sqrt{0.5} \tag{2}$$

it returns that

$$P_{upper}(z = z_0) = 0.25 \cdot P_{upper}(z = 0) \tag{3}$$

While (3) is always guaranteed by the boundary condition, it is fundamental to design the proper resistive layer length and resistivity with the aim of optimizing the power divider/combiner performance, in particular isolation and input matching for port 2 and port 3. In fact, if the resistive layer is too short for a given resistivity to dissipate all the power not coupled to port 1, this remaining power will couple to port 2 and port 3. On the other hand, if the resistive layer is too long for a given resistivity this will unnecessary increase the power divider/combiner length. Therefore, the optimum combination of resistive layer length and resistivity should dissipate exactly half of the input power.

For an ideal case where a perfect input matching for all ports and a perfect isolation between port 2 and port 3 hold, only forward waves propagate within the SIWs. In particular, the surface current density associated to the propagation within the upper SIW can be described by an exponential decay, as shown in Fig. 5:

$$J_{upper}(z) = J_{upper}(z = 0) \cdot e^{-\alpha z} \tag{4}$$

At the same time, because of the coupling between the upper and lower SIW, the surface current density associated to the propagation within the lower SIW can be also described by an exponential rising (Fig. 5):

$$J_{lower}(z) = J_{upper}(z = 0) \cdot \left(1 - e^{-\alpha z}\right) \tag{5}$$

Therefore, the total surface current density on the resistive layer can be described as follows (Fig. 5):

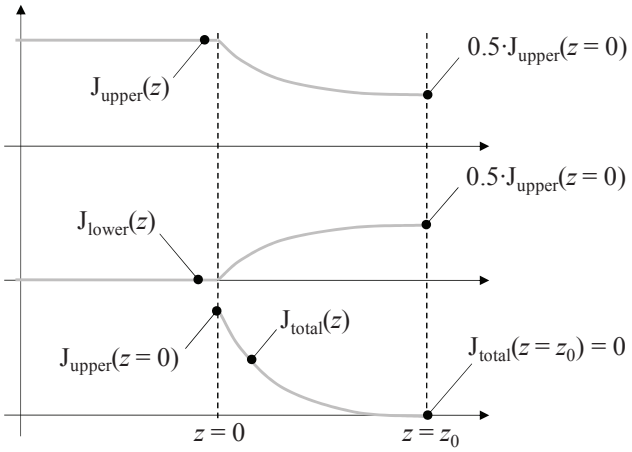


Fig. 5. Schema of the current density for the upper SIW (top), the lower SIW (centre), and the total net current density on the resistive layer (bottom) when port 2 is excited.

$$J_{total}(z) = J_{upper}(z = 0) \cdot \left(2e^{-\alpha z} - 1\right) \tag{6}$$

For the range of validity of (5) and (6):

$$0 < z < z_0 \tag{7}$$

$$z_0 = -ln(0.5)/\alpha \tag{8}$$

that guarantees $J_{upper}(z) = 0.5 \cdot J_{upper}(z = 0)$ and $J_{total}(z) = 0$ for (5) and (6), respectively, $J_{total}(z) < J_{upper}(z)$ always holds. Since the power dissipated by the resistive layer is associated to the square magnitude of the surface current density, this means that the power dissipated by the resistive layer separating the upper and lower SIW is less than the power dissipated by the same resistive layer hypothetically used to realize a single broad wall of a stand-alone SIW, where the entire surface current density would be described by (4).

This reduction factor F can be calculated as the square of the ratio between (6) and (4):

$$F(z) = \left(2 - e^{\alpha z}\right)^2 \tag{9}$$

The average value of (9) for the range of validity defined by (7) can be calculated as:

$$F_a = \frac{1}{z_0} \int_0^{z_0} F(z) dz \tag{10}$$

which returns:

$$F_a = \ln(0.5)^{-1} \cdot (4\ln(0.5) + 2.5) \sim 0.3932 \tag{11}$$

This basically means that the attenuation provided by the resistive layer used in the power divider/combiner is around 0.3932 times larger than the attenuation the same layer would provide when used as broad wall of a stand-alone SIW.

Therefore, the optimum combination of resistive layer length and resistivity can be calculated using the standard formula to calculate the attenuation constant of a normal waveguide [27], as if the resistive layer would be applied to only one of the two broad walls, and applying the reduction factor F_a:

$$P_{diss} = 8.686 \frac{R_s y}{2\eta b} \frac{1 + 2\left(\frac{f_c}{f}\right)^2 \frac{b}{a}}{\sqrt{1 - \left(\frac{f_c}{f}\right)^2}} F_a \qquad (12)$$

where P_{diss} is the total power dissipated by the resistive layer (measured in dB) R_s is the resistive layer resistivity, η is the medium impedance, a is the waveguide width, b is the waveguide height, f_c is the cut-off frequency, f is the operating frequency, and y is the resistive layer length. Please note that (12) accounts for the power losses given by the resistive card, neglecting the power losses due to the finite conductivity of the other broad wall and the side wall.

This can be considered an acceptable approximation, because for all practical cases the resistivity of the resistive layer is larger than the resistivity of the metal used for the other waveguide walls (e.g., copper, aluminum) by several orders of magnitude.

As explained above, the optimum combination of resistive layer length and resistivity is achieved when exactly half of the input power is dissipated. This means that the optimum combination is achieved when (12) returns P_{diss} = 3 dB. In particular, it is interesting to derive two different formulas for two typical cases, both calculated at the center frequency of the waveguide fundamental mode bandwidth, i.e., $f = 1.5 f_c$.

First, for a standard waveguide $a = 2b$ and the medium can be approximated as vacuum. Hence, (12) can be written as:

$$(13 R_s F_a \cdot 8.686 \cdot y) / (240\pi\sqrt{5} b) = 3 \qquad (13)$$

which yields:

$$R_s y = 113.92\, b \qquad (14)$$

with R_s measured in ohm. Second, for a standard SIW $a >> b$ and the medium is often a low loss dielectric described by the dielectric constant ε_r. Hence, (12) can be written as:

$$(3\sqrt{\varepsilon_r} R_s F_a \cdot 8.686 \cdot y) / (240\pi\sqrt{5} b) = 3 \qquad (15)$$

which yields:

$$R_s y = 493.64\, b / \sqrt{\varepsilon_r} \qquad (16)$$

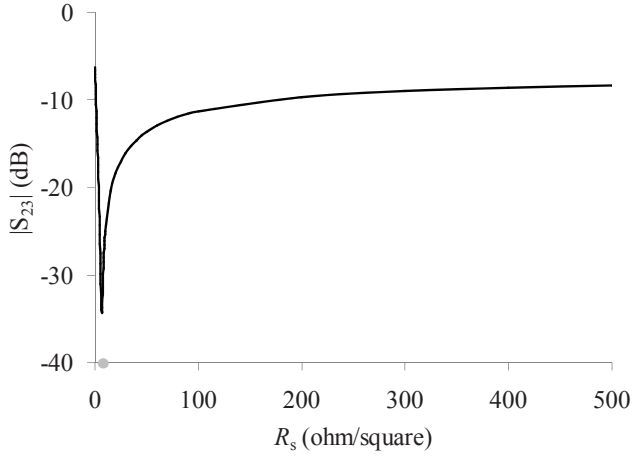
with R_s measured in ohm. It is clear that using these formulas it is possible to analytically design the optimum resistive layer length for a given layer resistivity (or viceversa), without using full-wave solvers.

III. Parametric Analysis for SIW 3-dB E-plane Power Divider/Combiners

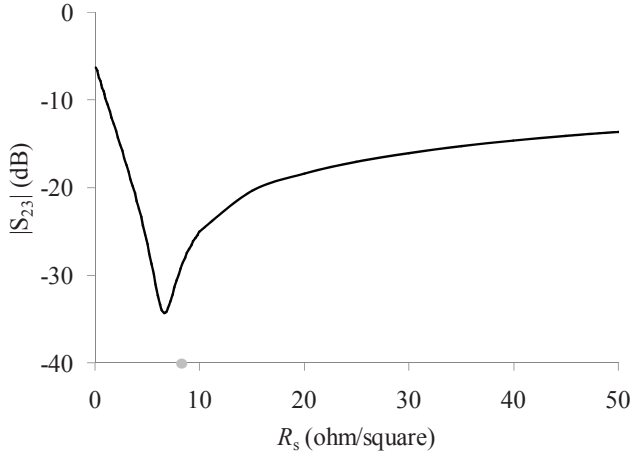
To validate the approach proposed in the previous chapter and to further discuss the performance achievable for such a type of power divider/combiner, a set of parametric analyses is carried out. Having in mind the subsequent realization of two prototypes aimed at covering the entire X-band (8–12 GHz), fabricated using either milling technique or screen-printing, the SIW is designed to have the bandwidth of a standard WR90 waveguide, with a fundamental TE_{10} mode cut-off frequency f_c = 6.56 GHz. The related SIW physical width w = 15.94 mm is determined once the SIW substrate dielectric constant, the via diameter, and the via spacing are provided [18]. For this parametric analysis ε_r = 2.2 (typical value for standard laminates), d = 1 mm (typical value for a milling-technique realization, the most stringent fabrication approach in this respect among the two approaches mentioned above), and s = 2 mm (to have side losses lower than 10^{-5} dB/mm according to [23]), respectively. Finally, to determine the right-hand part of (16), the substrate thickness is required. For this parametric analysis b = 0.25 mm, which can be considered a typical case for normal realizations.

The power divider/combiner is modeled as shown in Fig. 2 using a Finite Element Method (FEM) commercial full-wave solver, assuming no losses either from the dielectric substrate or from the metal walls and vias. The resistive layer is modeled as a rectangular-shaped resistive sheet where the surface resistance R_s and the card dimensions x and y are parameterized. With the aim of having a performance benchmark to compare different power divider/combiner layouts (i.e., with different resistive layer dimension and resistivity), the magnitude of the isolation $|S_{23}|$ between port 2 and port 3 at central frequency f = 10 GHz is used. It is interesting to observe that the magnitude of the isolation $|S_{23}|$ is a relevant indicator of the power divider/combiner performance.

Indeed, the magnitude of the reflection coefficient $|S_{11}|$ and the magnitude of the power transmission $|S_{21}|$ and $|S_{31}|$ (ideally identical to each other due to the circuit symmetry), are not affected by the resistive layer as explained previously, being $|S_{11}|$ ideally almost perfect because the E-plane structure does not perturb the field distribution, and $|S_{21}| = |S_{31}| = 0.5$ because of the symmetry. In addition, the other parameters affected by the resistive layer, i.e., the magnitude of the reflection coefficients $|S_{22}|$ and $|S_{33}|$ (ideally identical to each other due to the circuit symmetry) improve as $|S_{23}|$ improves. This can be understood according to the balanced-/unbalanced- (even-/odd-) mode analysis discussed previously in Sec. II and shown in Fig. 3. In particular, the input matching at ports 2 and 3 can be calculated as $S_{22} = S_{33} = \Gamma_{even}/2 + \Gamma_{odd}/2$ where Γ_{even} and Γ_{odd} are the reflection coefficient for the even- and odd-mode, respectively. At the same time the coupling (i.e., the inverse of isolation) is $S_{23} = \Gamma_{even}/2 - \Gamma_{odd}/2$. Due to the symmetry of the structure, in the ideal case $\Gamma_{even} = 0$. Then, Γ_{odd} is determined by the reflection at the begin and at the end of the resistive layer.



(a)



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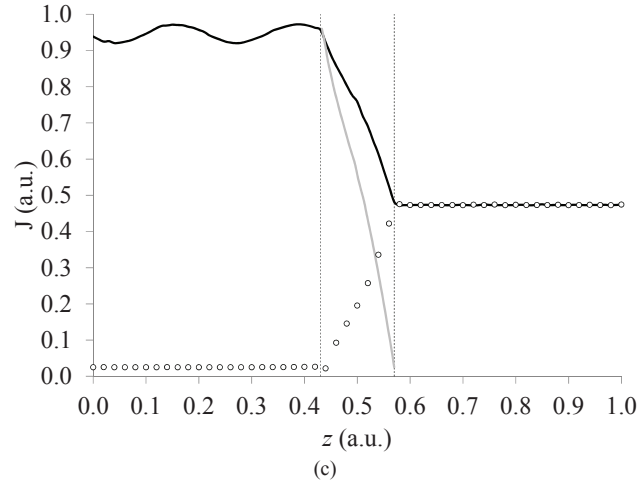

(c)

Fig. 6. (a) Magnitude of the isolation $|S_{23}|$ at 10 GHz calculated by a full-wave solver for different values of the surface resistance R_s (0–500 ohm/square) and x = 16 mm, y = 10 mm, b = 0.25 mm, ε_r = 2.2. The grey dot on the horizontal axis indicates the optimum surface resistance R_s as calculated using (16). (b) Same graph, magnified view up to 50 ohm/square. (c) Current density calculated by a full-wave solver for the upper SIW (solid black line), the lower SIW (white dots), and the total net current density on the resistive layer (solid grey line, the length of the layer is marked by vertical dashed lines) when port 2 is excited for R_s = 8.32 ohm/square, confirming the theoretical assumptions shown in Fig. 5.

If the layer is sufficiently long (as it is always the case for layers designed using the equation presented in Sec. II, in particular (14) and (16)), only the reflection at its beginning will remain. Therefore, Γ_{odd} is directly affecting both $|S_{22}|$, $|S_{33}|$, and $|S_{23}|$, and an improvement for the isolation is automatically turned into an improvement for the input matching of ports 2 and 3.

First, let us discuss a specific case, where x = 16 mm and y = 10 mm. The width x of the resistive layer is selected to cover the entire SIW width, thus providing the maximum dissipation effect. The length y is selected arbitrarily as a relevant case. Fig. 6a and 6b report the magnitude of the isolation S_{23} at 10 GHz for different values of the surface resistance R_s, ranging from 1 to 500 ohm/square. It is clear that for very low and high values of the surface resistance R_s the magnitude of the isolation S_{23} approaches the theoretical value for a lossless (i.e., with no resistive layer) power divider/combiner, i.e., -6 dB, as it can be explained according to the circuit-theory models developed for this type of junctions [28]. In fact, a very low value for the surface resistance R_s mimics a PEC wall, with no dissipation effect. On the other hand, a very high value for the surface resistance R_s mimics a PMC. In this case the resistive layer does not provide anymore a boundary condition to support the field distribution for two separate SIWs, and an immediate recombination between the field propagating in the upper SIW and the field propagating in the lower SIW is obtained.

This turns into a balanced mode, with a null net current on the resistive layer. Finally, it is interesting to observe that an optimum value for the surface resistance R_s exists, as expected. In addition, (16) provides R_s = 8.32 ohm/square as the optimum value for a resistive card of length y = 10 mm, confirming the full-wave simulations.

In addition, the full-wave simulations are also used to confirm the theoretical current densities presented in Fig. 5. As an example, Fig. 6c shows the current density for the upper and lower SIW, and for net current density on the resistive layer for the case under discussion (x = 16 mm, y = 10 mm, R_s = 8.32 ohm/square). It can be observed that apart modest ripples given by the non-ideal matching at the input ports, and non-perfect exponential curves given by the non-ideal isolation (assumption used for Fig. 5), the current densities calculated by the full-wave solver and shown in Fig. 6c can be considered a good approximation of the theoretical curves shown in Fig. 5.

The same discussion provided above for a resistive layer with length y = 10 mm can be repeated for other lengths. For all cases it is always possible to determine the optimum surface resistance R_s (i.e., the value providing the best isolation S_{23}). Fig. 7 reports the optimum surface resistance R_s for different values of the length y, ranging from 2 to 20 mm.

It is interesting to observe the good agreement between the results provided by (16) and the full-wave simulations, which are also used to calculate the value achieved for the magnitude of the isolation $|S_{23}|$. In particular, Fig. 8 reports the threshold values of the isolation $|S_{23}|$ at 10 GHz for each length y.

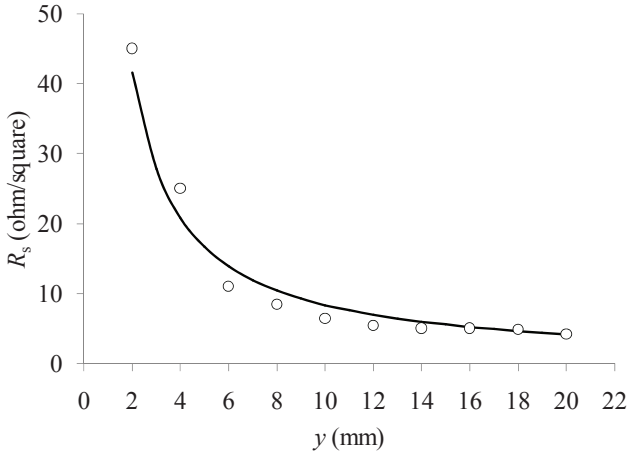

Fig. 7. Optimum surface resistance R_s calculated by a full-wave solver (white dots) and calculated using (16) (solid black line) for different values of the resistive card length y, ranging from 2 mm to 20 mm. Other parameters: x = 16 mm, b = 0.25 mm, ε_r = 2.2.

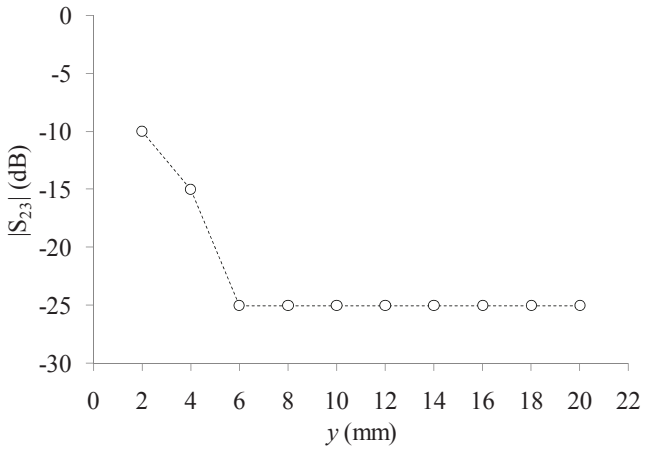

Fig. 8. Magnitude of the isolation $|S_{23}|$ at 10 GHz calculated by a full-wave solver for different values of the resistive card length y, ranging from 2 mm to 20 mm, and assuming for each length the optimum surface resistance R_s shown in Fig. 7. Other parameters: x = 16 mm, b = 0.25 mm, ε_r = 2.2.

These thresholds are defined to take into account numerical inaccuracies. In practice, instead of providing for each length y the best isolation achieved with the optimum surface resistance (e.g., 8.32 ohm/square for a length of 10 mm, providing an isolation of around -33 dB, as shown in Fig. 6) it is defined a threshold (e.g., -25 dB for all lengths equal to or longer than 6 mm) achievable by a selected range of optimum surface resistances (e.g., for y = 10 mm an isolation better than -25 dB can be obtained for a value of R_s spanning from 4.8 ohm/square to 10 ohm/square). It is evident that the isolation S_{23} deteriorates for shorter lengths, below around 6 mm. In fact, as anticipated by (16) and shown in Fig. 7, shorter lengths require higher values for the surface resistance R_s. However, this condition implies an abrupt transition from the upper and lower SIW to the single SIW, resulting into a deteriorated isolation. Indeed, for shorter lengths (2 mm and 4 mm) the best possible isolation can only achieve modest results, and the threshold is adjusted accordingly at -10 dB and -15 dB, respectively. On the other side, for lengths exceeding around 6 mm, the magnitude of the isolation S_{23} at 10 GHz is always better than -25 dB.

However, this can require low values for the surface resistance R_s, which may be not always commercially available. For this reason, an equivalent surface resistance R_s, lower than the nominal value provided by the manufacturer, can be engineered reducing the width x of the resistive layer. In particular, for a resistive layer as large as the waveguide (i.e., x = 16 mm for the example discussed in this Section) the surface resistance is obviously equal to the nominal surface resistance. Conversely, for a resistive layer smaller than the waveguide, the equivalent surface resistance R_s^E is proportional to the fraction of the waveguide covered by the resistive layer, weighted by the cosine-like (for a coordinate system centred along the waveguide axis) distribution of the fundamental TE_{10} mode:

$$R_s^E = R_s \sin(0.5\,\pi x_2/x) \tag{17}$$

where x_2 is the fraction of the waveguide covered by the resistive layer, and trigonometric and integral mathematical steps are omitted for brevity. Of course, to reduce the increased length of the resistive layer resulting from the use of an equivalent surface resistance, tapered layers can be exploited with minimal impact on the achievable results as long as the length of the taper is sufficiently smooth.

IV. Experimental Prototype

Two different manufacturing techniques are exploited to realize a prototype. The first demonstrator is fabricated according to a screen-printing approach, while the second demonstrator is fabricated according to a milling technique. Moreover, in the first demonstrator the restive layer is realized using a carbon paste, while in the second demonstrator a flexible resistive card is used. The preparatory work for both demonstrators was reported in [14, 15]. The investigation of two completely different approaches allows to highlight the advantages and disadvantages of both techniques. This is very useful to understand the potentials and limits for SIW implementation, where the ratio between the height of the waveguides and the thickness of the resistive layer poses a serious challenge in terms of manufacturing difficulties.

A. Screen-printing technique

The layout for this demonstrator is shown in Fig. 9. The width of the resistor is R_w, its length is R_l. The edge toward port 2 and port 3 is curved to improve the input matching for those ports. Fig. 10 shows in details the fabrication for the structure. The shape of the resistor is etched into the middle metallic layer (Fig. 10a) and carbon resistive paste is applied using a screen-printing process (Fig. 10b). An overlap of R_o between the paste and the metal ensures a proper electrical connection. The paste is pre-cured at 100 °C for 20 min. (Fig. 10c) In the last step the multilayer is build by adding a bonding film and a upper substrate (Fig. 10d).

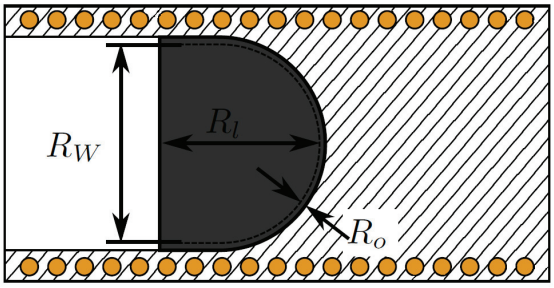

Fig. 9. Schematic of the 3-dB E-plane Power Divider/Combiner prototype realized according to the screen-printing technique, and using a carbon paste for the resistive layer.

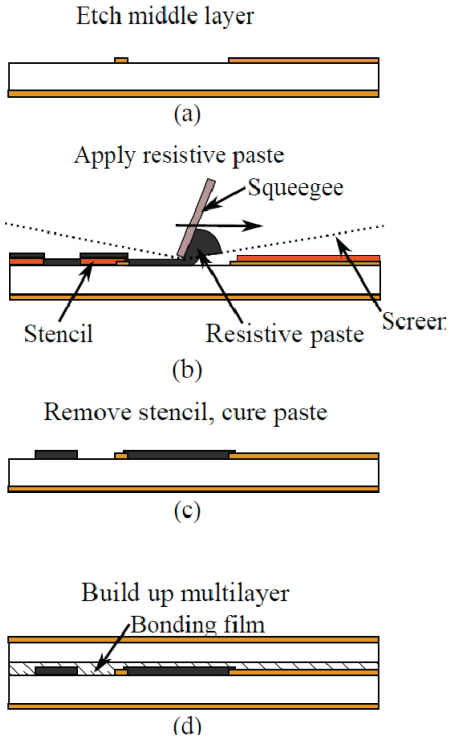

Fig. 10. Fabrication processed for the screen-printing technique, using a carbon resistive past for the resistive layer.

The multilayer is processed at up to 180 °C. At this temperature the resistor is completely cured. Finally, vias are drilled and plated to create the SIWs. The demonstrator is fabricated using Rogers RO4003 laminates (ε_r = 3.55, tanδ = 0.0027). The thickness of the laminates is b = 0.3 mm for the lower substrate and b = 0.2 mm for the upper substrate, so that, together with the 0.1 mm thick bonding film, the layer stack-up is symmetric. Rogers RO4450F bondply with $\varepsilon_r = 3.52$ and $\tan\delta = 0.004$ is used as bonding film. It is well matched to the RO4003 substrate ($\varepsilon_r = 3.55$, $\tan\delta = 0.0027$). Indeed, simulations with and without the bonding film exhibit no significant difference. The SIW width is w = 12.7 mm, the via diameter d = 0.3 mm, and the via spacing s = 0.65 mm. As explained previously, the resistor width is designed to be as large as possible (ideally matching the SIW width). To account for some fabrication constraint during the paste deposition, the final value for the resistor width is R_w = 11.8 mm. The overlap between the resistive paste and the metal layer is R_o = 0.15 mm, while the radius of curvature of the curved edge is R_w / 2 = 5.9 mm.

According to (16) the parameters above impose around R_s y = 78.6 ohm•mm. The main challenge of this fabrication technique is to control the resistive paste thickness. The uncertainty is due to the use of a squeegee to deposit the paste itself, and to the resistivity, which exhibits a large difference before and after the curing. To overcome these difficulties, an extensive experimental campaign is carried out to characterize the paste resistivity. 126 dummy resistors were fabricated. The mean surface resistance before curing is 76.7 ohm, with a standard deviation of 16.8 ohm.

The mean surface resistance after curing is 13.2 ohm with a standard deviation of 2.9 ohm. With these experimental data, and retaining R_s = 13.2 ohm as reference value, (16) returns around y = 6.0 mm for a rectangular-shaped resistive layer as large as the SIW width. This constitutes an optimum design point for the device, obtained with analytical equations. To further refine the device performance accounting the for slight difference between the resistor and the SIW width, and for the curved edge (which is added, as discussed at the beginning of this sub-Section, to further improve the input matching for ports 2 and 3 in such a way a good value can be always achieved even against the variation of the surface resistance), the resistor length is optimized using time-domain full-wave commercial software. The final value is $R_l = y$ = 7.85 mm.

The manufactured prototype is shown in Fig. 11, while its measured performance is reported in Figs. 12 to 15, including the phase unbalance between port 2 and port 3. To measure the prototype using a standard Vector Network Analyzer (VNA), SIW-to-microstrip transitions, bends, and connectors are added.

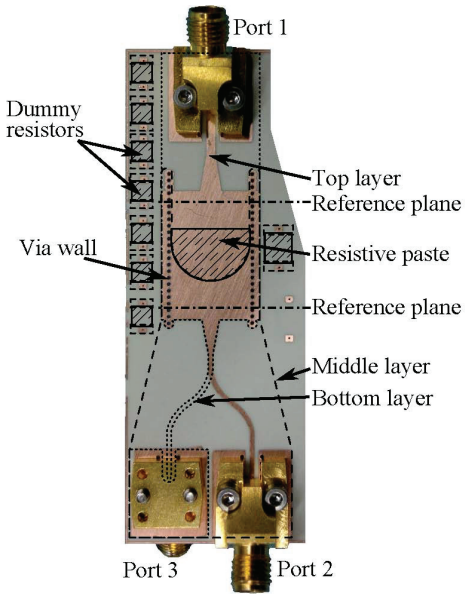

Fig. 11. Photograph of the 3-dB E-plane power divider/combiner prototype realized screen-printing of a carbon paste for the resistive layer.

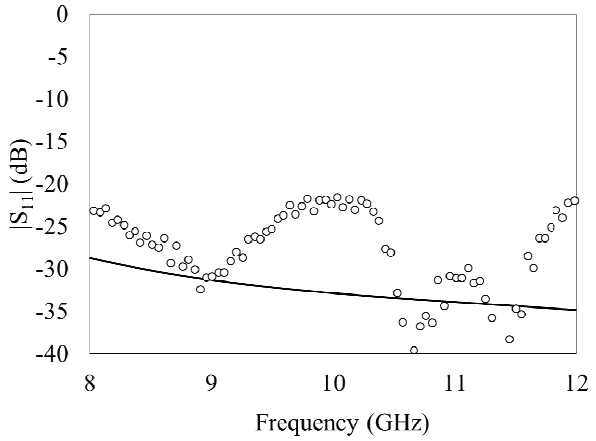

Fig. 12. $|S_{11}|$ of the prototype shown in Fig. 11. Simulated values (solid line) compared with measured values (dots).

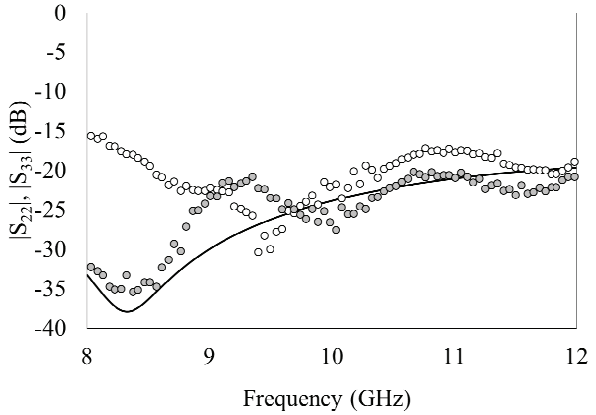

Fig. 13. $|S_{22}|$ and $|S_{33}|$ of the prototype shown in Fig. 11. Simulated values (solid line, identical for both ports) compared with measured values (white and grey dots for $|S_{22}|$ and $|S_{33}|$, respectively).

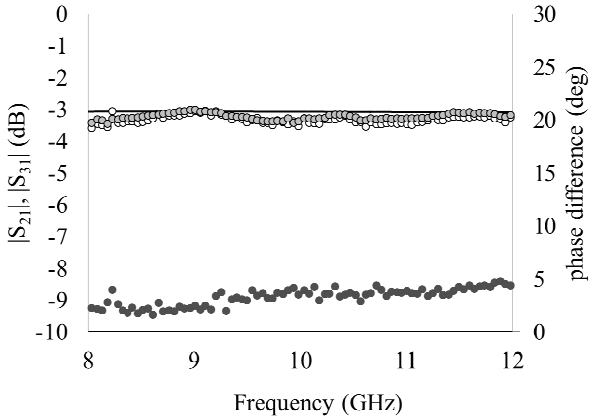

Fig. 14. $|S_{21}|$ and $|S_{31}|$ of the prototype shown in Fig. 11. Simulated values (solid line, identical for both ports) compared with measured values (white and grey dots for $|S_{21}|$ and $|S_{31}|$, respectively). In addition, the measured phase difference between S_{21} and S_{31} is also reported (black dots).

To measure the prototype using a standard Vector Network Analyzer (VNA), SIW-to-microstrip transitions, bends, and connectors are added. Their effect is eliminated using a calibration technique based on three SIW short standards of different length for each port and a reciprocal through network.

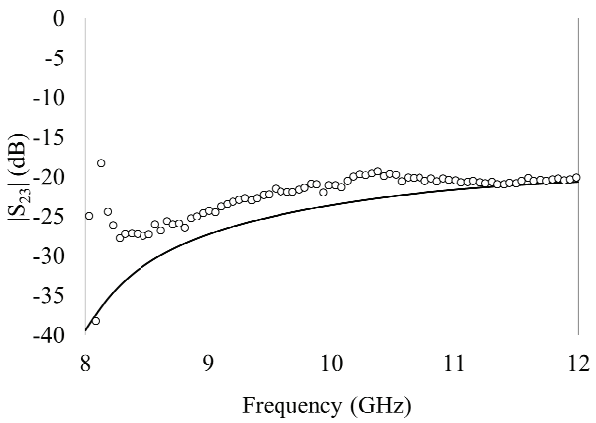

Fig. 15. $|S_{23}|$ of the prototype shown in Fig. 11. Simulated values (solid line) compared with measured values (dots).

The resulting reference planes (reciprocal distance 10 mm) for the VNA are indicated in Fig. 11, and all the simulations (which account for dielectric losses, around 0.2 dB) are also referred to those planes. Some extra buried resistors, fabricated for production-check purposes, and the middle layer are also marked in Fig 11.

B. Milling manufacturing technique

The layout for this demonstrator is shown in Fig. 16. Also in this case SIW-to-microstrip transitions are implemented, and a tapered resistive layer, discussed later in this same paragraph, is shown. The manufacturing process can be described according to the following steps, and is shown in Fig. 17. First, the upper metal layer of the upper substrate and the lower metal layer of the lower substrate are patterned using a commercial LPKF E33 milling machine, and the vias are drilled. In addition, the same milling machine is used to realize on each substrate a small inward profile, required for the subsequent installation of the microstrip-to-SMA connector. Second, the remaining metal layers (i.e., bottom metal layer of the upper substrate and upper metal layer of the lower substrate) are completely removed by chemical etching. Third, the central metal plane, made out of copper adhesive tape, and the resistive card (discussed later) are shaped using scissors and glued onto the substrate. Fourth, the two substrates are glued together and the vias are metalized using a conductive paste. The demonstrator is fabricated using a woven fiberglass PTFE laminate Taconic TLY-5 laminates (ε_r = 2.2, tanδ = 0.0009).

The thickness of the laminates is b = 0.25 mm for both the lower and the upper substrate. The SIW width is w = 15.9 mm, the via diameter d = 1 mm, and the via spacing s = 2 mm. According to (16) the parameters above impose around R_s y = 83.2 ohm•mm. The main challenge of this fabrication technique is to work with commercially-available resistive cards, and the hand-made shaping and handling of the resistive card itself. In fact, for this demonstrator, the resistive layer is realized using a flexible resistive card, provided by Florida RF™ Labs. The resistive layer (model number 73-0157) comprises a nichrome resistive film (which provides the dissipative effect, R_s = 50 ohm/square), on a mylar® flexible card (relative dielectric constant ε_r = 3.3, thickness a. 25 μm).

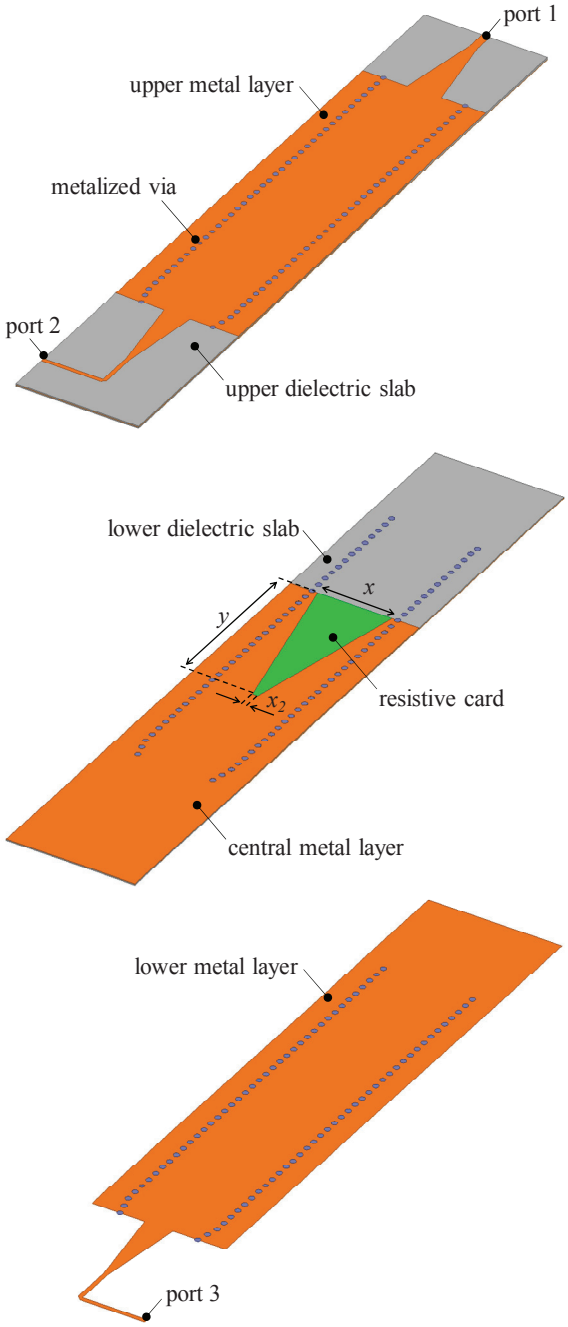

Fig. 16. Schematic of the 3-dB E-plane power divider/combiner prototype realized according to the milling manufacturing technique, and using a flexible resistive card for the resistive layer. The upper dielectric slab, with the upper metal layer (top), the lower dielectric slab with the central metal plane and the resistive card (centre), and the lower metal layer of the lower dielectric slab (bottom) are shown.

The presence of the mylar card can be neglected because its thickness is 10 times thinner than that of the Taconic TLY-5 substrate. The surface resistance (R_s = 50 ohm/square) is the lowest commercially available value. However, according to (16) this would impose for a rectangular-shaped card a length y = 1.66 mm. As described in the previous section, this would lead to a relatively poor isolation $|S_{23}|$, and according to an extrapolation from Fig. 7 this would be around -10 dB.

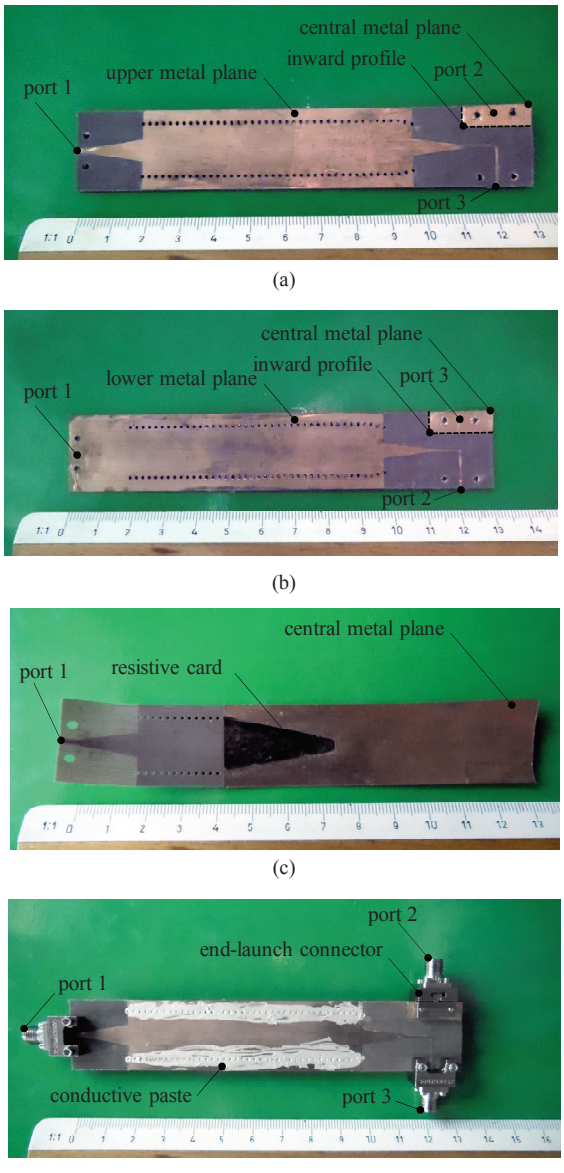

Fig. 17. Photographs of the 3-dB E-plane power dvider/combiner prototype realized according to the milling manufacturing technique, and using a flexible resistive card for the resistive layer. The photographs show (a) the upper dielectric slab, with the upper metal plane, the inward profile for port 2, and part of the central metal plane, (b) the lower dielectric slab with the lower metal plane, the inward profile for port 3, and part of the central metal plane, (c) the reverse side of the upper dielectric slab, with the central metal plane and the resistive card (vias of the central metal plane to be drilled), (d) the final prototype with all vias metalized with the conductive paste and the end-launch connectors (bottom).

In addition, such a short card would pose manufacturing problems. These problems can be overcome using a reduced-width resistive card, thus synthesizing an equivalent surface resistance, using (17). In particular, with x_2 = 3 mm an equivalent surface resistance R_s^E = 14.5 ohm/square is calculated, which in turn drives a card length of around 6 mm. However, to ease the fabrication process, which for this prototype is based on normal scissors and hand gluing, a tapered card is preferred (y = 30 mm, x = 16 mm, x_2 = 3 mm), at the cost of a longer resistive card. Thus, in this case the

optimum length is dictated by the ability of handling the card with required precision.

The performance of the manufactured prototype, measured using a standard VNA, is shown in Figs. 18 to 21, including the phase unbalance between port 2 and port 3. For this demonstrator, no internal reference planes are implemented. This is because for this prototype, realized using milling technique and flexible substrates and resistive layers, a calibration procedure based on short standards of different length and a reciprocal through network, as per the first prototype, is deemed too critical in terms of reliability. For this reason, it is preferred to use the standard calibration at the VNA ports, and to minimize the effects given by the microstrip transitions paying particular care to improve as much as possible the SIW-to-microstrip transition response.

This is achieved modifying the metal vias close the SIW-to-microstrip transitions, which are slightly shifted inward to improve port 2 and port 3 matching, as shown in Fig. 16. Furthermore, the entire prototype shown in Fig. 17 is simulated, including connectors, to provide an adequate comparison between measurements and simulations. In particular, Fig. 20 shows $|S_{21}|$ and $|S_{31}|$, where the simulated curve is compensated to take into account the insertion losses given by the end-launch connectors and the ohmic and dielectric losses of the materials used to fabricate the power divider/combiner (copper and Taconic TLY-5, respectively).

While the ohmic and dielectric losses are derived from simulations (around 1 dB), losses associated to the end-launch connectors are derived experimentally. To this aim a microstrip line of length as long as the entire power divider/combiner was simulated, fabricated, and tested. Then, the insertion losses given by the end-launch connectors are extracted by comparing simulated and measured results, and they account for around 1 dB more. Therefore, the simulated curve for $|S_{21}|$ and $|S_{31}|$ is lowered from the theoretical value given by the SIW part only, i.e., -3 dB, to the final value of around -5 dB, including microstrip sections and connectors, as shown in Fig. 20. Finally, it can be observed that the phase unbalance between port 2 and port 3, reported in Fig. 20, is below around 8 degrees, slightly worse than the value achieved for the prototype based on the screen-printing technique (around 5 degree, Fig. 14). However, this value is deteriorated by the manufacturing tolerances, which are affected by the hand-made shaping and handling of the resistive card, and by the contributions from transitions and connectors.

V. Conclusions

This paper presented the analysis, design, fabrication and measurement of a 3-dB E-plane power divider/combiner based on SIW technology and on the use of a resistive layer. In particular, an analytical formula able to return the optimum resistive layer length for a given resistivity (or vice-versa) is derived. This formula is not limited to SIW technology, and it is also applicable for a classic realization based on empty rectangular waveguides.

Two prototypes, realized according to two different manufacturing techniques, were designed to cover the entire X band from 8 GHz to 12 GHz. The realization on SIW technology is particularly suited to realize balanced amplifiers and mixers and beam-forming networks exploiting the advantages provided by the printed-circuit fabrication approach, i.e., compactness, weight and cost reduction, and integration with active stages.

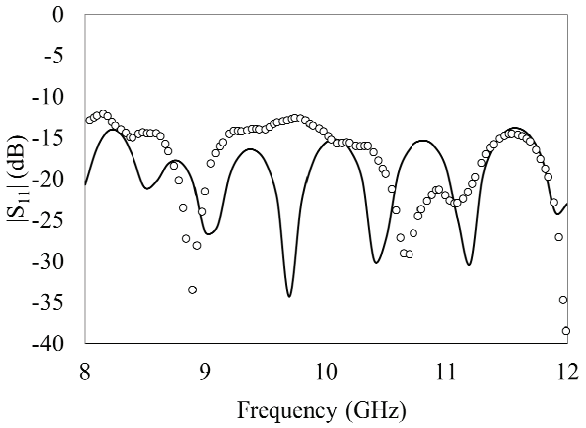

Fig. 18. $|S_{11}|$ of the prototype shown in Fig. 17. Simulated values (solid line) compared with measured values (dots).

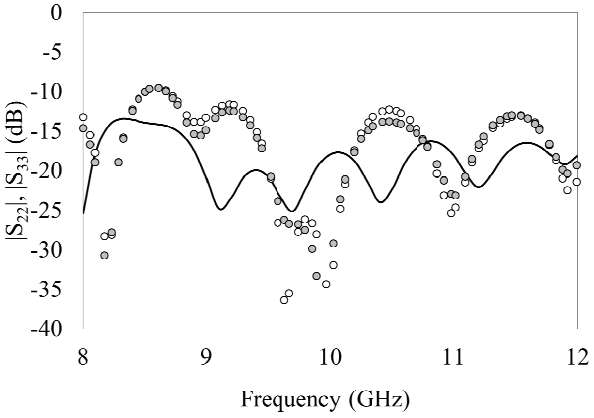

Fig. 19. $|S_{22}|$ and $|S_{33}|$ of the prototype shown in Fig. 17. Simulated values (solid line, identical for both ports) compared with measured values (white and grey dots for $|S_{22}|$ and $|S_{33}|$, respectively).

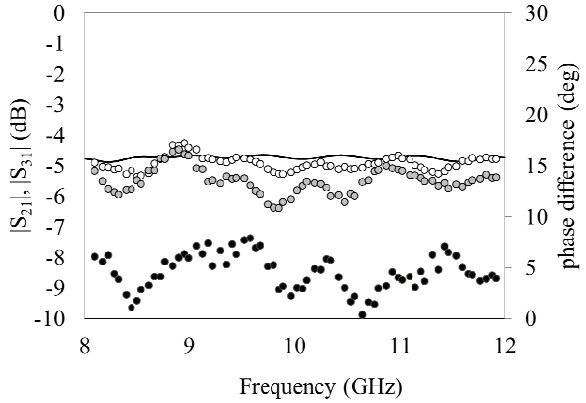

Fig. 20. $|S_{21}|$ and $|S_{31}|$ of the prototype shown in Fig. 17. Simulated values (solid line, identical for both ports) compared with measured values (white and grey dots for $|S_{21}|$ and $|S_{31}|$, respectively). In addition, the measured phase difference between S_{21} and S_{31} is also reported (black dots).

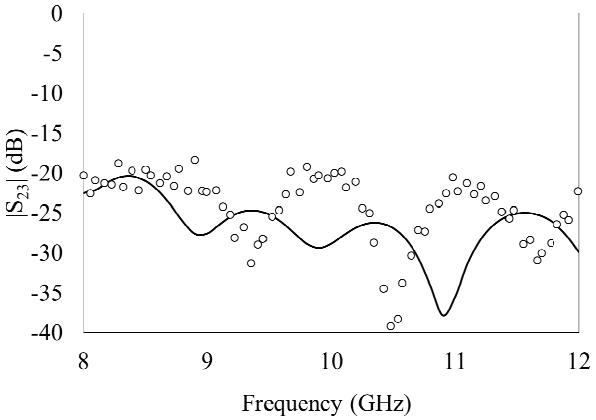

Fig. 21. $|S_{23}|$ of the prototype shown in Fig. 17. Simulated values (solid line) compared with measured values (dots).

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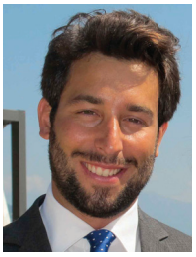
Dr. Pasian is member of the European Microwave Association (EuMA). He was a recipient of a competitive grant from the Italian Ministry of Education, University, and Research under the funding schema Scientific Independence of Young Researchers (SIR2104). He was the Technical Program Co-Chair of the European Microwave Conference 2014, the Conference Prize Committee Chair of the European Microwave Week 2014, and the Finance Chair of the IEEE International Conference on Numerical and Electromagnetic Modeling and Optimization (NEMO 2014). He is an Associate Editor of the EuMA International Journal of Microwave and Wireless Technologies.



Lorenzo Silvestri (S' 14) received the M.S. degree in electronic engineering from University of Pavia, Pavia, Italy, in 2014. He is currently pursuing his Ph.D. degree at the Department of Industrial and Information Technology, University of Pavia, Pavia, Italy.

From 2014 to 2015 he worked with a post-graduate scholarship (University of Pavia, Pavia, Italy) on the development of new components in SIW technology on innovative substrate.

Christian Rave (S'14) received the B.Sc. and M.Sc. degrees in electrical engineering from the Technische Universität Hamburg–Harburg (TUHH), Hamburg, Germany, in 2010 and 2012, respectively, where he is currently pursuing the Ph.D. degree with the Institute of High Frequency Technology.

He is currently a Research Assistant with the Institute of High Frequency Technology, TUHH. His current research interests include components and system aspects for active antennas for satellite communications.

Maurizio Bozzi (S'98–M'01–SM'12) was born in Voghera, Italy, in 1971. He received the Ph.D. degree in electronics and computer science from the University of Pavia, Pavia, Italy, in 2000.

He held research positions with various universities worldwide, including the Technische Universität Darmstadt, Germany; the Universitat de Valencia, Spain; and the École Polytechnique de Montréal, Canada. In 2002, he joined the Department of Electronics, University of Pavia, where he is currently an Associate Professor. He is also a Guest Professor of the Tianjin University (China) for the term 2015-2017.

He has authored or co-authored more than 90 journal papers and 250 conference papers. He co-edited the book Periodic Structures (Research Signpost, 2006) and co-authored the book Microstrip Lines and Slotlines (Artech House, 2013). His main research interests concern the computational electromagnetics, the substrate integrated waveguide technology, and the use of novel materials and fabrication technologies for microwave circuits (including paper, textile, and 3D printing).

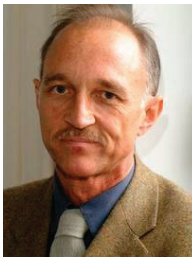
Prof. Bozzi is the 2016 Secretary of the IEEE Microwave Theory and Techniques Society (MTT-S), an elected member of the Administrative Committee of the IEEE MTT-S for the term 2017–2019, and a member of the General Assembly (GA) of the European Microwave Association (EuMA) for the term 2014–2016. He is an associate editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, the IET Electronics Letters, and the IET Microwaves, Antennas and Propagation. He was the General Conference Chair of the IEEE International Conference on Numerical Electromagnetic Modeling and Optimization, NEMO2014, Pavia, Italy, 2014, and the General Chair of the IEEE MTT-S International Microwave Workshop Series on Millimeter Wave Integration Technologies, Sitges, Spain, 2011.

He received several awards, including the 2015 Premium Award for Best Paper in IET Microwaves, Antennas & Propagation, the 2014 Premium Award for the Best Paper in Electronics Letters, the Best Young Scientist Paper Award of the XXVII General Assembly, URSI, in 2002, and the MECSA Prize of the Italian Conference on Electromagnetics (XIII RiNEm), in 2000.

Luca Perregrini (M'97-SM'12-F'16) was born in Sondrio, Italy, in 1964. He received the "Laurea" degree in Electronic Engineering and the Ph.D. in Electronics and Computer Science in 1989 and 1993, respectively.

In 1992 he joined the Faculty of Engineering of the University of Pavia, he is currently full professor of electromagnetic fields and responsible of the Microwave Laboratory. He has been the tutor of several Ph.D. students and the supervisor of many MS and BS students. He has been a visiting professor at the École Polytechnique de Montréal, Québec, Canada in 2001, 2002, 2005, and 2006.He has been responsible of many research contracts with prominent international research centers and companies. His main research interests have been focused on the development of numerical methods for electromagnetics, and the design of microwave components and antennas. He authored or co-authored more than 80 journal papers and more than 230 conference papers, six book chapters, two textbooks, and co-edited the book Periodic Structures, (Research Signpost, 2006). His current research interests include the development of numerical methods for electromagnetics, and the design of microwave components and antennas.

Prof. Perregrini served as a member of prize committees for several conferences/societies. He has been an invited speaker at many conferences, and has delivered invited seminar talks in Universities and research centers worldwide. he was a member of the General Assembly of EuMA from 2011 to 2013. He is a member of the Technical Committee MTT–15 (Microwave Field Theory) of IEEE Microwave Theory and Technique Society (MTT-S), of the Board of Directors of the European Microwave Association (EuMA), and of the Società Italiana di Elettromagnetismo (SIEm). He is Fellow of the Institute of Electrical and Electronics Engineers (IEEE), He was the co-recipient of the Best Paper Award at the 15th Mediterranean Microwave Symposium (MMS2015), of the Best Student Paper Award at the 4th European Conference on Antennas and Propagation (EuCAP 2010), and the 2nd Best Student Paper Award at the 27th Int. Review of Progress in Applied Computational Electromagnetics (ACES 2010). He is the appointed Technical Program Committee Chair of the International Microwave Workshop Series on Advanced Materials and Processes (IMWS-AMP 2017), Pavia, Italy, in 2017. He was the Technical Program Committee Chair of the IEEE MTT-S International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO2014), Pavia, Italy, in 2014, and of the European Microwave Conference, Rome, Italy, in 2014. He was Associate Editor of the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2010 to 2013 and of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES from 2013 to 2016, and Gest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES in 2015, and Gest Editor of International Journal of Microwave and Wireless Technologies in 2015. He is currently Editor in Chief of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUE. He also serves as Associate Editor of the International Journal of Microwave and Wireless Technologies (since 2011), and of IET Electronic Letters since 2015.



Arne F. Jacob (S'79–M'81–SM'02–F'09) received the Dipl.-Ing. degree in electrical engineering and the Dr.Ing. degree from the Technische Universität Braunschweig, Braunschweig, Germany, in 1979 and 1986, respectively.

He was a Fellow of the European Organization for Nuclear Research, Geneva, Switzerland, from 1986 to 1988. In 1988, he joined the Lawrence Berkeley Laboratory, University of California at Berkeley, Berkeley, CA, USA, where he was a Staff Scientist with the Accelerator and Fusion Research Division for almost three years. In 1990, he became a Professor with the Institut für Hochfrequenztechnik, Technische Universität Braunschweig.

Since 2004, he has been a Professor with the Technische Universität Hamburg–Harburg, Hamburg, Germany, where he heads the Institute of High Frequency Technology. His current research interests include the design, packaging, and application of integrated (sub-)systems up to millimeter frequencies and the characterization of complex materials.

Kamal K. Samanta graduated in Science (Phy Hons) and Engineering (ECE) before his double Masters in Management (R&D) and Technology (ECE) from the University of Calcutta, which followed his PhD degree in Microwave Eng. from the University of Leeds, England. For more than two decades, he has been extensively involved in a wide range of multidisciplinary industrial R&D activities starting from novel microwave material and fabrication process to advanced devices, circuits and systems, covering frequency MHz to 200 GHz and power from µW (MMICs) to Megawatts (SSPAs). He has produced many innovative and the world's first industrial solutions. His roles have included that of Senior Principal/Lead R&D - Engineer, -Scientist and -Consultant. The organisations he has worked for include Thales Aerospace (for Radar/EW/ESM systems); European Aeronautics Defence and Space (EADS) Astrium (presently Airbus), UK; Indian Space Research Organization (satellite payload ckts); IPR, Dept. of Atomic Energy, India (2 MW 64 phased array); RFMD and Filtronics Compound Semiconductor, UK (MMIC radios,

PAs); and Milmega UK (GaN PA MMICs, systems). Presently he is working for Sony Europe as a Consultant for advanced mmW R&D and Technical Lead for 3D low cost front-end modules for next generation wireless comm., and a visiting researcher at the University of Leeds, UK. Dr. Samanta is highly motivated to innovative multidisciplinary industrial R & D, and in the field of advanced multilayer/3D mmW integration and packaging, and very high power amplifier, recently, he has delivered more than 45 invited special/keynote talks in IEEE conferences.

Dr. Samanta was the recipient of the Commonwealth Fellowship (2003), the Best International Researcher Award (2005) and the Engineering Excellence Award from the IET (IEE) in London, (2005). He sits on the IEEE MTT-S Technical Committees (TC) -5, 6, 8 & 12 (on High Power/PA, MMIC/MCM, passives & filters, and packaging). Dr. Samanta is the Guest Editor for the Focus Issues of IEEE Microwave Magazine on 'Heterogeneous Integration' and on 'mmW MCM'. He has been serving as an Editor for the IEEE Microwave and Wireless Components Letters, and for the IET Microwave Antennas and Propagation.