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Insights into Silicon Photonics Mach-Zehnder-based Optical Transmitter Architectures

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Abstract — Mach-Zehnder-based modulator architectures lend themselves to the realization of high data rate Silicon Photonics transmitters. In this work the challenges set by the integration of such devices on silicon are analyzed in depth. The two main alternative electronic driver architectures, namely multistage and travelling wave, are compared with focus to power efficiency. This is in fact a key parameter when considering the stringent requirements of standard module form factors. A 25Gbps multistage and a 56Gbps travelling wave modulator have been realized. Each electro-optical transmitter is obtained by the 3D assembly of an electronic IC on top of a photonic IC through copper pillars. STMicroelectronics PIC25G Silicon Photonics platform has been adopted for the fabrication of optical devices, while 65nm CMOS and 55nm BiCMOS technologies are exploited to realize the electronic drivers. A 30% better power efficiency compared to Silicon Photonics state-of-the-art at similar data rates and comparable extinction ratio performance has been demonstrated in both cases. Since packaging is also a crucial aspect for Silicon Photonics high volume production, experiments on bare dice as well as on packaged chips are reported.

I. Introduction

Silicon Photonics is emerging as a promising technology enabling miniaturization and cost reduction of electro-optical devices. These advantages can be exploited in various applications including but not limited to data communications, commercial video and consumer electronics, sensing, lab on chip and gyroscopes [1]. Nowadays the evolution of this technology is mainly driven by the fast growing market of data centers. The continuous increase of Internet data traffic volume in fact mandates the development of power efficient and cost effective high

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speed interconnects to overcome the attenuation and crosstalk limits of metal links [2]. Optical communications are now expanding within data centers, where optoelectronic modules act as interfaces between the electrical and the optical domains to transmit data between switches and servers. Such modules are built with a large number of discrete optical and optoelectronic components plus few electronic ICs and they are challenging with regard to size, cost, and power consumption. In this scenario, Silicon Photonics is attractive for large-scale industrialization of low-cost miniaturized optical transceivers addressing short/medium-reach optical communications up to a few kilometers [3].

Silicon Photonics based transceivers can be realized by monolithic integration of optical devices together with electronic components. This solution suffers however from limited flexibility and scalability. Thick SOI and BOX, generally not included in standard advanced CMOS technologies, are in fact required to obtain low-loss propagation for the optical signal [3]. This in turn requires the development of dedicated CMOS technologies, creating either local photonic substrates on standard electronic platforms or integrating electronic devices on photonic substrates. In both cases the realization cost increases and the performance of the electronic circuits are not necessarily optimized. A 3D-integrated solution allows instead the use of separate Electronic Integrated Circuits (EICs). This maximizes the EIC design flexibility since the electronic technology can be selected according to the target application. Minimal performance degradation compared to a monolithically integrated solution is obtained realizing the 3D dice assembly through copper pillars. This recent bumping solution, already in high volume production, in fact ensures fine pitch at low cost. The 3D structure has to be finally assembled on the substrate of the optical module. Low cost electro-optical assembly techniques maximizing signal integrity are key and alternative solutions are currently under investigation [3].

This paper focuses the transmitter portion of the integrated optical transceiver, extremely

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challenging due to the power efficiency required by standard modules' form factors. Different approaches for the design of Mach-Zehnder modulators (MZMs) are analyzed and compared in the following. In particular, the analysis demonstrates that a multistage architecture adopting rail-to-rail inverter-based CMOS drivers allows maximum extinction ratio (ER). However, as data rate increases, inverter-based CMOS driving is not fast enough. Travelling wave architectures adopting CML/ECL driving are then preferred, even if at the cost of an ER reduction caused by electrical propagation losses and bandwidth limitations of silicon integrated transmission lines. In this work, alternative design choices relying on both CMOS and CML/ECL architectures are compared. STMicroelectronics 3D-compatible Silicon Photonics platform (PIC25G), implementing only optical devices in the front-end of line (FEOL), has been used for the photonic section [4]. A 25Gbps transmitter based on a multistage architecture and achieving an ER higher than 4dB [5] is presented together with a 56Gbps solution based on a travelling wave architecture and achieving an ER of 2.5dB [6]. The comparison between theoretical analysis, simulations and measurements is reported at probe-level and on testboard with packaged samples. The paper is organized as follows: an overview of Silicon Photonics modulators is provided in Section II together with the basic operation principles of MZMs. Sections III and IV introduce the two main alternative Silicon Photonics MZM driving architectures for high rate communications: multistage and travelling wave. Section V compares the power efficiencies of the two architectures. Section VI presents the design of the demonstrators and the experimental results, providing details about the package and testboard. Finally, section VII draws the conclusions.

II. Overview of Silicon Photonics modulators

A modulated optical signal can be generated either by direct modulation of the laser cavity or by modulation of the laser output through an external device. While direct modulation is advantageous in terms of simplicity and compactness, external modulation provides and optical transmitted signal with higher spectral purity [7]. Furthermore, in parallel applications with

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several lanes operating at the same wavelength (e.g. 100G-PSM4) external modulation allows using a single continuous-wave laser source to serve more than one lane. This simplifies the electro-optical transmitter architecture and reduces the overall link power consumption. Two alternative physical effects can be exploited for the realization of external modulators: electro-absorption and electro-refraction [8]. Electro-absorption consists in the variation of the material absorption coefficient due to the application of an external electric field. Intensity modulation of the carrier can be performed through this effect. However, electro-absorption modulators do not lend themselves to the realization of silicon integrated transmitters. In fact, since the primary electric field effects exploited to obtain electro-absorption are weak in silicon, their realization requires hybrid integration of III-V materials [9] or use of Ge-based modulators [10]. While these solutions allow shortening the devices down to few tens of microns, the electro-absorption effect is intrinsically wavelength and temperature dependent [10]. This limits the operating wavelength range and requires the use of a temperature control to achieve repeatable performance. Electro-refraction instead consists in the variation of the material refractive index through the application of an external electric field. Ring resonators and balanced Mach-Zehnder interferometers are the most exploited architectures to achieve intensity modulation of light by varying its phase through refractive index changes. Ring resonator modulators have been recently analyzed in depth for the realization of miniaturized silicon modulators [11-13]. However, they are very susceptible to operating condition variations, in particular temperature, thus requiring accurate thermal controllers [14]. This not only affects the overall power budget of electro-optical transmitters but also poses reliability and yield issues. Furthermore, achieving moderate speeds of 20-25Gbps with wide open and symmetric eye diagrams is still critical [12,13]. MZMs are the most mature solution for the realization of reliable externally modulated Silicon Photonics transmitters providing high yield and well controlled performance. When implemented in a push-pull configuration, MZMs

allow achieving optimal chirp performance thus reducing dispersion [7]. Furthermore, MZMs can operate over a much wider optical bandwidth than ring resonator modulators without requiring any device tuning. Finally, current generation MZMs already show bandwidths larger than 40GHz [4], paving the way to the next generation of optical modules.

A MZM consists of a balanced Mach-Zehnder interferometer. The incoming optical signal is split into two nominally identical optical paths and recombined after an induced phase shift difference $\Delta\varphi$ between the two paths (Fig. 1a and 1b). The generated output power P_{out}, neglecting second order effects such as unbalance in the two arms' losses and deviation from the 3dB condition of the directional couplers, can be derived from [7] and it is given by:

$$P_{out} = P_{max} \sin^2\left(\frac{\Delta\varphi}{2}\right) \tag{1}$$

$$\overline{P_{out}} = P_{max} \cos^2\left(\frac{\Delta\varphi}{2}\right) \tag{2}$$

The maximum output optical power P_{max} is determined by the continuous wave input power and by the optical propagation losses along the MZM. The phase-shift difference $\Delta\varphi=\Delta\varphi_{mod}+\Delta\varphi_0$ is realized by means of a static phase shift $\Delta\varphi_0$ plus a variable component $\Delta\varphi_{mod}$ obtained through a high speed modulating driving signal V_{drive} (Fig. 1a). The static phase shift difference $\Delta\varphi_0$ is introduced by means of a Low Speed Phase Modulator (LSPM) within the interferometer. The operating point is set around $\Delta\varphi=\pi/2$, maximizing the Optical Modulation Amplitude (OMA) which is defined as follows:

$$OMA = P_1 - P_0 \tag{3}$$

The varying phase difference $\Delta\varphi_{mod}$ depends upon V_{drive} and L_{HSPM} according to:

$$\Delta\varphi_{mod} = \pi \frac{V_{drive} L_{HSPM}}{V_\pi L_\pi} \tag{4}$$

where the High-Speed Phase Modulator (HSPM) $V_\pi L_\pi$ is set by the technology and represents

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the product between the voltage and the geometrical length necessary to achieve a π phase shift. The driver supply voltage is limited by transistor reliability rules in integrated realizations, setting then a limit to the maximum driving voltage. Dual-drive push-pull configurations (Fig. 1b) are generally adopted to halve the modulator length compared to single-drive, for the same driving voltage amplitude and for a given Extinction Ratio (ER), defined as:

$$ER = \frac{P_1}{P_0}. \quad (5)$$

The ER can then be improved by increasing either the driving voltage swing or the modulator length, which in turn increases P_1 and reduces P_0, as shown in Fig. 1c for a push-pull configuration.

In Silicon Photonics, the plasma dispersion effect is usually exploited to obtain high-speed phase modulation [14]. The most widely adopted modulator devices are carrier depletion P-N junctions (see the inset of Fig. 1a). The relatively low modulation efficiency of Silicon Photonics carrier depletion HSPMs generally requires modulator lengths in the range of few millimeters to achieve the desired ER, featuring capacitances in the range of several hundreds of femto Farad. The simplest driving architecture, consisting of a lumped stage driving the junction nonlinear capacitive load, is thus not feasible at bit rates in the range of tens of Gbps and distributed structures similar to those adopted in RF design are needed. In the next sections alternative driving topologies are then investigated.

III. Multistage MZM architectures

Multistage architectures, where the modulator electrodes are split into several sections driven by dedicated stages, lend themselves to high data rate operation. Each modulator section can be modelled as a lumped capacitive load and can be driven rail-to-rail at high speed and low power by means of CMOS inverter structures. This solution optimizes the driving efficiency and at the same time maximizes the achievable ER. The highest available voltage is in fact

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applied all along the electrode length. According to equations (1) to (5) and neglecting ISI effects, the achievable ER and OMA change as a function of HSPM length is shown in Fig.2. A push-pull MZM realized with first generation PIC25G HSPMs (0.55dB/mm insertion loss and 10.5°/mm phase shift at 2.5V, corresponding to $V_\pi L_\pi$=40V·mm [4]) and stacked CMOS inverters operating under a 2.5V supply, as adopted in the demonstrator described in Section VI.A, is considered. The reported OMA values have been normalized to the maximum optical power value achievable in case of no optical insertion loss within the MZM. While the ER monotonically increases with the MZM length for $0<\Delta\phi/2<\pi/2$, an optimum length exists maximizing the transmitted OMA. The OMA versus L_{HSPM} is in fact not monotonic due to the impact of the increasing optical losses. In Fig.2 the expected performance of the first generation HSPMs is compared to the second generation, which provides HSPMs featuring 0.6dB/mm insertion loss and 17.2°/mm phase shift at 2.5V, corresponding to $V_\pi L_\pi$=25V·mm [3]. The advantages of the latter in terms of both ER and OMA are evident. Second generation lends itself to low supply voltage operation for enhanced power efficiency.

Given the total modulator length, which is set by the desired ER once the available driving voltage is determined, a proper section length must be selected. The upper limit is set by the modulator section self-resonance frequency. This has to be kept higher than the signal bandwidth of interest. Simulation examples for sections from 250µm to 1mm are reported in Fig.3, considering first generation PIC25G HSPMs and associated electrodes at reverse bias voltage of 1.25V. Section lengths shorter than 500 µm are mandatory at 50Gbps and beyond. Longer lengths can be selected for lower data rates. Instead, the lower length limit is mainly determined by the structure complexity and associated layout. The number of modulation sections must thus be large enough to reduce each capacitive load ensuring the desired driving speed, i.e. the electrical rise and fall times, without compromising the overall complexity.

To minimize the rise and fall times of modulated optical outputs the several electrical driving

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signals must be properly synchronized with each other, matching the group delay of the optical wave propagating in the waveguide. This is key especially at very high data rates. Fig.4 shows the degradation of the optical rise and fall times in an ideal 3mm-long PIC25G multistage modulator with 500μm-long and 250μm-long sections as a function of the delay mismatch between the electrical and the optical signals' group delay. When perfect matching is achieved, rise and fall times are minimum. Higher transition times instead result in case of mismatches. Simulated eye diagrams are also shown at 25Gbps for 500μm-long and at 50Gbps for 250μm-long sections, demonstrating that delay matching is not critical at 25Gbps but becomes more and more of concern with increasing data rates, eventually requiring precision delay control loops.

A 25Gbps transmitter relying upon a multistage architecture, exploiting the above techniques and realized in PIC25G and 65nm CMOS technologies, is described in Section VI.A.

IV. Travelling wave MZM architectures

A multistage architecture adopting CMOS stages for rail-to-rail driving is the optimal choice to maximize the ER, but the maximum achievable data rate is intrinsically limited by the transistor speed. As data rate increases, a travelling wave MZM architecture is preferred. In this realization, like in discrete photonics [7], the electrode of each MZM arm is realized as a transmission line as shown in Fig. 5a for a push-pull architecture. CML or ECL stages generally drive the load impedance realized by the terminated electrode transmission line. However, differently from discrete photonics realizations, Silicon Photonics suffers from electrical propagation losses and bandwidth limitations of integrated transmission lines. Moreover the HSPM sections that are placed farther away from the driver contribute less to phase modulation, while increasing optical attenuation and consuming area. As a consequence, for a given driving voltage, which is mainly set by the technology's Safe Operating Area (SOA) constraints, an optimum length exists maximizing transmitted OMA that is different from the

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optimum found for the multistage architecture. The ER instead monotonically increases with the MZM length for $0<\Delta\phi/2<\pi/2$. The electrical propagation losses can be minimized by periodically loading the electrode transmission line with short HSPM sections (Fig. 5b) to isolate longitudinal current flow in the metal electrodes [15,16]. In this way lossy propagation through p-n junctions is avoided. The resulting filling ratio can be optimized to minimize optical rise and fall times by ensuring matching between the delay of the electrical wave propagating in the electrodes and the delay of the optical wave propagating in the waveguide.

To derive the OMA and ER curves neglecting ISI effects, equations (1) to (5) can be applied also in the case of travelling wave modulators. However, in the travelling wave architecture not all the sections along the MZM arm length equally contribute to the phase shift. The un-doped parts between one HSPM section and the other give in fact no contribution. Moreover, the provided phase shift reduces along the MZM arm as the voltage decays from its initial value V_{drive} due to the electrical propagation losses. To keep these effects into account, the concept of effective length L_{eff} can be introduced. L_{eff} is the length of a HSPM that, driven with a voltage V_{drive} assumed constant along its length, provides a phase shift equal to that of the analyzed HSPM. The effective length is thus defined by the following equation:

$$V_{drive}L_{eff} = \int_0^{L_{HSPM}} V_{drive}e^{-\alpha z} \sum_{n=-\infty}^{\infty} \mathrm{rect}\left(\frac{z-nL}{\delta L}-\frac{1}{2}\right)dz \qquad (6)$$

where z is the longitudinal dimension of the HSPM, L_{HSPM} is the entire geometrical length of the HSPM, α is the voltage attenuation constant and the summation represents the periodic loading of the electrode transmission line of period L and fill in factor δ. L_{eff} can thus be used in equations (1) to (5) to derive ER and OMA performance for the travelling wave modulators.

Fig. 6 shows the ER and the OMA as a function of the HSPM length. A push-pull MZM realized with first generation PIC25G HSPMs is considered together with a driving architecture relying upon ECL pairs under a 2.8V supply implementing equalization techniques. A filling

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ratio of 60% and electrical propagation losses of ~3dB/mm at Nyquist frequency (28GHz for 56Gbps) are assumed. While the travelling wave architecture enables operation at higher data rates than the multistage one, the maximum achievable OMA is lower due to the lower driving voltage and the increased electrical propagation losses. In Fig.6, the expected performance of the first generation HSPMs is compared to the second generation ones. For the latter, a filling ratio of 80% and ~3dB/mm of propagation losses are assumed. Extinction ratio values in the range of 5dB, suitable for most standards for optical modules, are achievable using the most recent HSPMs.

A 56Gbps transmitter relying upon a travelling wave architecture, exploiting the above techniques and realized in PIC25G and 55nm BiCMOS technologies, will be described in Section VI.B.

V. MULTISTAGE VS. TRAVELLING WAVE MZM ARCHITECTURES

The analysis carried out in the previous paragraphs show that multistage architectures based on CMOS drivers are preferred in applications requiring large ER values, but they are limited in speed. Travelling wave architectures based on CML/ECL drivers are instead preferred at higher rates, but they do not ensure large ER values due to the limited voltage swing and the losses of the integrated transmission line.

In applications with intermediate data rates and requiring moderate ER values, the choice between the two architectures is driven by power consumption considerations. Assuming pseudorandom bit streams with rise and fall times negligible with respect to the bit duration T_b, the dynamic power for each arm of the multistage and travelling wave architectures, $P_{dyn,MS}$ and $P_{dyn,TW}$ respectively, is given by:

$$P_{dyn,MS} = \frac{1}{4} \cdot \frac{1}{T_b} \cdot C \cdot V_{MS}^2 \tag{7}$$

$$P_{dyn,TW} = \mathrm{V}_{AVG} \cdot \mathrm{I}_{AVG} = \frac{1}{4} \cdot \frac{V_{TW}^2}{R} \tag{8}$$

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where $1/T_b$ is the bit rate, C is the average capacitance value across voltage for the whole HSPM, R is the characteristic impedance of the travelling wave electrode, and V_{MS} and V_{TW} are respectively the driving voltages for the multistage and the travelling wave solution. The dynamic power is proportional to the total HSPM length through the capacitance value in the case of a multistage driving, while in the case of a travelling wave driving it is independent from this parameter. Considering also the driver efficiencies η_{MS} and η_{TW}, defined as the ratio between the dynamic power reported in equations (7) and (8) versus the total dissipated power, the powers dissipated by the multistage and travelling wave architecture, P_{MS} and P_{TW} respectively, are given by:

$$P_{MS} = \frac{1}{\eta_{MS}} \cdot \frac{1}{4} \cdot \frac{1}{T_b} \cdot C \cdot V_{MS}^2 \tag{9}$$

$$P_{TW} = \frac{1}{\eta_{TW}} \cdot \frac{1}{4} \cdot \frac{V_{TW}^2}{R} \tag{10}$$

The driver efficiencies η_{MS} and η_{TW} take into account both driver non idealities, such as the finite slope of driving edges, and the power dissipated in the pre-driving stages.

The resulting transmitter power efficiencies, defined as the ratio between the power consumption and the bit rate and expressed in pJ/bit, are plotted as a function of the bit rate in Fig.7. The transmitter power efficiency is independent of the bit rate for the multistage architecture, while it improves proportionally for the travelling wave solution. The crossing point B_0, given by:

$$B_0 = \frac{\eta_{MS}}{\eta_{TW}} \cdot \frac{1}{CR} \cdot \left(\frac{V_{TW}}{V_{MS}}\right)^2 \tag{11}$$

identifies the bit rate beyond which travelling wave architectures are the preferred choice. Due to its dependence on η_{MS} and η_{TW}, the absolute value of B_0 depends on the specific design implementation. As an example, assuming a 3mm-long HSPM realized in first generation

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PIC25G technology featuring ~300fF/mm [4], a 50Ω sizing of the travelling wave transmission line, driver efficiencies of ~20% for multistage and of ~15% for travelling wave and comparable voltage swings, a multistage architecture is advantageous in terms of power consumption at bit rates lower than 30Gbps while a travelling wave solution is preferred beyond. Power consumption advantages of a multistage architecture making use of CMOS drivers versus a travelling wave architecture using CML/ECL drivers become even more evident as operating rate decreases. This makes multistage architecture attractive for multi-standard operation needing backward compatibility with existing standards.

VI. Demonstrator Design and Implementation

One 25Gbps and one 56Gbps transmitters have been designed and characterized, comparing measurement results with electro-optical co-simulations. Both transmitters have been realized using first generation PIC25G technology and operate at 1310nm wavelength. The EIC has been 3D integrated on top of the PIC by means of 50μm-pitch and 20μm-diameter copper pillars, minimizing the interconnection parasitic capacitance. The realized demonstrators comprise the full Silicon Photonics transmitters, integrating I/O grating couplers, waveguides, HSPMs, 3dB-couplers and LSPMs. The adopted HSPMs feature 10.5°/mm phase shift under a 2.5V reverse biasing corresponding to a $V_\pi L_\pi$ of 40Vmm and a specific capacitance of ~300fF/mm [4].

A. 25Gbps transmitter based on a multistage MZM

As demonstrated in section V, at a moderate data rate of 25Gbps a multistage approach is preferable to optimize the driving efficiency and maximize the achievable ER. In this section, a demonstrator comprising a dual drive push-pull MZM and a 65nm CMOS driver operating at 2.5V supply and adopting a modular architecture as described in [5] is presented. With a rail-to-rail driving, an ER of 5dB is ideally achieved with an HSPM length of 3 mm when the MZM is biased at quadrature point (Fig. 2). To ensure a large enough self-resonance frequency of the

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HSPM sections and to guarantee the desired electrical rise and fall times, the 3mm-long electrodes have been segmented into 500μm-long sections, each featuring a 52GHz self-resonance frequency and a 150fF capacitance. The circuit schematics of the driver are reported in Fig. 8. Each driving stage is based on stacked CMOS inverters driven by two out-of-phase DC-shifted synchronous input signals with the same amplitude. This is realized in order to achieve the desired 25Gbps, 2.5V voltage swing without violating MOS transistor SOAs while ensuring proper reverse bias of the HSPM p-n junctions. Operation during charge and discharge phases is detailed in Fig. 8. DC-shifted signals at driving stage inputs, for push-pull driving of two HSPM sections, are generated by means of boost capacitors $C_{1\text{-}2}$ of 350fF and CMOS latch. CMOS latch allows proper operation also in the presence of long periodicity PRBSs and at lower data rate by avoiding undesired discharge of boost capacitors. No perceptible phase shift appears between nodes L' and H'. The DC shifter is enabled by the dedicated awake signals (AWK-*). Pre-charging mos ensure a well-defined state of the latch at startup.

Fig. 9 shows the photomicrograph of the demonstrator. The transmitter core occupies 0.6mm^2 and dissipates 275mW at 25Gbps. Lower data rates are also supported with a dissipation of 75mW at 10Gbps in low power mode and with less than 0.5dB penalty on the ER [5]. Maximum OMA is achieved at quadrature point, while the ER can be traded with the OMA by proper LSPM setting. The measurement setup is shown in Fig. 10. Eye diagram measurements have been performed by directly accessing input pads via RF probes with 2^7-1 Non-Return-to-Zero (NRZ) pseudo-random bit sequences (PRBS7). The CW laser power delivered to the input grating coupler is close to 13dBm. The optical eye diagram at 25Gbps with the MZM operated at quadrature point is measured with the oscilloscope standard triggering, and compared to simulations in Fig. 11. Simulations have been performed by co-simulating electronic with photonic devices and show a very good agreement with the measurements. An ER of 4dB has been achieved. This value can be increased up to 6dB by a different setting of the MZM

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operating point, while maintaining the OMA penalty below 25% and the eye diagram crossing point beyond 45%. Tab. I compares the results of the demonstrator with those of recently published electro-optical transmitters based on carrier depletion MZMs and operating at comparable data rates [17,18]. This work demonstrates a state-of-the-art ER of up to 6dB with 30% better transmitter power efficiency than published data, demonstrating the effectiveness of the proposed multistage approach for 25Gbps operation. CMOS drivers in 65nm CMOS technology, however, do not lend themselves to efficient operation at higher data rates and travelling wave architectures are to be preferred. This is demonstrated in next section for 56Gbps operation.

B. 56Gbps transmitter based on a travelling wave MZM

In this section, a demonstrator addressing 50GBaud operation at moderate power consumption is presented. The effect of electrical propagation losses of integrated transmission lines is counteracted by means of optimized equalization, as described in [6]. The demonstrator comprises a PIC25G dual-drive push-pull MZM and a 55nm BiCMOS driver. The differential electrode of each MZM arm has been realized as a bifilar transmission line to maximize its characteristic impedance, thus reducing the current supplied by the driver and minimizing the power consumption. The bifilar line has been periodically loaded with short HSPM sections with a 60% filling ratio. The transmission line, including reverse biased HSPM sections, features a simulated characteristic impedance of ~60Ω and an attenuation of ~3dB/mm at 28GHz. A 5.34mm modulator length has been selected, realizing an ER of 2.5dB at 1.6Vppd driving voltage.

Simplified schematics of the three-stage driver are shown in Fig. 12. An emitter follower, DC coupled to the previous stage and stacked on top of an ECL pair, realizes the driving stage. This achieves a 1.6Vppd output signal without violating SOA recommendations. To increase the driving efficiency at high frequency, the ECL pair is AC coupled to the previous stage to

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operate mainly during signal transitions, providing fast current switching. In the pre-driving stage, two ECL pairs with different passive input coupling networks and shared loads allow implementing both VGA and equalization functions. This solution is effective also under large signals. SOA issues are avoided using a cascode as shared load for the ECL pairs. Shunt peaking has been implemented at the pre-driving stage output to further reduce rise and fall times. The input stage is based on an emitter follower structure with input capacitance smaller than the pre-driving stage, ensuring wideband input matching (|S11|<-10dB up to 32GHz).

Fig. 13 shows the photomicrograph of the 3D assembly, which includes the proposed 0.38mm^2 driver core together with additional test structures. The power consumption at 56Gbps is 300mW, corresponding to a transmitter power efficiency of 5.4pJ/bit. The measurement setup is shown in Fig. 10. The eye diagram measurements have been performed by directly accessing input pads via RF probes with Non-Return-to-Zero (NRZ) 2^{31}-1 pseudo-random bit sequences (PRBS31). In all reported measurements the HSPM reverse bias voltage is equal to 1.2V. The CW laser power delivered to the input grating coupler is close to 13dBm. The measured 56Gbps optical eye diagram is shown in Fig. 14. Scope triggering without averaging is applied. The eye diagram with the MZM operated at quadrature point to maximize OMA is compared with simulations in Fig. 14a. An ER of 2.5dB has been achieved, in agreement with Silicon Photonics state-of-the-art [19]. The ER can be increased to 3.5dB by shifting the MZM operating point by $\pi/10$, while maintaining the crossing point of the eye diagram beyond 48% (see Fig. 14b). Optical eye diagrams at 28Gbps to demonstrate backward-compatibility are shown in Fig. 15.

Tab. II compares present work with published electro-optical transmitters realized in different technologies and having similar data rates [19-21]. This work shows ~30% power saving compared to Silicon Photonics state-of-the-art [19], demonstrating the effectiveness of the proposed equalization approach. Furthermore, it favorably compares with Directly Modulated

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Laser (DML) transmitters, allowing more than 500mW power budget allocation for the external CW laser compared to the state-of-the-art of 1310nm DML [20].

C. Low-cost optical packaging

Measurement results shown in Sections VI.A and VI.B have been obtained by directly accessing input pads via RF probes to demonstrate the intrinsic performance of the 3D-integrated Silicon Photonics transmitters and the accuracy of theoretical analysis. However, low-cost electro-optical assembly techniques maximizing the signal integrity are key and several alternative solutions are under investigation. In this work, an electro-optical assembly approach relying upon the wire bonding of the Silicon Photonics 3D stack on a low cost Land Grid Array (LGA) package with a 4-metal layer organic substrate [3] has been used for testing purposes. Output optical signals have been collected through a V-block aligned with the Photonic Integrated Circuit (PIC) grating couplers, directly glued on the PIC (inset of Fig. 16), while bondwires are covered by resin for mechanical protection. The packaged demonstrators have been mounted into a custom plastic socket employing spring probe contacts. The socket has been assembled on a 4-metal layer Printed Circuit Board (PCB) using 2.4mm coaxial connectors (Fig. 16).

On the electrical side, the main issue of such assembly is the signal integrity. It has in fact to be ensured up to 56Gbps through the whole electrical input transmission path, from the connector to the PIC pad. 3D Electro Magnetic (EM) simulations have been set up to analyze and select the proper geometry of all interconnects, for input matching at the target characteristic impedance over the whole bandwidth. Grounded coplanar waveguides (G-CPW) have been adopted on both the LGA substrate and the PCB. A particular attention has been focused on the pitch of the ground vias to prevent higher-order modes propagation. G-CPWs paths have been designed on each substrate to ensure a phase matching between differential signals better than ±5deg at 40GHz. All transitions have been analyzed by means of 3D

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electromagnetic simulations and designed as transmission lines, rather than assuming them as lumped elements or parasitics. Spring probes in the socket and bond wires have thus been EM simulated within their embedding materials, taking advantage of the dielectric constant of these materials to design transmission lines with the required characteristic impedance. The transfer function (TF) of the complete transmission path has been derived by comparing the small-signal TF of the travelling wave optical transmitter measured on-wafer to the small-signal TF of the same optical transmitter measured in package, by means of a 4-port differential Vector Network analyzer in conjunction with a reference photodiode. The comparison of the measured S-parameters with 3D EM simulations is plotted in Fig. 17, showing a good agreement. It must be noted that no high-frequency characterization was available for the embedding materials, as well as for the top finishing of the GCPWs on the PCB, which can justify the partial mismatch between the results. The smooth behavior of the attenuation of the electrical input path allows the compensation of the bandwidth limitation by means of equalization in the optical transmitter.

Optical eye diagrams at the output of the travelling wave modulator described in Section VI.B are shown in Fig. 18 to compare testboard measurements of packaged chips with probe testing results. The same input electrical signal has been used and the same IC settings have been selected with no additional input equalization. The realized assembly minimizes the degradation of the transmitted signal versus probe testing up to 40Gbps. The eye diagram is still open at 56Gbps even if slightly degraded due to the bandwidth limitation of the complete electrical input path. Larger equalization should be applied for further eye opening at 56Gbps. The proposed assembly approach and associated simulation method, adopted here for demonstration purposes, can be leveraged to optimize future designs of electrical interconnects on optical module substrates.

VII. Conclusions

Optical transmitters constitute the most challenging section of electro-optical transceivers due

to the stringent power consumption constraints set by standard modules' form factors. Among Silicon Photonics alternatives enabling cost reduction and miniaturization compared to discrete duals, MZMs constitute the most mature solution for industrial applications. In this work alternative architectures for high data rates, namely multistage and travelling wave, have been compared and analytical criteria for the choice between the two have been provided. Demonstrators relying upon first generation PIC25G optical devices and achieving 30% better power efficiency compared to Silicon Photonics state-of-the-art with comparable extinction ratio at similar data rates have been realized for both architectures. Probe testing results have been compared with measurements of packaged chips on testboard, demonstrating the effectiveness of the proposed design methodology for assembled parts. Finally, performance improvements are expected from next generations of silicon integrated optical devices, in particular HSPMs. It has been then demonstrated that Silicon Photonics MZM-based optical transmitters might be suitable to address not only current but also next generation optical communication standards.

VIII. Acknowledgment

This work has been carried out within the Studio di Microelettronica, a joint research laboratory between Università degli Studi di Pavia and STMicroelectronics. The authors would like to thank Anritsu and Tektronix for providing test equipment.

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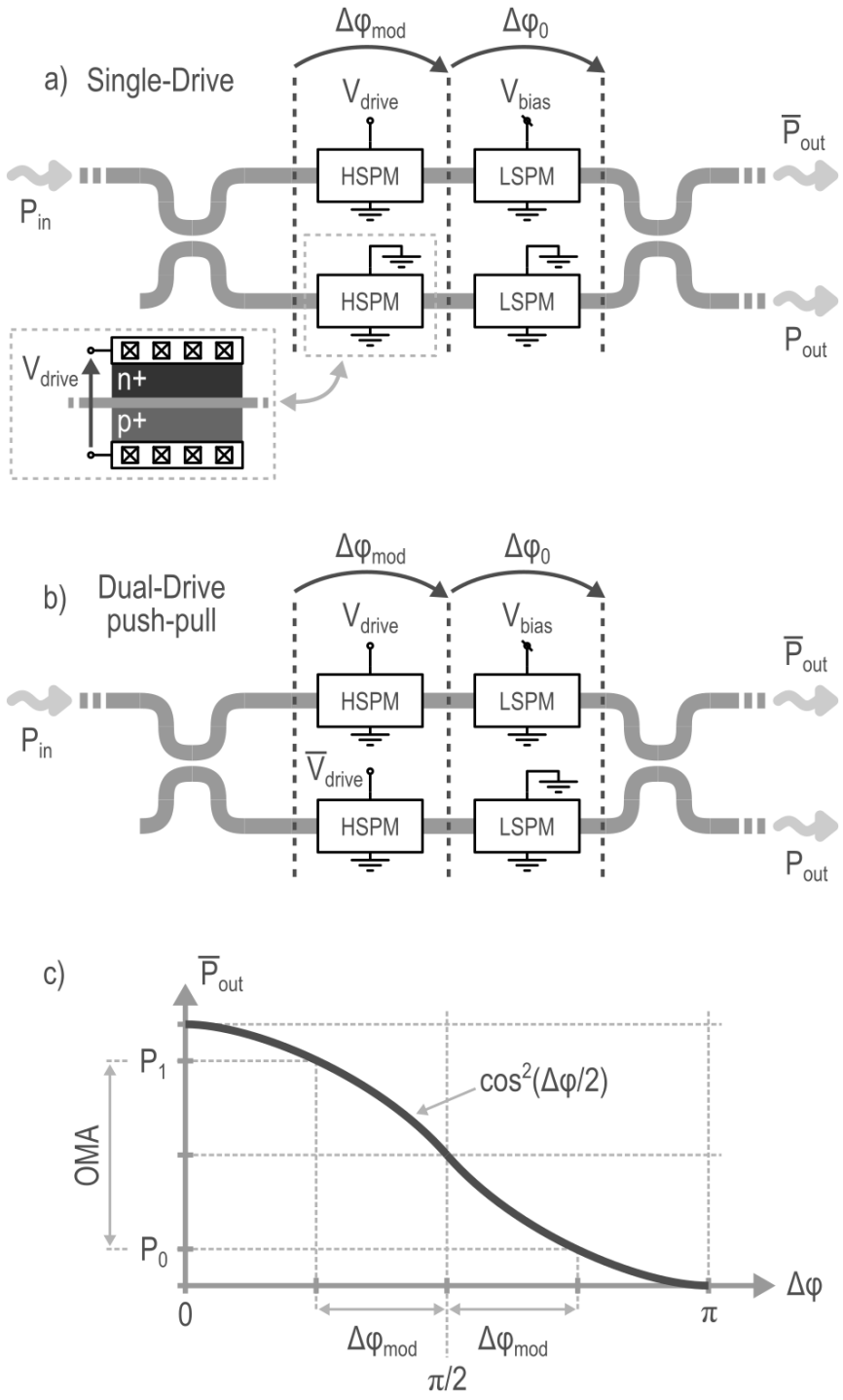

Figure 1: (a) Single-drive MZM architecture, with integrated HSPM detail; (b) Dual-drive push-pull MZM architecture; (c) Dual-drive push-pull input-output characteristic

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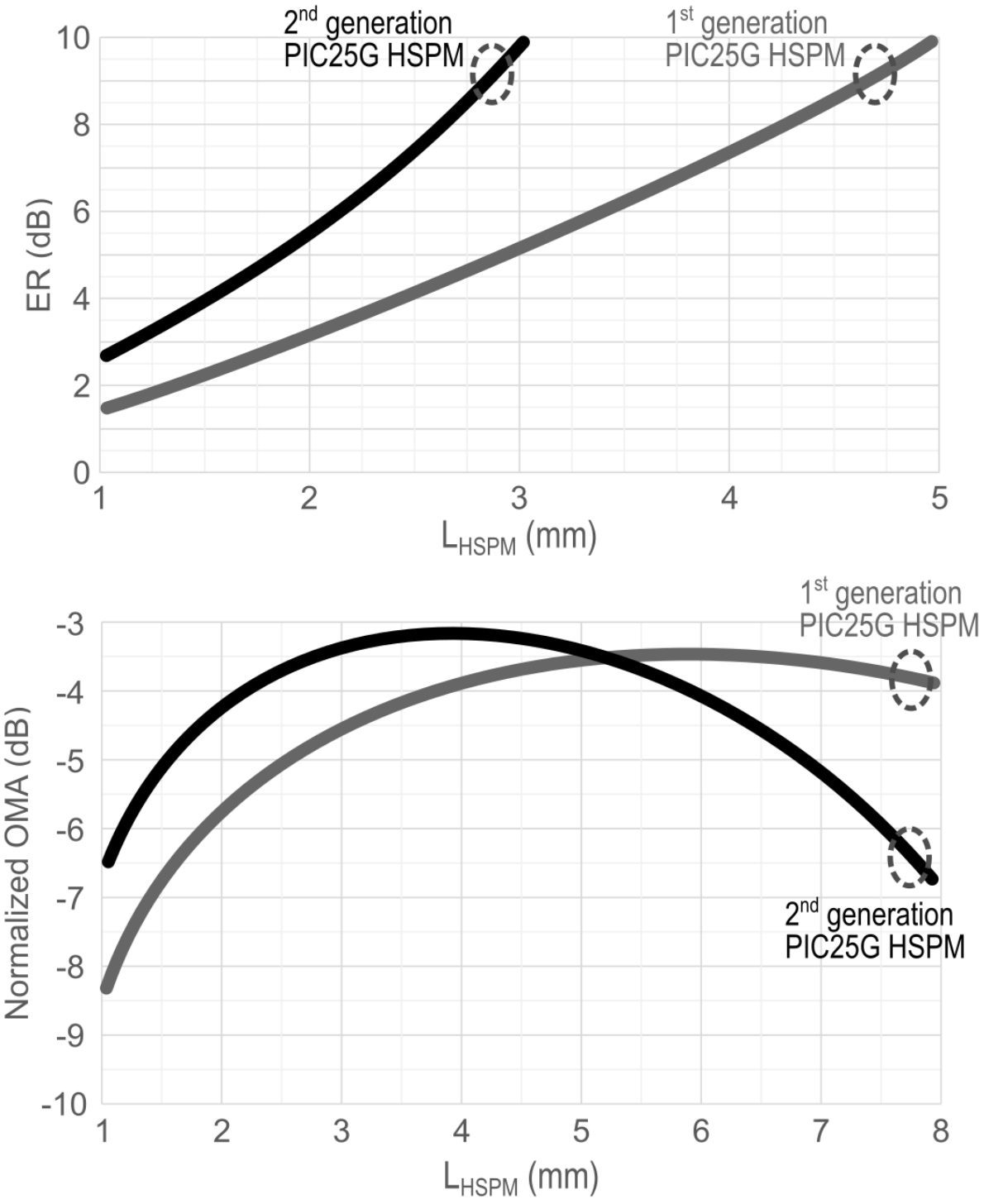

Figure. 2: (a) ER and (b) normalized OMA vs. HSPM total length for a PIC25G push-pull multistage MZM architecture biased at quadrature point

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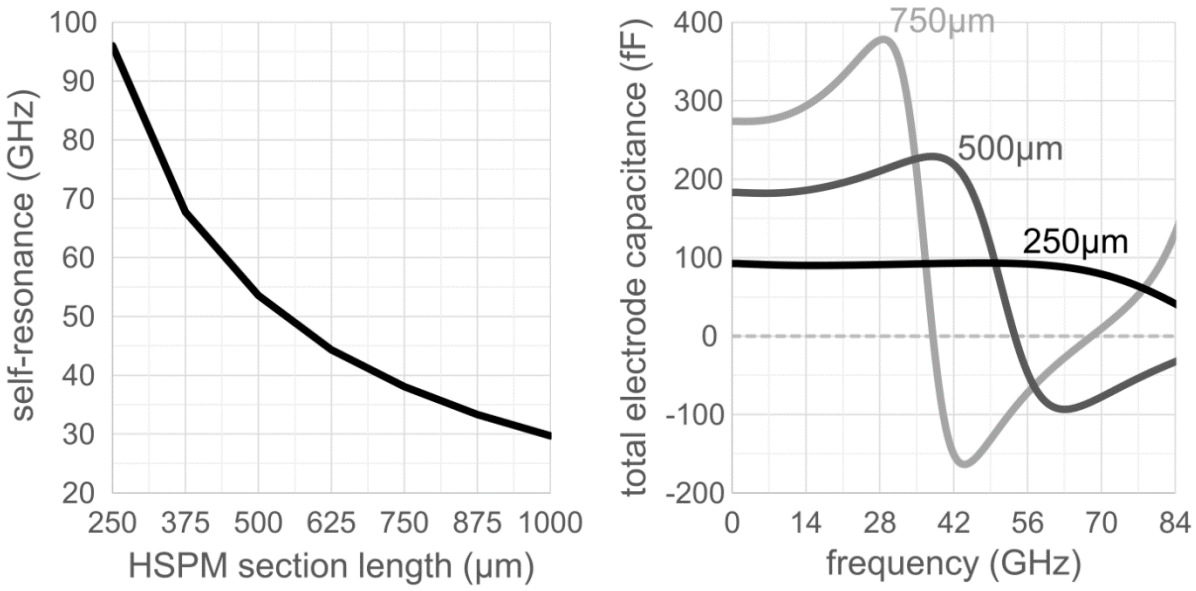

Figure 3: PIC25G HSPM + electrodes: (a) self-resonance frequency vs. HSPM sections length; (b) capacitance vs. frequency for different HSPM section lengths

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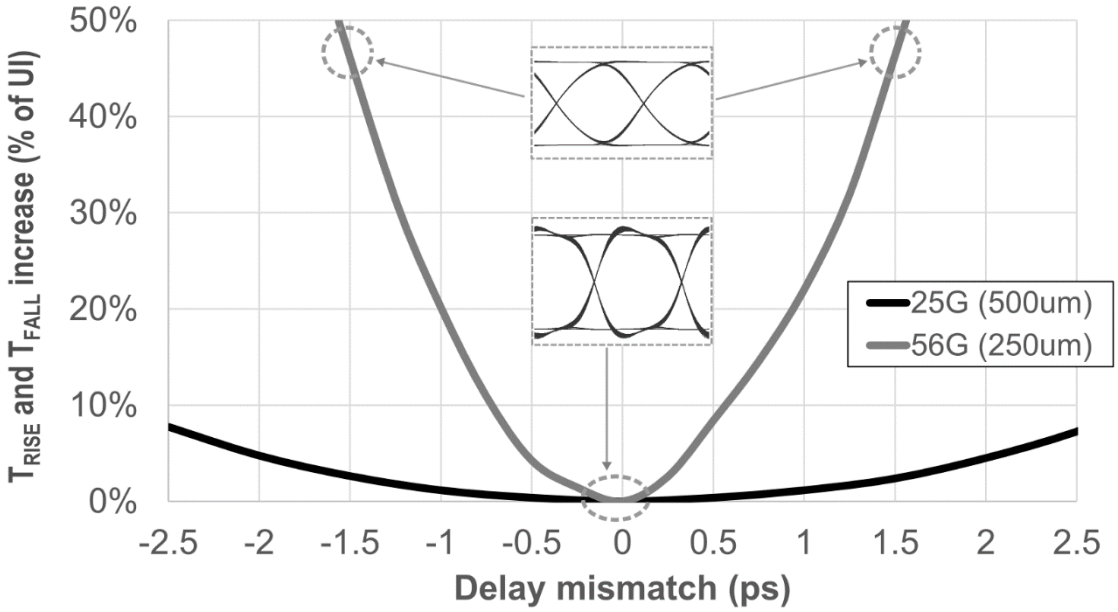

Figure 4: Optical rise and fall times increase due to the delay mismatch for a multistage MZM with ideal input transition times: (a) 500μm-long sections for 25Gbps operation; (b) 250μm-long sections for 56Gbps operation

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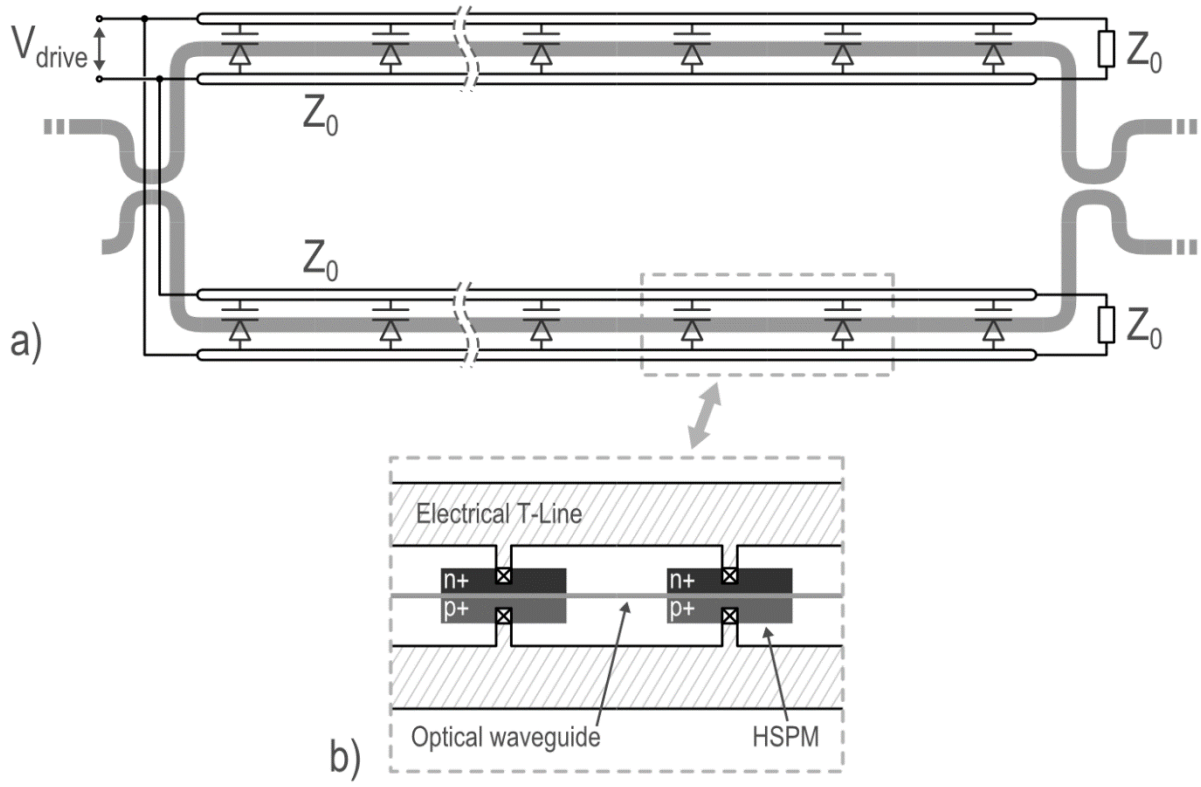

Figure 5: (a) Dual-drive push-pull travelling-wave MZM architecture; (b) Periodically-loaded transmission line with HSPM sections interleaved by un-doped optical waveguide

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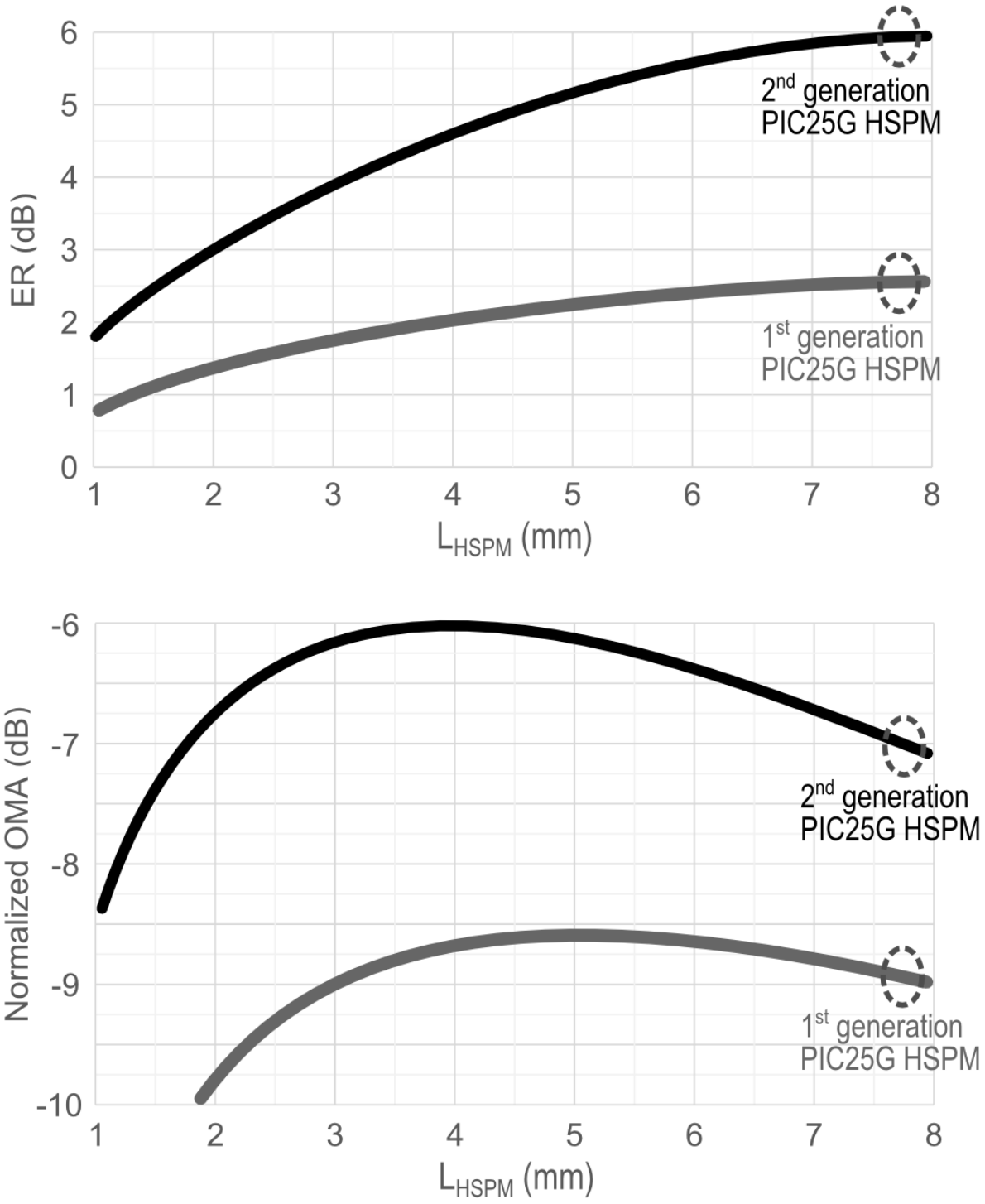

Figure. 6: (a) ER and (b) normalized OMA vs. HSPM total length for a PIC25G dual-drive push-pull travelling wave MZM architecture biased at quadrature point

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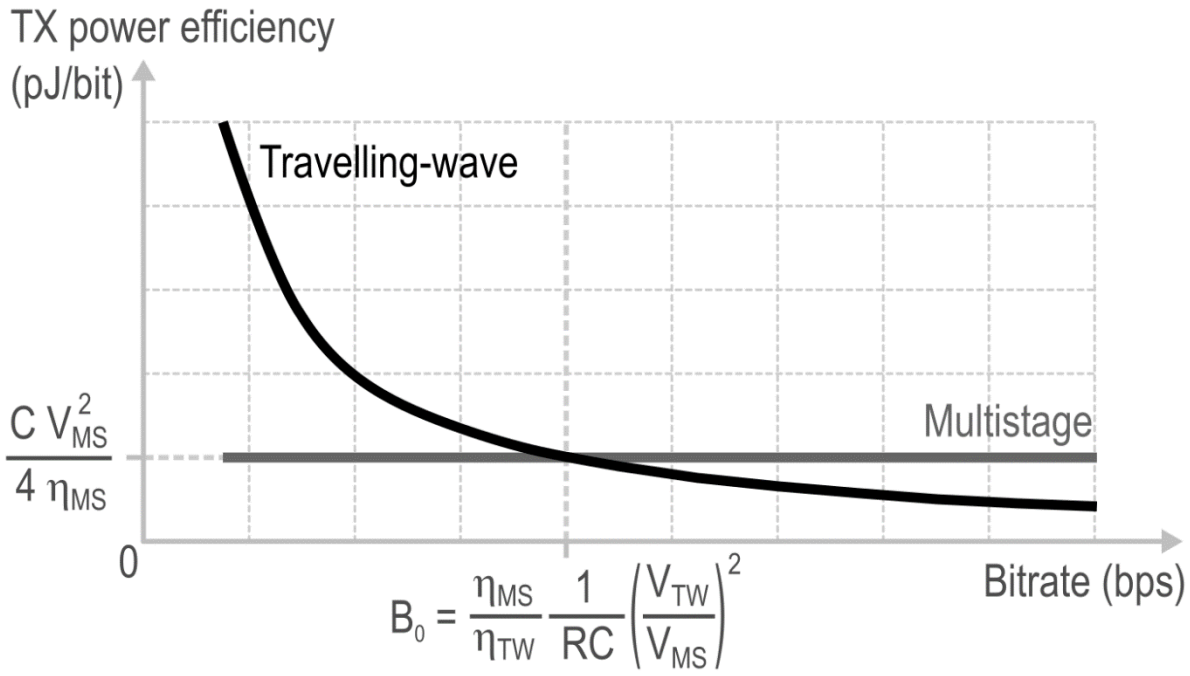

Figure 7: MZM-based transmitter power efficiency: multistage vs. travelling wave.

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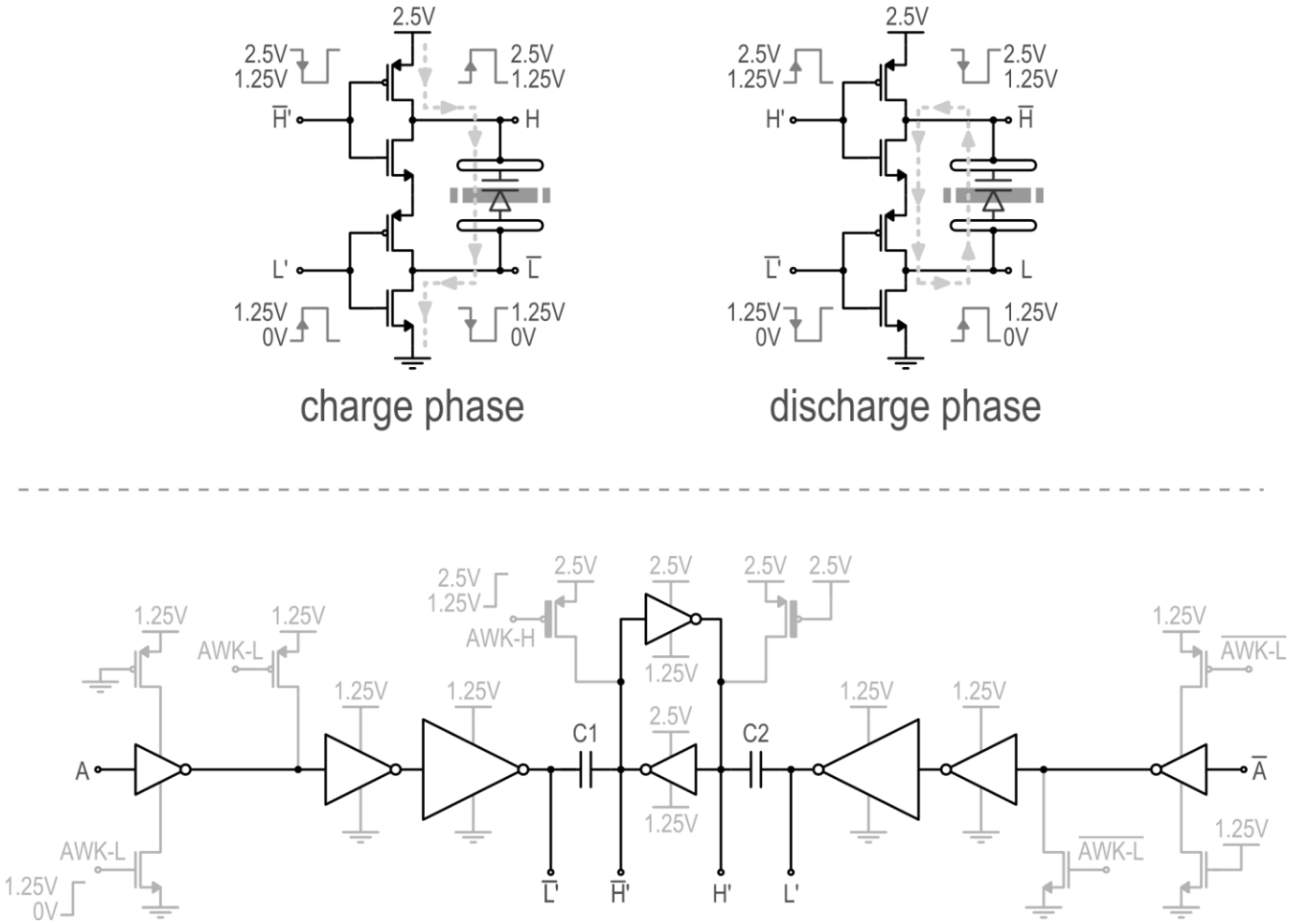

Figure 8: Schematics of stacked CMOS inverter drivers (top) and DC-shifter (bottom, with pre-charging MOS transistors in grey). Thick-line gates transistors indicate thick-oxide transistors

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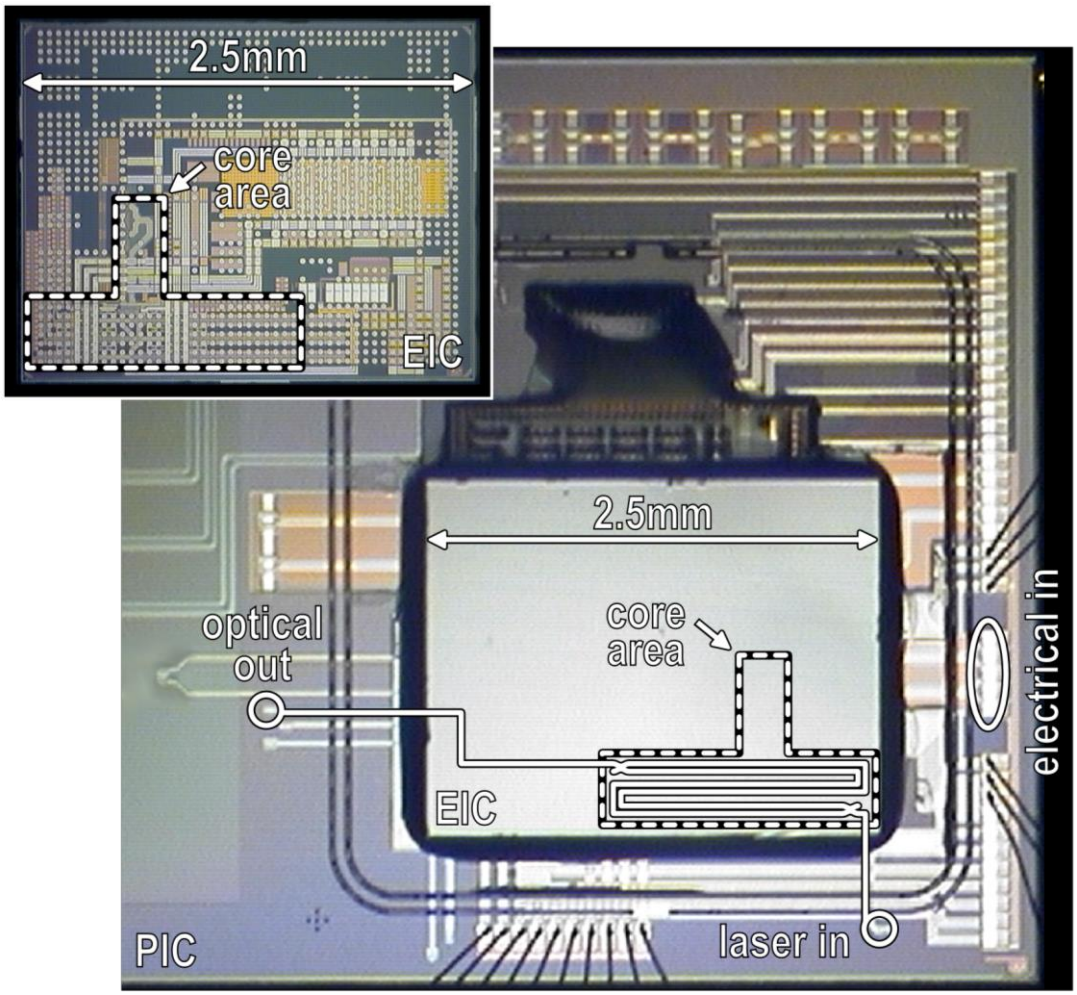

Figure 9: Photomicrograph of the multistage 3D assembly and stand-alone EIC

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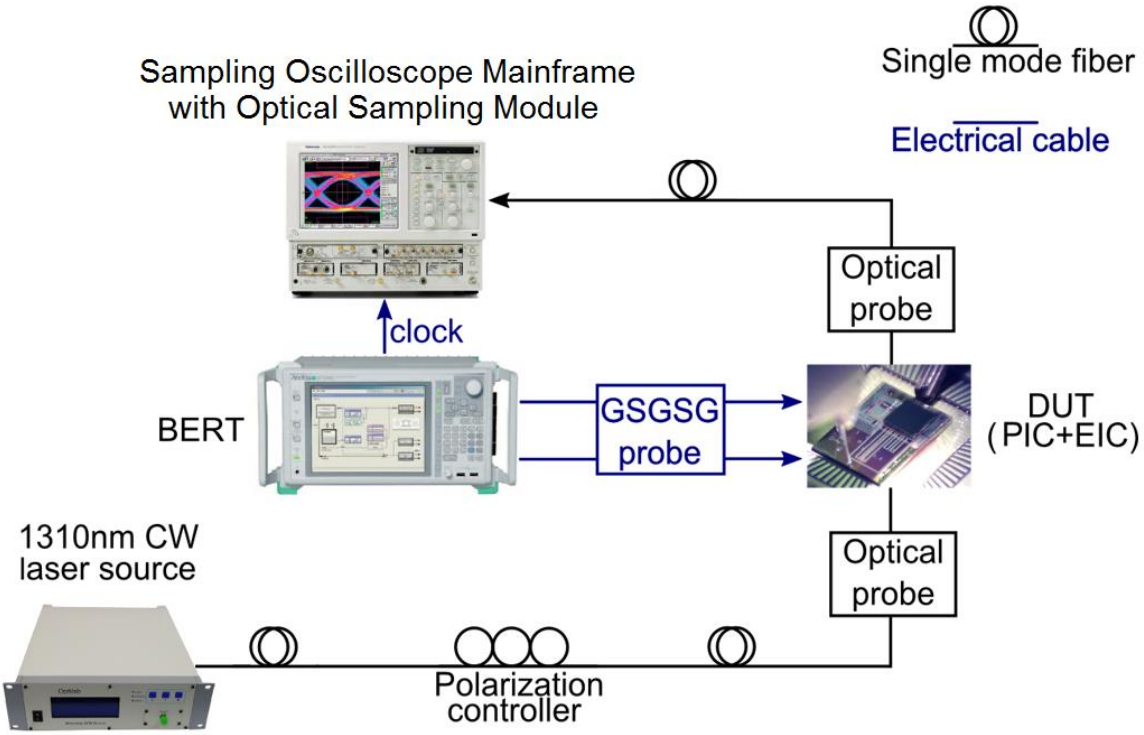

Figure 10: Measurement setup

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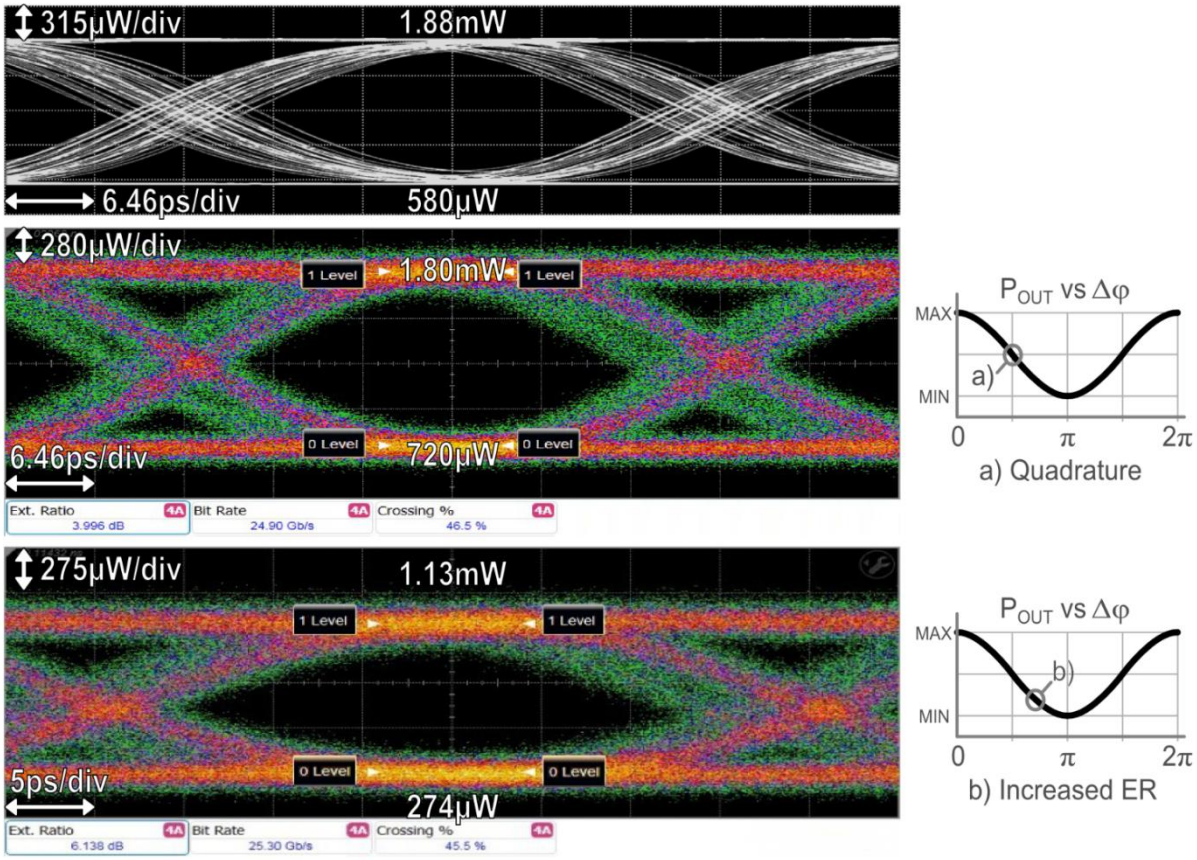

Figure 11: 25Gbps MZM eye diagrams: a) electro-optical co-simulations at quadrature point; b) measurements with the oscilloscope standard triggering at quadrature point; c) measurements at increased ER with oscilloscope standard trigger.

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Item	Unit	[18]	[17]	This work
PIC technology	-	N/A	180nm SOI CMOS	**PIC25G**
EIC technology	-	CMOS 130nm	65nm CMOS	**65nm CMOS**
Chip-to-chip assembly technology	-	Wire bonding	Wire bonding	**Copper pillar**
Modulator architecture	-	Travelling wave	Travelling wave	**Multistage**
Data rate	Gbps	20	25	**25**
HSPM length	mm	1	N/A	**3**
Transmitter power efficiency	pJ/bit	15.6	20.8	**11**
Extinction Ratio	dB	5	4	**4 (up to 6)**

Tab.I: Performance summary and comparison with state of the art Silicon Photonics transmitters using carrier depletion MZMs

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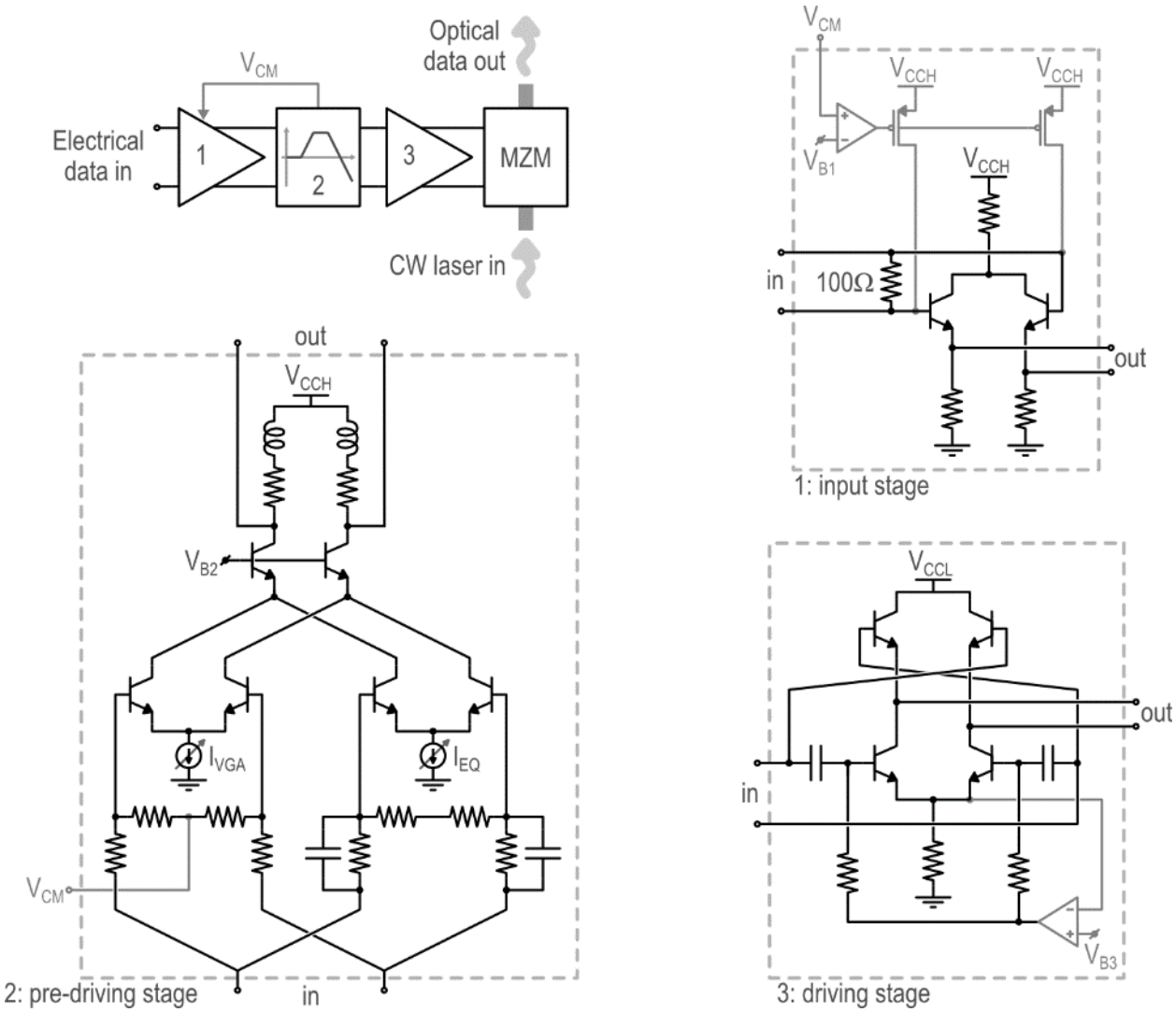

Figure 12: Simplified pre-driver and driver schematics.

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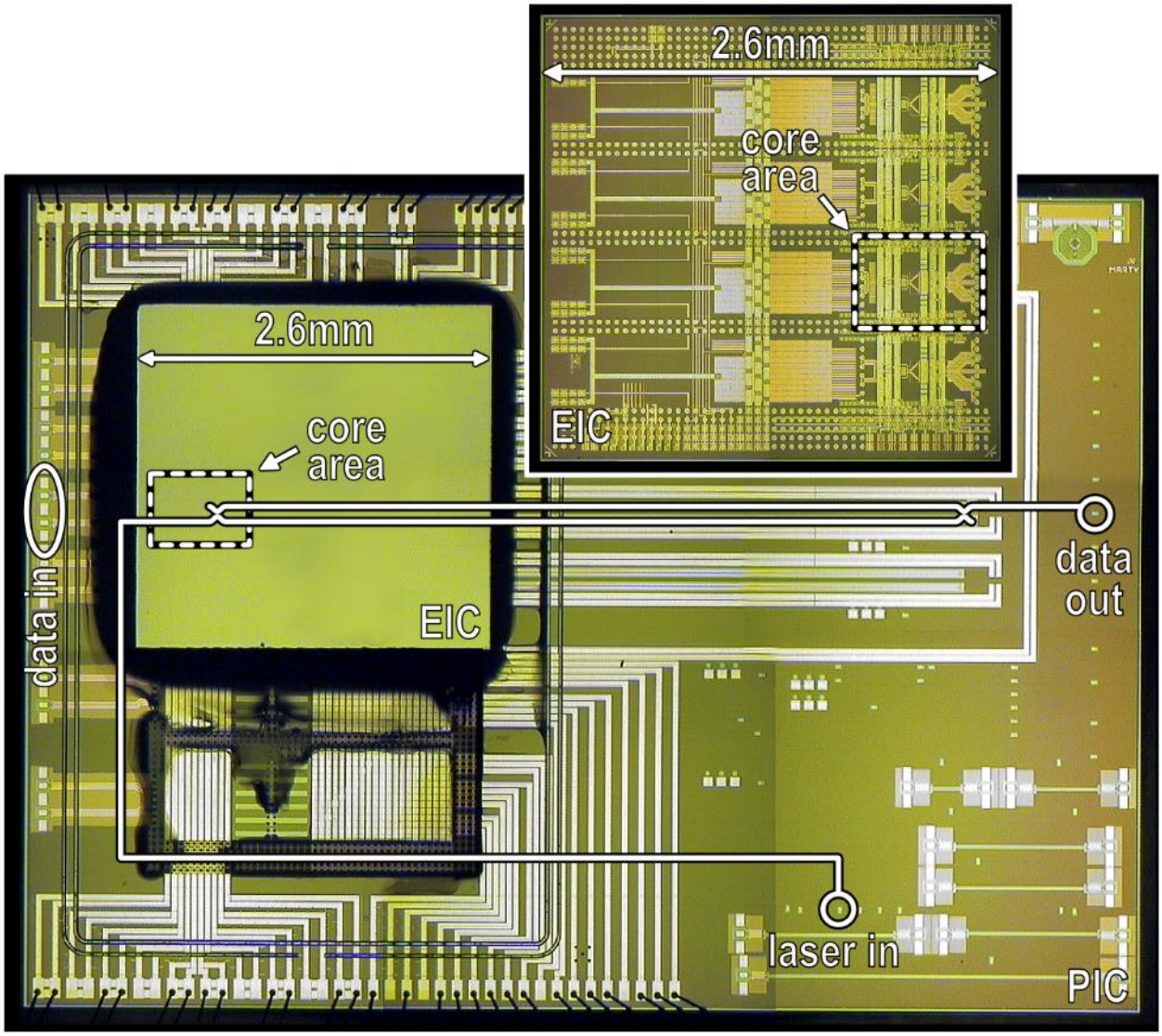

Figure 13: Photomicrograph of the travelling wave 3D assembly and stand-alone EIC

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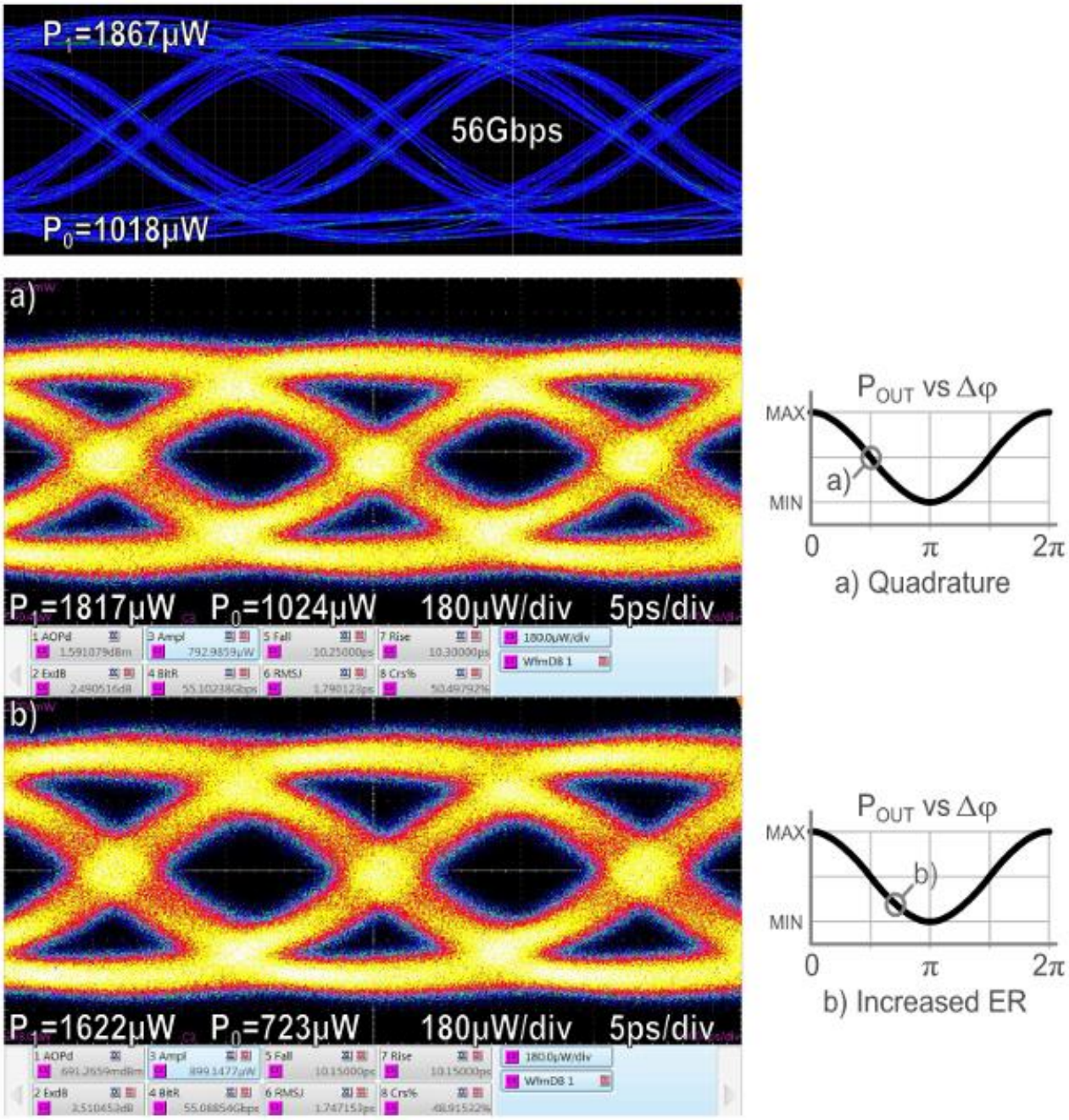

Figure 14: 56Gbps MZM eye diagrams: a) electro-optical co-simulations at quadrature point; b) measurements with the oscilloscope standard triggering at quadrature point; c) measurements at increased ER with oscilloscope standard trigger.

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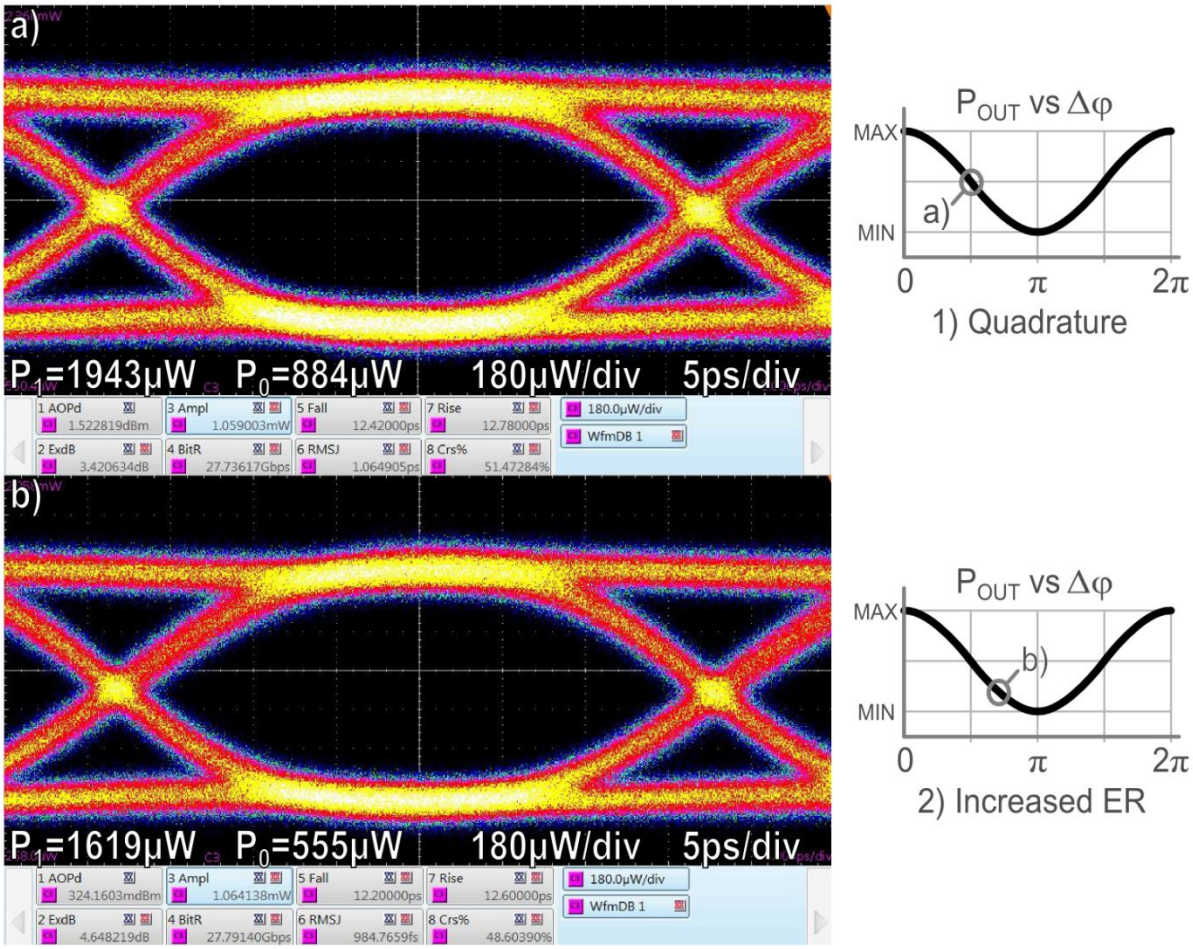

Figure 15: 28Gbps PRBS31 MZM eye diagrams: a) measurements at quadrature point; b) measurements at increased ER.

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Item	Unit	[21]	[20]	[19]	This work
Wavelength	μm	0.85	1.3	1.3	**1.3**
Data rate	Gbps	56	50	56	**56**
Transmitter architecture	-	Directly modulated VCSEL	Directly modulated DFB-LD	Silicon Photonics MZM	**Silicon Photonics MZM**
Driver technology	-	130nm BiCMOS	180nm BiCMOS	130nm BiCMOS	**55nm BiCMOS**
Test data pattern	-	PRBS7	PRBS9	PRBS9	**PRBS31**
ER at quadrature	dB	N/A	N/A	2.7	**2.5**
MZM driver dissipated power	mW	-	-	430	**300**
DML driver dissipated power	mW	682	810	-	**-**

Tab.II: State of the art 56Gbps electro-optical transmitters.

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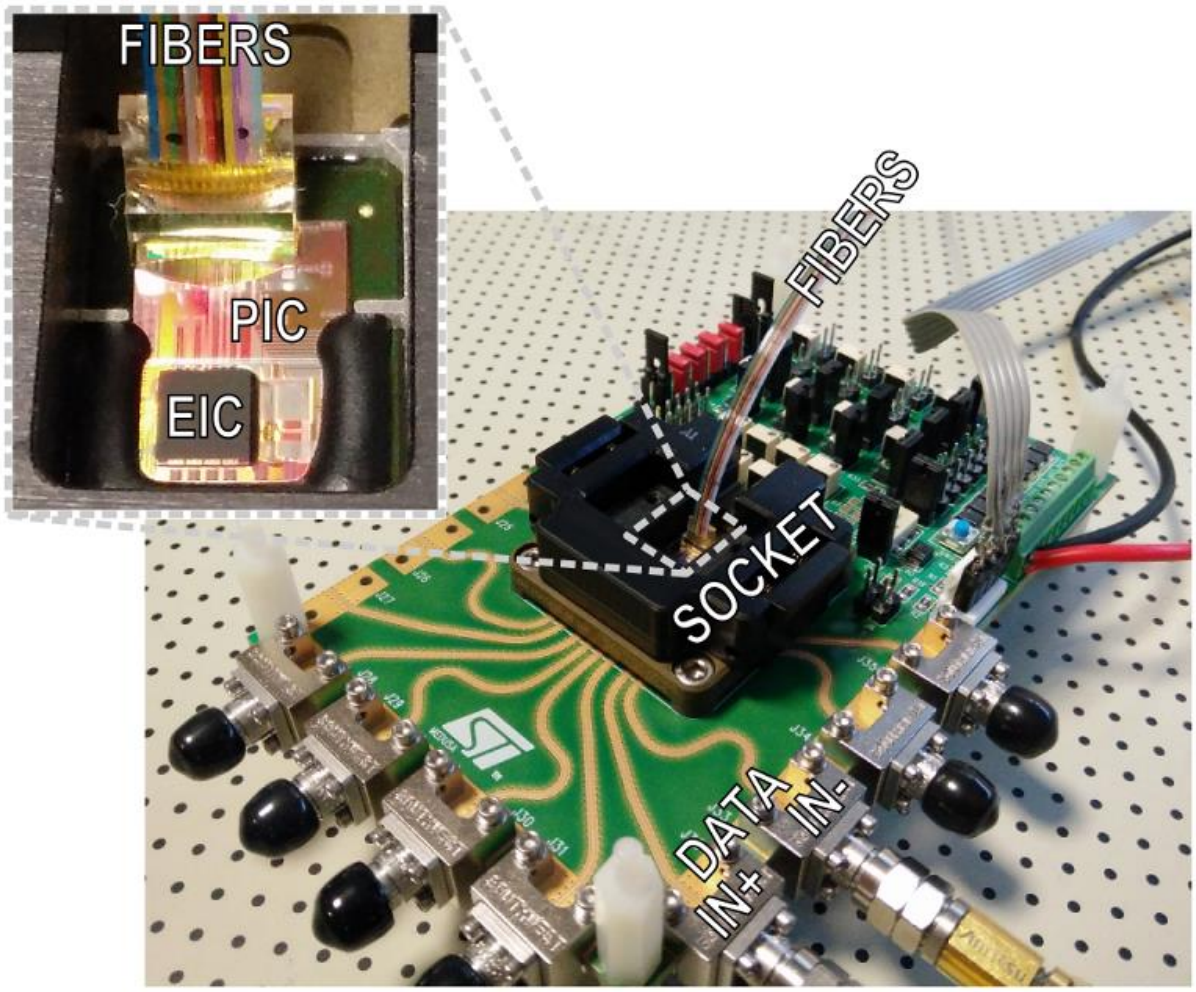

Figure 16: 4-metal layer PCB with plastic socket and 2.4mm coaxial connectors

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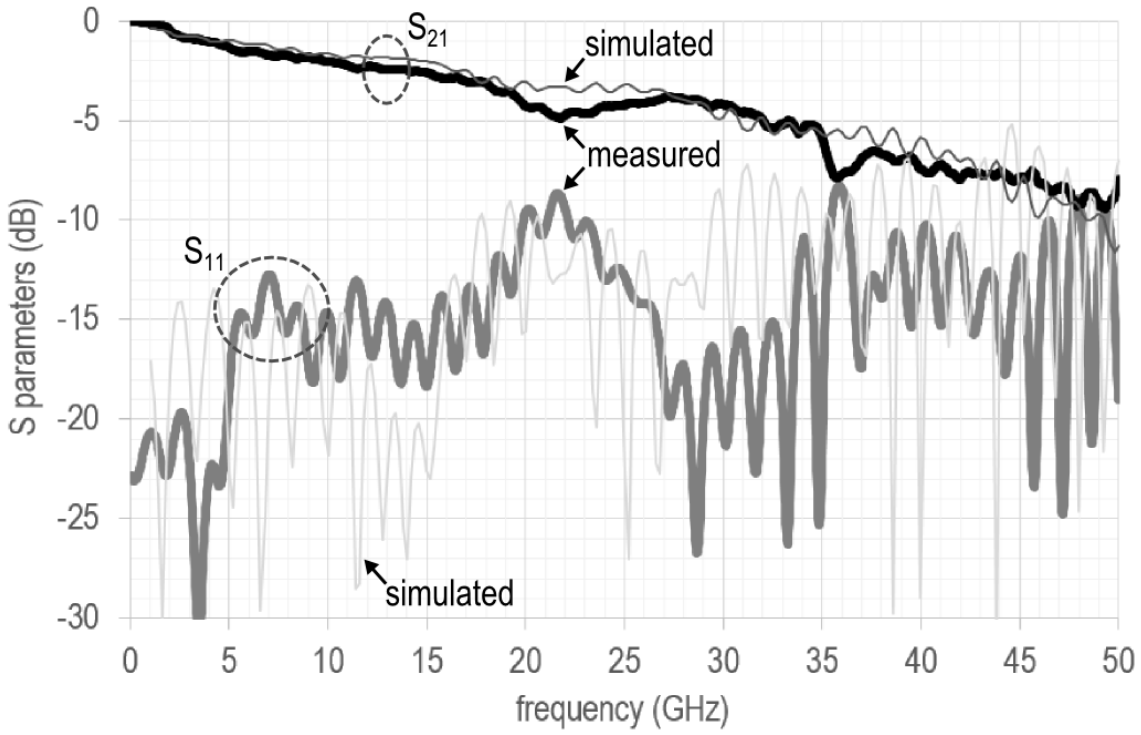

Figure 17: Comparison of measured S-parameters with 3D EM simulations

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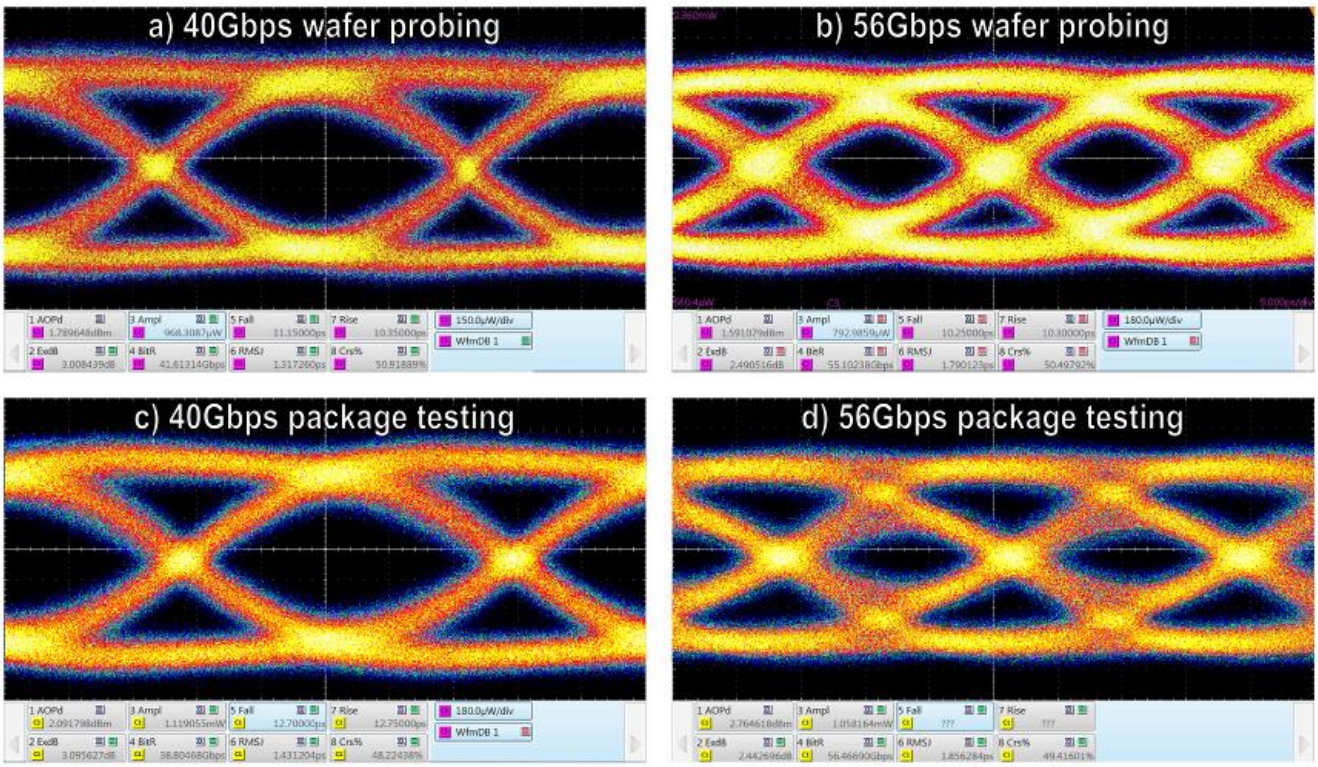

Figure 18: Optical eye diagrams at 40Gbps and 56Gbps: probe testing (a, b) vs. packaged chip on PCB (c, d)