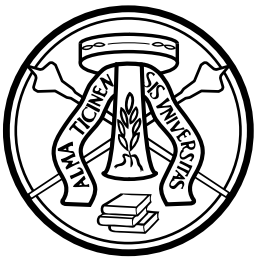

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DEPARTMENT OF ELECTRICAL, COMPUTER AND BIOMEDICAL ENGINEERING

PH.D. SCHOOL IN MICROELECTRONICS
CYCLE XXXVII

Design of an Ultra-Low Power Quasi-Passive Error-Feedback Noise-Shaping SAR Converter for Audio Activity Detection

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Abstract

Design of an Ultra-Low Power Quasi-Passive Error-Feedback Noise-Shaping SAR Converter for Audio Activity Detection

by Marco Tambussi

This doctoral thesis, carried out in collaboration with TDK-InvenSense, presents the study and the design of an ultra-low power Analog-to-Digital Converter (ADC) suited for Audio Activity Detection (AAD) features. Exploiting oversampling and noise-shaping techniques, a Successive-Approximation-Register (SAR) converter is boosted to achieve high-resolution and low-noise while consuming the lowest possible power. AAD circuits are used in a wide variety of battery-operated devices, such as mobile phones and wearable devices, where the need to preserve energy is crucial. For this reason and many others that are explained later, power consumption is one of the main aspects considered. In this thesis are described the working principles of a Quasi-Passive Error-Feedback Noise-Shaping SAR (QP-EF-NS-SAR) converter, from the conception to the measurements, passing through all the design steps that led to the final physical implementation. This converter reaches 78 dB of Dynamic Range (DR) achieving a Schreier Figure-of-Merit (FoM_s) of 165.3 dB. Fabricated in a 65-nm BCD process, the proposed ADC core occupies 0.129 μm^2 consuming only 14.9 µW from a 1.2-V supply.

Contents

Introduction

MOBILE devices have grown significantly in the last few years. It is estimated that, from the year 2020 to 2025, the total number of mobile devices will increase from 14 to 18.2 billion units, making this market one of the world's most profitable. Integrated audio systems are crucial since are present in almost every one of these battery-operated devices. Micro Electro-Mechanical Systems (MEMS) microphones chains are employed in a huge variety of different fields. In mobile phones [1–11] and wearable devices [1,2,5,6,12,13], they are used to capture high-quality audio calls and recording, in the automotive area [10, 14–16] they are utilized for hand-free calling, voice control or even pedestrian detection [17]. In the medical field [13, 14, 18], they are exploited in smart stethoscopes [19, 20], blood pressure monitoring, or to detect abnormal heartbeats [21]. Furthermore, these devices are fully integrated into the Internet of Things (IoT) ecosystem [2, 5, 18, 22]. Audio Activity Detection (AAD) is one of the most sought-after application in the consumer market and allows the recognition of specific patterns inside an audio signal. MEMS microphones that uses this feature are used in smart voice assistants [7, 10, 23, 24] like Amazon Alexa and Google Home, which operate based on the user's voice commands. They are also embedded in smart TV remote controls and can be installed in smart home rooms [5]. Besides, they are also utilized in Augmented Reality (AR) and Virtual Reality (VR) [25–27] in order to enable communication with Head Mounted Displays (HMD). Within the True Wireless Stereo (TWS) framework, they are employed to ensure clear sounds by exploiting beamforming and noise cancellation techniques.

More in detail, audio activity detection is a feature that allows a microphone, or in general a front-end circuit, to identify an event inside an audio signal. This can be human speech, in this case is defined as Voice Activity Detection (VAD), or a specific sound. As shown in Fig. A, AAD is used in a variety of different applications, from VAD to echo cancellation passing through more complex pattern recognition. Broadly speaking, it is a "wake-up" pre-processing method used to enable the signal readout interface when voice or sound is present to avoid processing undesired noise and wasting energy [28]. On top of that, increasing the system complexity, keyword recognition features can be applied. This auxiliary circuit works continuously seeking for the aforementioned event

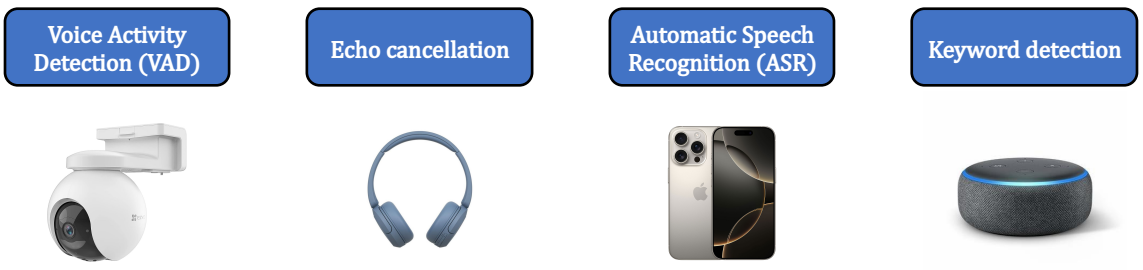


FIGURE A: Main applications of audio activity detection.

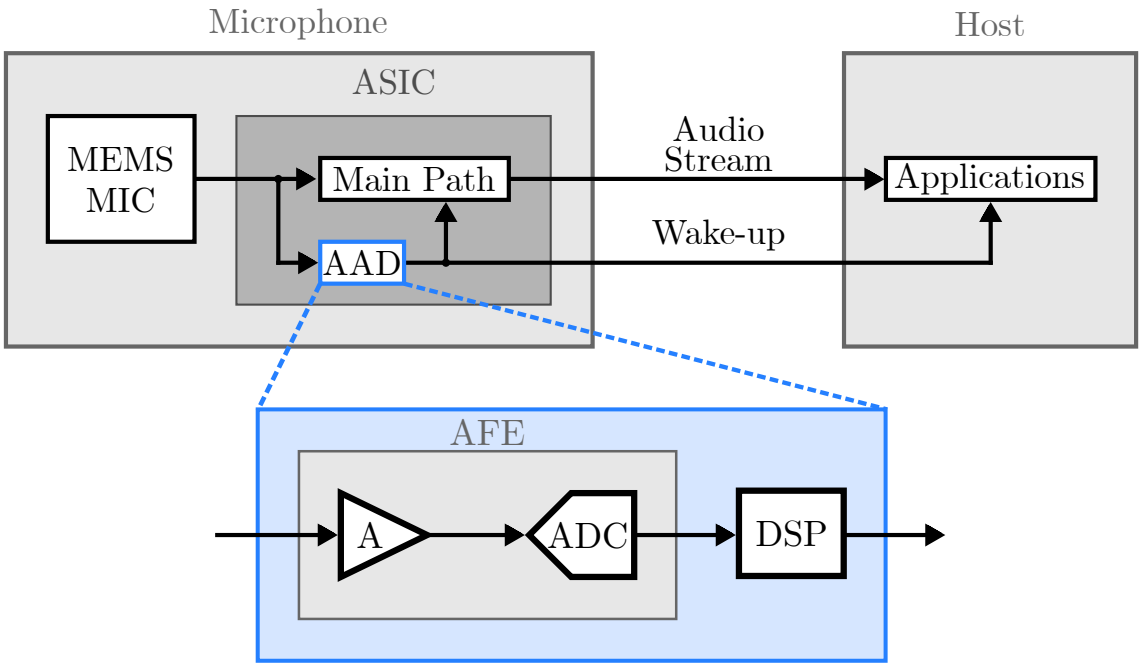


FIGURE B: Simplified schematic of a microphone read-out circuit with a detail on the AAD classic circuit implementation.

and triggers the main microphone path whenever it is needed. In battery-operated devices it is then crucial that AAD circuits should consume less power as possible since they are always on. In the literature, there are several techniques and algorithms that are used to process the audio signal such as the Zero Crossing Rate (ZCR) [29], the energy-based methods [30], the Single Frequency Filtering (SFF) [31], the Sequential Frequency Scanning (SFS) [32], etc. Although purely analog circuits can be implemented, the most of AAD techniques require solutions in the digital domain. Digital signals can convey information with less noise, distortion and interference; they can be stored on digital support in order, for instance, to be used later. Depending on the target application, more refined digital system can be implemented. In high level applications, such as keyword detection or automatic speech recognition, digital systems based on Neural Networks (NN) are commonly employed. Neural networks are data-driven models inspired by the structure of biological neural systems and are capable of learning complex and non-linear mappings from audio data. Their use in AAD applications is motivated by their ability to automatically extract discriminative features and to achieve high robustness against noise, speaker variability, and diverse acoustic conditions.

In a typical microphone system, shown in Fig. B, the audio signal picked up by a MEMS microphone is routed into two different paths:

- The main path converts and amplifies the useful signal and sends it forward to the rest of the circuit.
- The AAD path amplifies and converts the signal into the digital domain, delivering it to a Digital Signal Processing circuit, which takes the decision to "wake-up" or not the main path.

It is clear that the auxiliary path, being always "active", needs to be power efficient, otherwise nullifying the advantages of using AAD.

The main blocks that compose the AAD are three:

1. a Pre-Amplifier (PA);
2. an Analog-to-Digital Converter (ADC);
3. a Digital Signal Processing circuit (DSP);

The PA is a circuit that amplifies the input signal in order to provide a clean and robust signal to the rest of the chain. Its gain can be fixed or variable depending on the output swing needed, independently of the microphone used or of the operating conditions. Its output signal is then processed by an ADC, which converts the analog audio signal into the digital domain. For this type of application, the two main targets to achieve are the lowest possible power consumption and the lowest possible area occupation. On top of this, it is necessary to achieve a resolution sufficiently high to allow suitable processing with the following DSP. The DSP, indeed, plays the role of taking the decision of activating or not the main path based on various factors.

This thesis presents a Quasi-Passive Error-Feedback Noise-Shaping Successive Approximation Register (QP-EF-NS-SAR) analog-to-digital converter specifically designed to be fitted in an AAD chain. This topology combines the benefits of the SAR ADC architecture, like low power consumption, high conversion efficiency and small area occupation, with the benefits of noise shaping, which allows increasing drastically the overall resolution. This hybrid topology alters the spectral shape of the quantization error in such a way that it is no longer uniformly distributed but its contribution is pushed at a higher frequency, outside the audio band. Combining this effect with oversampling techniques and filtering the out-of-band spectral components, a boost in the Effective Number of Bits (ENOB) is achieved. More in detail in the proposed converter a second order Charge-Sharing based loop filter is exploited in order to minimize power consumption while preserving a good final resolution. This scheme, called Quasi-Passive loop filter, will be extensively described further. Moreover, NS-SAR ADCs scale well with technology below 65 nm, unlike over-sampled $\Sigma\Delta$ converters, which are their direct competitors in this market share.

This thesis is organized as follows: In Chapter 1, the basic theory of analog to digital converters is thoroughly described with emphasis on SAR converters and the oversampling technique commonly employed for these circuits. The theoretical and implementative differences between active and passive noise shaping circuits for SAR ADCs are discussed. Subsequently, in Chapter 2, after a preliminary analysis with the support of block level Matlab® and Simulink® simulations, the design steps of the later and final implementation of the proposed ADC are described. Chapter 3 is devoted to presenting all the measurement results as well as how the measurement setup was designed and built. Finally, all results, design choices, considerations, and comparison with the State-of-the-Art (SotA) are included in Chapter 4.

Chapter 1

Noise-Shaping SAR Converter Theory

AUDIO Analog Front-Ends (AFEs) employ several blocks that work in unison to ensure that the audio signal is transduced properly from its physical form to an electric signal. The term "sound" is used to describe a physical quantity, defined as a vibration that propagates as an acoustic wave in a transmission medium. The human ear can detect the variation of the atmospheric pressure caused by this vibration in a frequency range of approximately 20 Hz to 20 kHz. To translate this perturbation into the electrical domain, a family of transducer devices, called microphones, can be used. In particular, the most used devices in integrated electronics are the MEMS microphones. There is a huge variety of commercially available MEMS microphones that employ different transduction method to convert acoustic waves into an electric quantity such as electromagnetic, piezo-resistive, piezo-electrical, optical, spintronic and capacitive. Nevertheless, the majority of MEMS microphones produced, rely on capacitive transduction due to its superior sensitivity, lower power consumption, and enhanced compatibility with batch production. Capacitive MEMS transducers exploit a mechanical mass that, when hit by the sound wave, vibrates generating a capacitance variation. The aforementioned transducers require an interface circuit to translate this capacitance variation into an analog electrical signal, amplify it, and, in many instances, convert it into digital form. As previously indicated, a complete read-out circuit comprises a pre-amplifier and an ADC (see Fig. B). In a typical environment, sound intensity ranges from 0 dBSPL (auditory threshold) to 140 dBSPL (threshold of pain). Given that microphone sensitivity typically ranges from $-45\,\mathrm{dBV/Pa}$ to $-35\,\mathrm{dBV/Pa}$, this results in an electrical signal with an amplitude of only a few millivolts (or tens of millivolts in optimal scenarios), which are insufficient for most applications. It is therefore essential to use an audio pre-amplifier (PA) to amplify the signal before onward transmission. Furthermore, they facilitate decoupling between the microphone and the rest of the circuitry, and guarantee optimal biasing of the microphone itself.

The optimization of this interface circuit is conducted in parallel with the enhancement of MEMS microphone performance, including Signal-to-Noise Ratio (SNR), Dynamic Range (DR), Total Harmonic Distortion (THD), as well as power consumption. In modern audio applications on portable devices, power consumption has become a primary consideration, and thus it is a crucial factor in the optimization process. In this chapter, a discussion on the basic theory of analog-to-digital converters is conducted placing greater emphasis on the SAR ADC structure and the oversampling techniques used to improve its resolution.

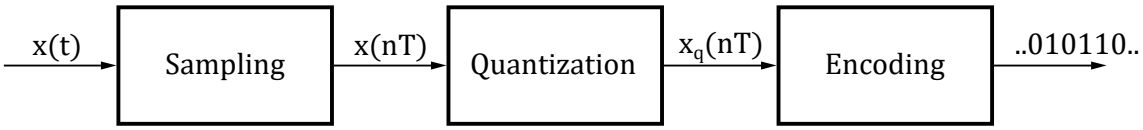


FIGURE 1.1: Block diagram of an analog-to-digital converter.

1.1 Data Converter

The need to manipulate the signal in order to recognize human speech leads inevitably to convert it from the analog world into the digital domain. It is undoubtedly easier to work with a stream of bits when it comes to understand its behaviour. Digital signals can convey information with less noise, distortion and interference, and they can be stored on digital support in order, for example, to be used later. They are more flexible because DSP operations can be altered using digitally programmable systems and, in general, digital systems are more accurate since the probability of error occurrence can be reduced by employing error detection and correction codes. Analog-to-digital converters are electronic circuits whose purpose is to translate an analog value into a digital stream of bits. As shown in Fig. 1.1, to perform such operation, three main steps are required, respectively named Sampling, Quantization, and Encoding. Sampling is the operation that discretize the time axis of the analog signal. $x(t)$ is a purely analog signal that can assume every value withing its intrinsic range for every time value (t). After the sampling process, a new time-discrete signal, $x(nT_s)$, is created where n is a integer number that define the sample and T_s is the sampling period. The quantization process makes discrete the value of all the previously generated samples. Finally, the encoding process converts the numerical sequence into a bit-stream.

1.1.1 Sampling

A conversion always starts with a sampling phase. Sampling involves extracting the values that an analog signal takes at specific time instants. When sampling is uniform, these time intervals are evenly spaced by a duration T_s, whose inverse, $F_s = 1/T_s$, represents the sampling frequency, measured in Hertz. A straightforward method to sample a signal is by multiplying it with a sequence of equally spaced ideal impulses, thereby

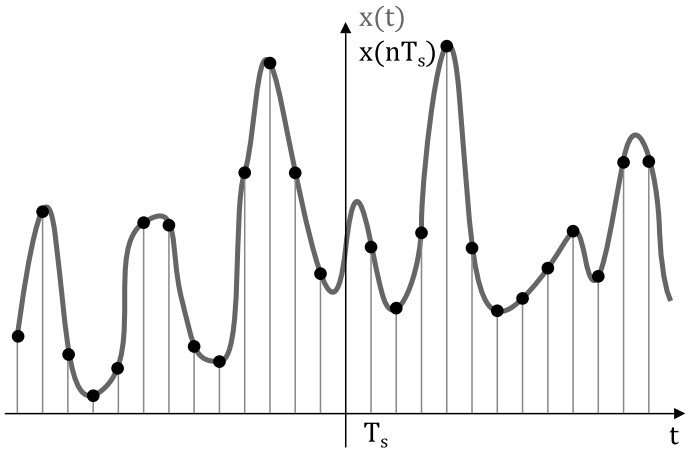


FIGURE 1.2: Example of a continuous-time signal sampling.

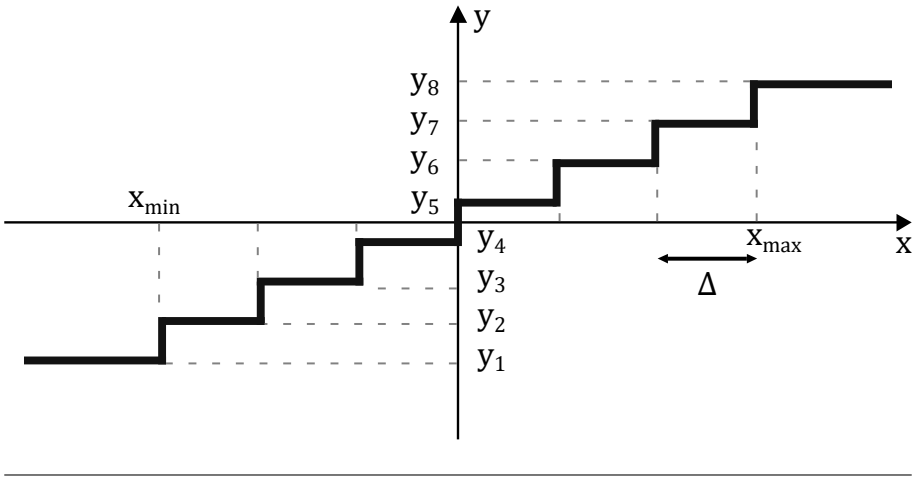


FIGURE 1.3: Example of a 3-bits uniform quantization.

extracting the signal value at the center of each impulse. As depicted in Fig. 1.2, the resulting sampled signal is essentially a series of impulses where each value corresponds to the amplitude of the original signal at that particular time instant. Although some information loss is inevitable in this process, under certain conditions, the sampled data can fully determine the original signal, allowing for its reconstruction. This requirement is outlined by the Nyquist criterion, which stipulates that the sampling frequency (F_s) must be proportional to the signal bandwidth (BW):

$$F_s \geq 2 \cdot BW. \tag{1.1}$$

As the signal frequency increases, more samples are required to accurately represent it without distortion. The minimum acceptable sampling frequency is known as the Nyquist frequency. Sampling at a frequency higher than this is called oversampling, while sampling at a lower frequency is known as under-sampling. In under-sampling, a phenomenon called aliasing occurs, where the "tails" of the original signal power spectrum overlap with those generated by sampling, leading to distortion. To prevent this, the signal bandwidth must be restricted, typically by using an anti-aliasing filter before the sampling stage.

1.1.2 Quantization

The sampling process produces a discrete-time signal that can take on values from a continuous set, meaning it can have infinite decimal places. To process the signal, these values need to be discretized. This is done by creating quantization intervals, each represented by a single value, typically the midpoint of the interval but in some cases either the upper or the lower bound can be used to represent the interval. Each value of the input (sampled signal) is then matched to its corresponding interval and assigned a quantization level. The number of these intervals is determined by the quantization resolution, which is measured in bits. An N-bit quantizer has 2^N quantization levels. A 3-bit example of uniform quantization, where all intervals have equal amplitude, is shown in Fig. 1.3. Assuming that $x_{FS} = x_{max} - x_{min}$ represents the range of the quantizer, also called dynamic range, and M denotes the number of quantization intervals (or steps), the amplitude, Δ, of each interval can be written as:

$$\Delta = \frac{x_{FS}}{M}. \tag{1.2}$$

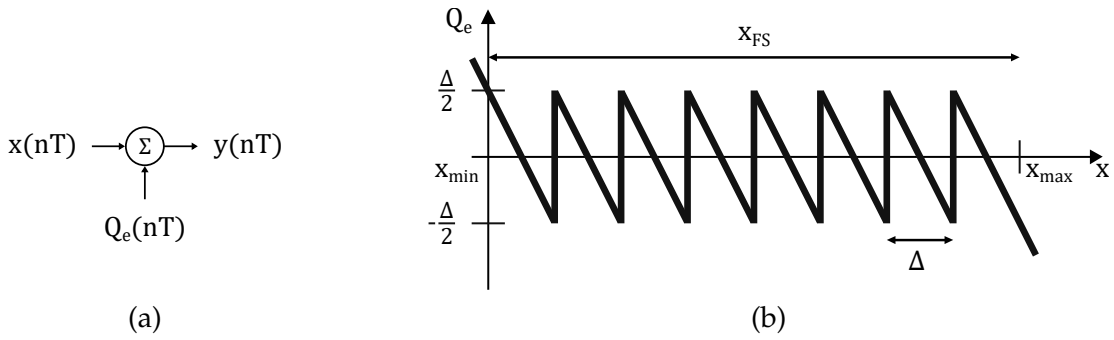


FIGURE 1.4: (a) Block diagram of the quantization process and (b) quantization error for a 3-bits data converter.

Since the midpoint of the n-th interval $x_{mid,n} = (n + 1/2)\Delta$ represents the interval amplitude, quantizing an input level that differs from $x_{mid,n}$ results in an error, known as quantization error (Q_e). Supposing a quantizer with input x, the output y will be:

$$y = x + Q_e = (n + 1/2)\Delta; \qquad n\Delta < x < (n + 1/2)\Delta. \tag{1.3}$$

In every A/D conversion is always present such quantization error which is a non-linear function of the input but it is linearly added to the sampled signal as shown in Fig. 1.4a. Keeping the same 3-bit quantization example, it is possible to plot quantization error variations with respect to the dynamic range (1.4b).

1.1.3 Encoding

After an analog signal is sampled and quantized, it is necessary that, through the encoding process, each quantized value is associated with binary symbols (bits). The resolution of this binary encoding, which involves combinations of 0s and 1s, is determined by the number of bits used. In practical analog-to-digital converters, binary numbers (base-2) are commonly used for encoding, with each bit corresponding to a power of 2. For this reason, the number of quantization steps turn out to be

$$M = 2^b \tag{1.4}$$

where $b = \lceil log_2(M) \rceil$ are the needed bits for the encoding of a single level. For instance, 3 bits can represent 8 (2^3) distinct quantization levels, with each quantized sample assigned a unique binary code. The Least Significant Bit (LSB) represents the 2^0 place, while the Most Significant Bit (MSB) denotes the highest power of 2. This binary integer directly represents the quantized amplitude of the sample in digital form. In certain situations, the amplitude range of an analog signal may be too wide, or the signal may exhibit significant amplitude variation. In such cases, linear encoding may not be the most efficient method for representing the signal. To improve encoding efficiency, the technique of companding is often employed. Companding involves both compression and expansion, and it works by mapping the output code words to the input analog amplitude levels logarithmically. This means that smaller signal amplitudes are encoded with higher resolution, while larger amplitudes are encoded more coarsely, optimizing the overall representation of the signal.

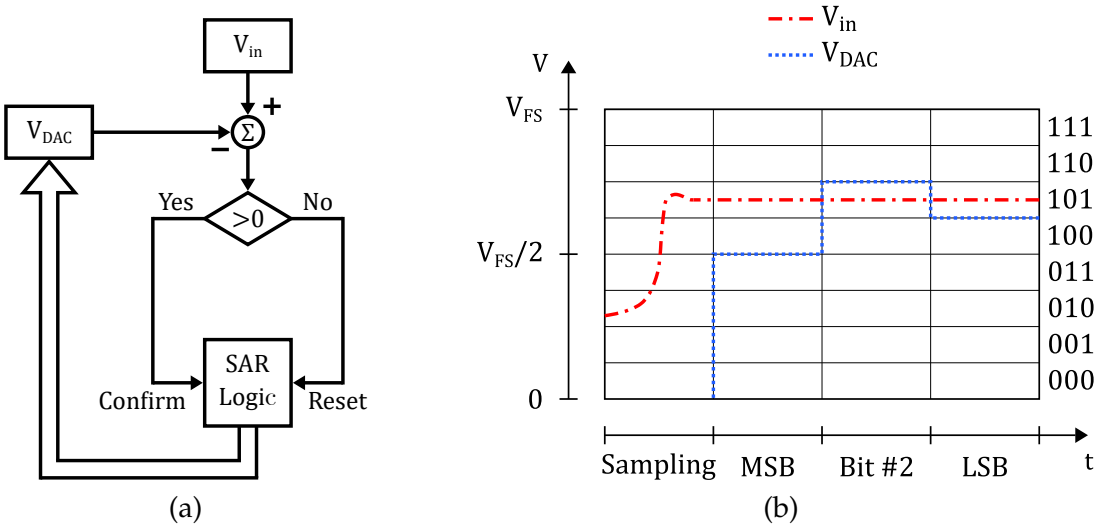


FIGURE 1.5: (a) Flowchart and (b) timing of the successive approximation algorithm.

1.2 Synchronous SAR ADCs

One of the main challenges in realizing AAD systems, since they have to be always on, is, of course, power consumption. For this reason and also for using the minimum possible area, among the various topologies of analog-to-digital converters, the successive-approximation-register ADC seems to be a good choice. This kind of converter is well known for its good performance in terms of power and area but yet it does not excel in resolution and conversion speed. Based on the binary search algorithm (or successive approximation algorithm), SAR ADCs convert the analog signal into streams of bits by refining, iteration after iteration, the output value. Synchronous SAR ADCs generate one bit per clock period, leading to wait n period of clock to fully create a n-bit digital word (plus one period for the input signal sampling). Among Nyquist rate converters, SAR ADCs are the slower in terms of conversion speed. To understand the logic behind these type of converters it is very useful to look at Fig. 1.5a, where the simplified flowchart is shown. The input signal, V_{in}, after being sampled, is compared to a threshold voltage, called V_{DAC}, generated by a Digital-to-Analog Converter (DAC). Usually the initial threshold value is set to half of the dynamic. Pre-setting this voltage means taking a guess on the value of the output bit. If the difference between the input voltage and the threshold is higher than zero, it implies that the guess was correct and the output bit is confirmed otherwise is reset. In both cases, a newly generated threshold is employed to continue the conversion. A more detailed 3-bit SAR converter behaviour example is shown in Fig. 1.5b. For a given input range $(0 - V_{FS})$, comparing the sampled input with $V_{FS}/2$ obtains the first bit (MSB) of the stream. Knowing this, it is possible to shrink the search only within $0 - V_{FS}/2$ or $V_{FS}/2 - V_{FS}$, depending on the value of the MSB, 0 or 1, respectively. In order to determine the second bit, a new threshold is then chosen between $V_{FS}/4$ or $3V_{FS}/4$. Once again, comparing the sampled signal with this threshold leads to the decision of the corresponding bit. Going on with this pattern all the remaining bits are generated. The voltages used as thresholds are generated by a digitally controlled DAC. Figure 1.6 shows the typical block diagram of a SAR ADC. After the input signal is sampled (during the first period of clock), it is maintained for the following n periods. During the first cycle, the SAR logic automatically sets the MSB

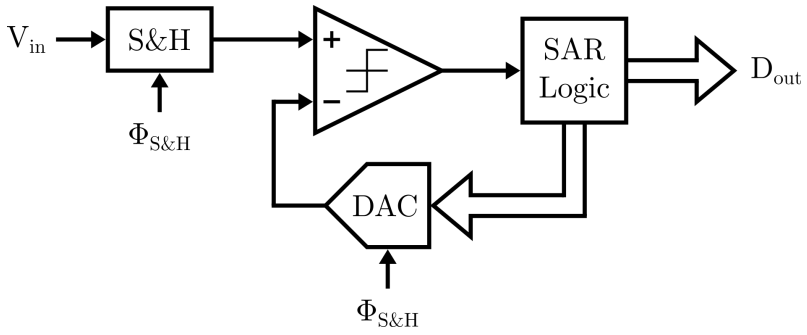


FIGURE 1.6: Basic building blocks of a SAR ADC.

to 1, in order to make the first comparison, which is performed by a comparator, whose output decides if the MSB needs to be modified (set to 0) or left untouched. Based on this result, during the next clock cycle, the new threshold is imposed by the DAC and another comparison is made. These operations continue until the last bit is found ($n+1$ periods of clock required) [33]. To overcome these problems, it is possible to apply oversampling and noise-shaping techniques. By doing so, the benefits of the SAR ADC architecture, like low power consumption, high conversion efficiency and small area occupation, with the benefits of noise shaping, which allow increasing drastically the overall resolution, are combined. Unlike over-sampled ΣΔ converters this hybrid topology scales well with technology (below 65 nm).

1.2.1 Charge Redistribution Capacitive DAC

One of the most popular implementation of the DAC in a SAR ADC is the so called charge redistribution scheme. This scheme is based on the capacitive divider DAC, shown in Fig. 1.7a. If a series of two initially discharged capacitors are connected between V_{ref} and ground, the voltage at the middle node, called V_{out}, will be:

$$V_{out} = V_{ref} \frac{C_1}{C_1 + C_2} \tag{1.5}$$

More in detail, it is possible to create an array of binary weighted capacitors, that are multiple of a unity element (C_u), that sums up to $2^n \cdot C_u$ (Fig. 1.7b), in order to realize 2^n possible output voltages. Connecting the bottom terminal to V_{ref} or to ground it is

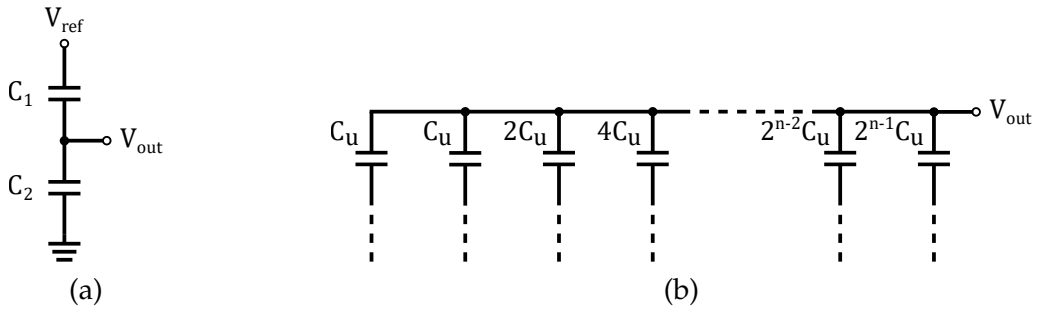


FIGURE 1.7: (a) Simple capacitor divider and (b) array of binary weighted capacitors.

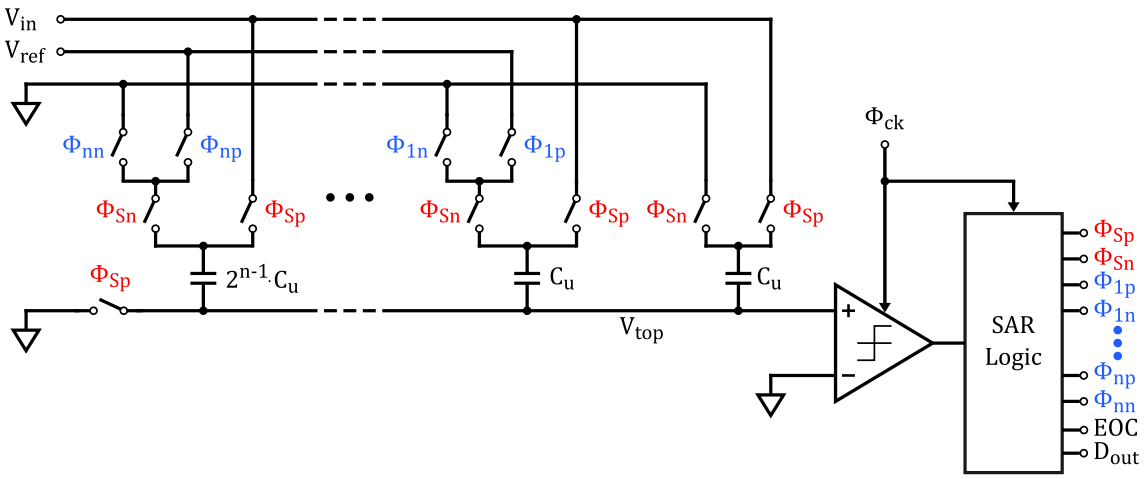


FIGURE 1.8: Scheme of a n-bit SAR ADC with capacitive DAC.

possible to create the desired binary weighted voltage. One unity capacitance can be always connected to ground imposing the full scale voltage to be $(2^n - 1)V_{ref}/2^n$ [34].

1.2.2 Capacitive DAC SAR ADCs

Implementing a SAR ADC using a capacitive divider as a DAC (CDAC) leads to some advantages. One of them is the inherent sampling: Fig. 1.8 shows a complete CDAC SAR ADC. Here the sample-and-hold function is performed directly by the DAC, which during the first phase of the conversion stores the input signal across all the capacitors. This scheme is also called charge redistribution SAR ADC, since the charge sampled at the beginning of the conversion cycle, during the conversion is redistributed on the capacitor array, obtaining a top plate voltage (V_{res}) close to zero (analog ground) at the end of the cycle. After the sampling phase, the total charge on the array is:

$$Q_{tot} = V_{in} \cdot 2^n \cdot C_u \tag{1.6}$$

The algorithm starts imposing the MSB to one, which means connecting the largest capacitor to V_{ref} and all the others to analog ground. In this configuration the flow of charge modifies the voltage on the top plate which become:

$$V_{res}(1) = \frac{V_{ref}}{2} - V_{in} \tag{1.7}$$

This voltage is exactly the difference between the MSB voltage and the input voltage. Therefore, the output of the comparator will be 1 or 0 depending only on the sign of this difference. After the decision, the first bit is set and the corresponding capacitor is then left to V_{ref} or connected to analog ground for all the other cycles.
After this, the search of the second bit can start: depending on the MSB, the new thresholds are $3V_{ref}/4$ or $V_{ref}/4$, respectively, leading the top plate to be:

$$V_{res}(2) = \frac{3V_{ref}}{4} - V_{in} \qquad or \qquad V_{res}(2) = \frac{V_{ref}}{4} - V_{in} \tag{1.8}$$

Once again this voltage is compared with analog ground, setting the value of the corresponding bit. These operations continue until all the n-bits are found [35].

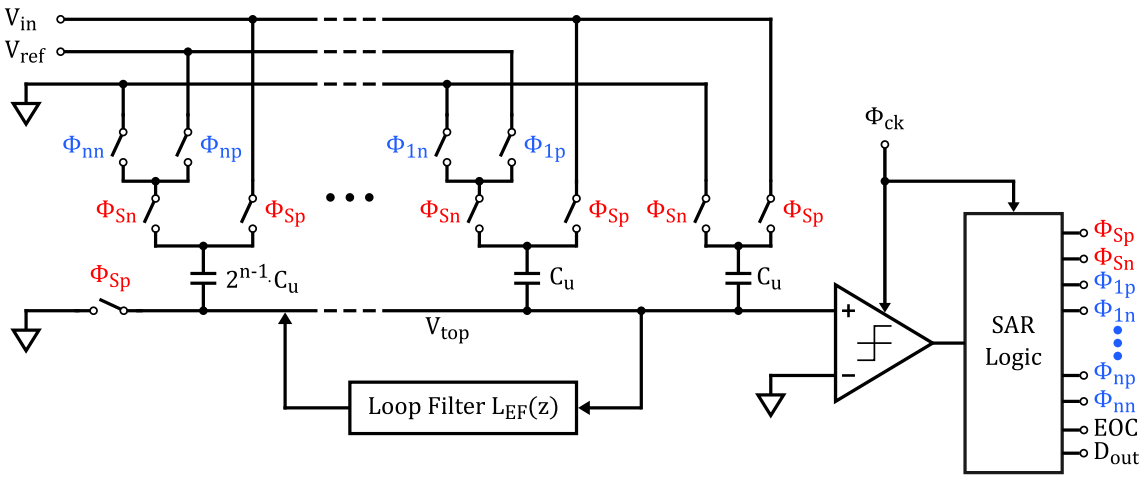


FIGURE 1.9: Conceptual schematic of an error-feedback CDAC SAR ADC.

1.3 Noise Shaping Techniques

Every time a signal is converted from the analog domain to the digital domain, a quantization error is introduced. By definition, the quantization error is the difference between the analog signal and the quantized digital one. It arises from the rounding or the truncation of the digitized signal and, in general, is correlated with the signal itself. The easiest way to reduce this type of error is, of course, increasing the resolution of the ADC. One of the main problems, that CDAC SAR ADCs have, is the limited resolution. Indeed, increasing the resolution by one bit means doubling the overall capacitance of the DAC and, consequently, the occupied area. As rule of thumb, when there is the need for more than 10 bits, CDAC SAR ADCs become not very efficient. One method to overcome this problem is the noise shaping technique. Indeed, it is possible to increase the overall SNR and, consequently, the effective number of bits of an ADC by altering the spectral shape of the quantization error in such a way that it is no longer uniformly distributed in band, but it is pushed at a higher frequency. Combining this effect with oversampling techniques and filtering the out-of-band spectral components, it is possible to increase the resolution. In general, in a CDAC SAR ADC (Fig. 1.8), one extra switching of the array based on the final comparator decision produces a residue voltage, V_{res}, at the top plate node that is given by:

$$V_{res} = Q_e + n_{comp}, \tag{1.9}$$

where Q_e is the quantization error and n_{comp} is the input referred noise of the comparator. This quantization error generation characteristic is exploited to introduce noise shaping in SAR ADCs. There are two main topologies that realize NS-SAR ADCs: the **Error-Feedback (EF)** topology and the **Feed-Forward (FF)** topology. Synchronous SAR converters are discrete time systems and therefore it is possible to analyze them using the Z-transform. In this thesis, from now on, unless otherwise specified, all the block diagram equations and calculation will be performed in the Z-domain.

1.3.1 Error-Feedback Noise Shaping SAR ADCs

In a CDAC SAR ADC, simply adding the quantization error, Q_e, to the next input sample realizes the long established error feedback modulator with inherent noise shaping. Figure 1.9 shows the conceptual implementation of an error feedback noise shaping SAR

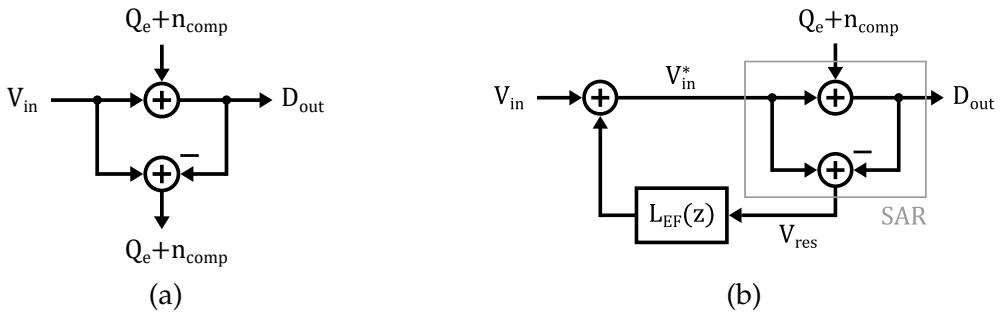


FIGURE 1.10: Conceptual signal flow diagram of (a) the SAR ADC and (b) the error-feedback SAR ADC.

ADC. In general, it is always possible to define the digital output as:

$$D_{out} = STF \cdot (V_{in}) + NTF \cdot (Q_e + n_{comp}) \tag{1.10}$$

where STF is the Signal-Transfer-Function and NTF is the Noise-Transfer-Function that shapes the quantization error. The quantization error is processed by a loop filter, $L_{EF}(z)$, before being fed back into the next input sample. Analyzing the flow diagram in Fig. 1.10b it is possible to derive the following equations:

$$\begin{cases} D_{out} = V^*_{in} + (Q_e + n_{comp}) \\ V^*_{in} = V_{in} - (V^*_{in} - D_{out}) \cdot L_{EF}(z) \end{cases} \tag{1.11}$$

Solving the system for D_{out}:

$$D_{out} = V_{in} + (1 - L_{EF}(z)) \cdot (Q_e + n_{comp}). \tag{1.12}$$

Using (1.10), it is possible to derive that

$$STF = 1 \qquad and \qquad NTF = 1 - L_{EF}(z), \tag{1.13}$$

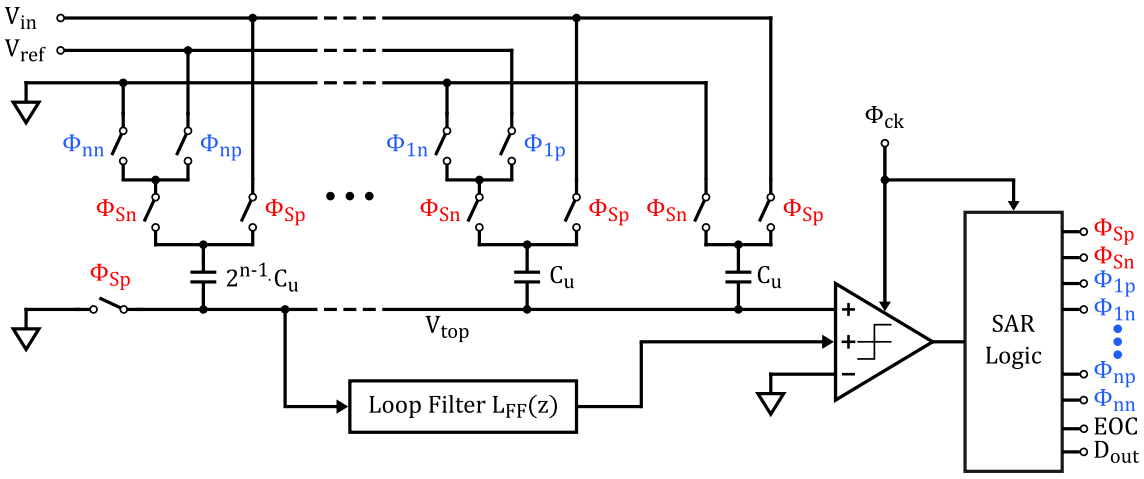


FIGURE 1.11: Conceptual schematic of a feed-forward CDAC SAR ADC.

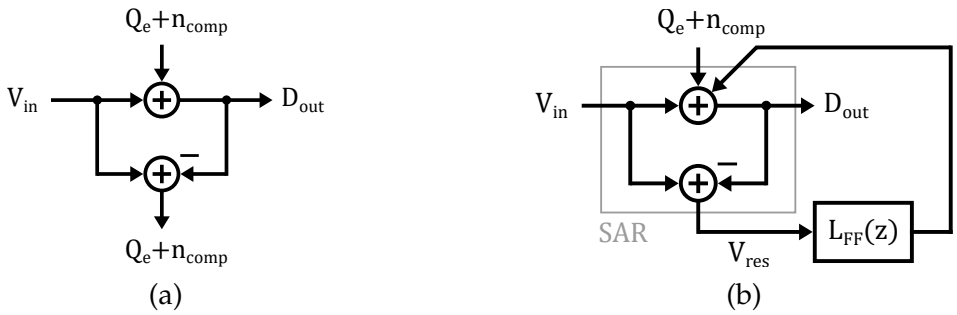


FIGURE 1.12: Conceptual signal flow diagram of (a) the SAR ADC and (b) the feed-forward SAR ADC.

So the signal is therefore left untouched while the noise can be shaped depending on the loop filter transfer function.

1.3.2 Feed-Forward Noise Shaping SAR ADCs

Differently from the other implementation, the Feed-Forward NS SAR ADC, filters the quantization error before feeding it forward to an additional comparator input (Fig. 1.11). This works as a summation node, prior to making a decision. From Fig. 1.12b it is possible to derive the overall transfer function:

$$\begin{aligned} & D_{out} = V_{in} + (Q_e + n_{comp}) + (V_{in} - D_{out}) \cdot L_{FF}(z) \\ \Rightarrow \quad & D_{out} = V_{in} + \frac{1}{1 + L_{FF}(z)} (Q_e + n_{comp}). \end{aligned} \tag{1.14}$$

This leads to:

$$STF = 1 \qquad and \qquad NTF = \frac{1}{1 + L_{FF}(z)}. \tag{1.15}$$

Also in this case, the signal is not filtered while the quantization noise can be shaped depending on the loop filter function. For both topologies, a more detailed and extensive discussion can be seen in [36].

1.3.3 Active Loop Filter Solutions

The main role of the loop filter transfer function is to shape the quantization error to improve the converter performance. To achieve this, it is necessary to suppress in-band noise, having a strong attenuation inside the signal bandwidth, while amplifying the high frequency components. The easiest way to obtain this, is to use an ideal differentiator transfer function. For discrete-time systems, it results in having the NTF in the form of $(1 - z^{-1})^n$, where n is the order of the noise shaping. For instance, by imposing a first and second order noise shaping to the EF and the FF loop filter, the following results are derived:

$$L_{EF}^{(1)}(z) = z^{-1}, \qquad L_{EF}^{(2)}(z) = z^{-1}(2 - z^{-1}), \tag{1.16}$$

$$L_{FF}^{(1)}(z) = \frac{z^{-1}}{1 - z^{-1}}, \qquad L_{FF}^{(2)}(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2}. \tag{1.17}$$

In a NS-SAR ADC, the resolution, besides the type and the order of the loop filter, depends on several factors, including the number of bits of the SAR converter itself and the

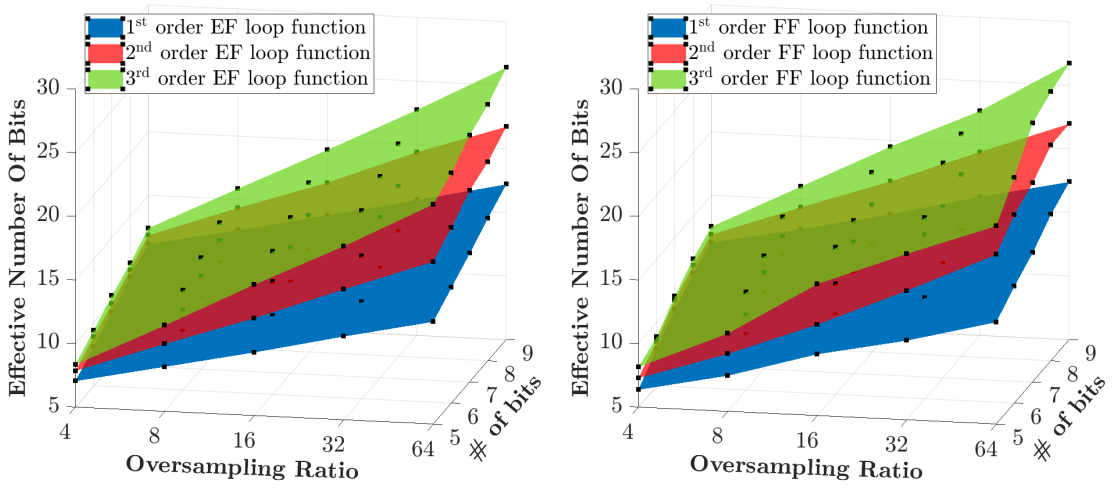


FIGURE 1.13: Resolution as a function of OSR and number of bits for (a) the active error-feedback SAR ADC and (b) the active feed-forward SAR ADC.

OSR. Figure 1.13 shows the final resolution (expressed in ENOB) as a function of these three factors for both topologies. It can be seen that increasing both the OSR and the number of bits, an enhancement of the ENOB is obtained. However, it must be remembered that raising the OSR leads to an increase of the sampling frequency and that adding one extra bit without degrading the matching performance translates in doubling the overall capacitance, i.e. the area. In addition to this two variables, the order of the loop filter function plays a significant role for the overall resolution.

Among the two topologies, EF-NS-SAR is the simplest one in terms of loop filter implementation, having only a FIR filter. The residue extraction can be done passively [37] or actively, using, for instance, a low-power dynamic amplifier [38]. The first solution implies filtering back the residue as it is and then adding it to the input signal in the next cycle with the aid of a high-gain closed-loop amplifier that works as a summation point. This solution ensures accurate control on the placement of the transfer function poles and zeros allowing reaching very good resolution. Drawbacks are that closed-loop amplifiers are not particularly power efficient and do not scale well with latest nm CMOS processes. Also special attention needs to be paid on their output noise contribution since it is added directly at the ADC input. The second solution amplifies the residue while it is sampled, in order to compensate the attenuation that arise during summation with the input signal. Current-mode solutions have also been implemented [39]. Due to their structure, FF-NS-SAR ADCs are in general more robust to loop gain mismatch, since the combination of FIR and IIR filters grants a high loop gain. On the other side these filters require high Gain-Bandwidth Product (GBW) amplifiers that are, in general, very power hungry. An n^{th} order IIR filter requires, roughly, n amplifiers, leading to have a direct trade-off between loop filter order (and thus resolution) and power consumption.

1.3.4 Passive Loop Filter Solutions

The main benefits of SAR ADCs, which are their ability to scale down dynamic power with clock frequency and area with the advancement of the technological nodes, are lost

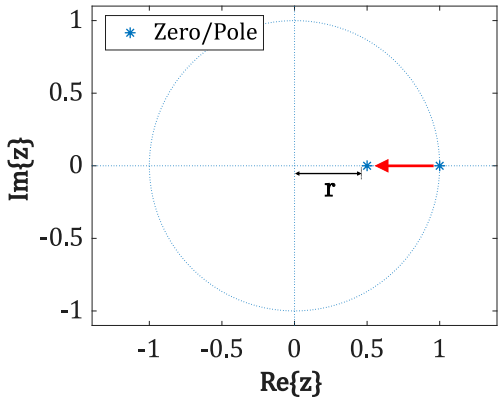


FIGURE 1.14: Zeros/poles shift on the Z-plane for passive transfer functions.

when active integrators are used in NS-SAR topologies. SAR converters are inherently low-power architectures, since most of the energy is dissipated by the comparator, while the DAC and the logic consume only a small amount of dynamic power. Adding power hungry circuits, as operational amplifiers, implies that the overall consumption raises significantly. To overcome this problem, passive loop filter solutions have been introduced [40, 41]. The biggest drawback of using fully passive loop filters is that, without amplification, losses in the residue transfer severely degrade the overall resolution. In practical terms, as shown in Fig. 1.14, this results in the impossibility of having singularities (zeroes and poles) located on the unit circle in the Z-plane. If a differentiator transfer function is used, the final result is a real differentiator (with losses) and not an ideal one as desired, leading to

$$NTF = (1 - rz^{-1})^n, \tag{1.18}$$

where $r < 1$ is the new distance from the center of the zeros/poles. Imposing first and second order passive transfer functions to both topologies leads, respectively, to:

$$L_{EF}^{(1)}(z) = rz^{-1}, \qquad L_{EF}^{(2)}(z) = rz^{-1}(2 - rz^{-1}), \tag{1.19}$$

$$L_{FF}^{(1)}(z) = \frac{rz^{-1}}{1 - rz^{-1}}, \qquad L_{FF}^{(2)}(z) = \frac{rz^{-1}(2 - rz^{-1})}{(1 - rz^{-1})^2}. \tag{1.20}$$

The choice of r is not straightforward: A simple first order passive loop filter, for instance, is generally implemented exploiting the charge sharing principle, leading to

$$r = \frac{C_{res}}{C_{DAC} + C_{res}}, \tag{1.21}$$

where C_{res} is the capacitor used to perform both the storage and the transfer of the residue and C_{DAC} is the total capacitance of the CDAC. This holds true for both topologies [41]. From (1.21) it can be seen that just having $r = 0.5$ means doubling the total capacitance and thus the area. Fig. 1.15 shows the resolution as a function of the OSR and the number of bits of the SAR core for a 1^{st}, 2^{nd} and 3^{rd} order loop filter functions choosing $r = 0.5$. Comparing it with Fig. 1.13 it can be noted that a substantial reduction in the final resolution occurs.

In spite of the lower resolution, a passive EF-NS-SAR ADC consumes far less power

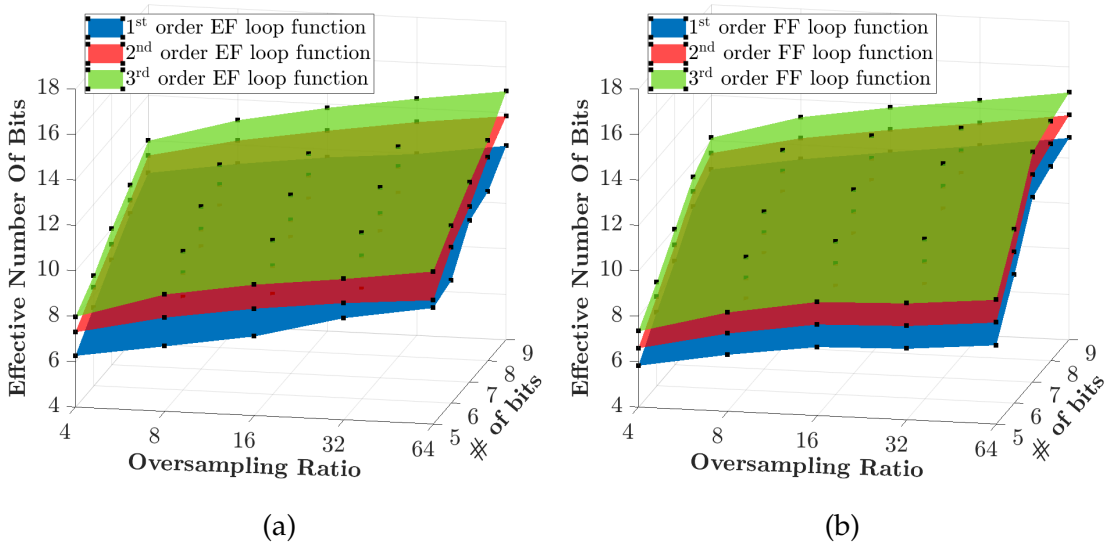


FIGURE 1.15: Resolution as a function of OSR and number of bits for passive (a) error-feedback SAR ADCs and (b) feed-forward SAR ADCs, choosing $r = 0.5$.

with respect to its active counterpart. Given that, to implement the transfer functions depicted in (1.19) and (1.20), a simple switched-capacitor network can be used (only dynamic power is consumed). Particular attention needs to be paid on the choice of the coefficients since higher values of r lead to a greater area occupation.
In a FF-NS-SAR ADC it is possible to realize all the coefficients needed for implementing (1.19) and (1.20) simply exploiting the comparator inputs as weighted summation points [42]. This implementation has become very popular in the literature since it takes advantage of an active block, such as the comparator, to amplify the signals, without resorting to additional amplifiers. Among the topologies presented above, this thesis focuses on the design and exploration of the EF architecture. Although feed-forward structures are generally known to offer better performance, especially in fully-passive implementations due to their superior noise transfer function shaping, this work deliberately chooses the EF topology for its unique advantages and research potential. One of the key motivations behind this choice is the architectural simplicity of EF designs. The separation between the SAR quantization loop and the feedback path allows for easier integration and design flexibility. The feedback network can be optimized for noise shaping without heavily impacting the rest of the system, which can be beneficial in terms of design modularity and overall stability. While FF topologies are extensively covered in literature, EF designs are still not as thoroughly studied, especially for low-power implementations. This opens up space for innovation and original contributions. Investigating this alternative architecture provides the opportunity to evaluate its practical trade-offs and possibly uncover configurations where EF can become a competitive solution, especially in applications with strict power and area constraints [36].

Chapter 2

MKI Test Chip Design Steps

RELYING on the preliminary analysis carried out in MATLAB® environment to define the main design parameters, in this chapter, the proposed Quasi-Passive Error-Feedback Noise-Shaping SAR ADC testchip, named *MKI*, is described, passing through the steps that led to the final silicon implementation. Moreover, the transistor-level description of all the main blocks is carried out.
According to the targets set by TDK-Invensense, the proposed ADC needs to fulfill the following requirements:

- Input signal bandwidth: $4 \div 8\,\text{kHz}$;
- Overall resolution: $12 \div 13\,\text{bits}$;
- Full-Scale: $200 \div 600\,\text{mV}_{\text{pp}}$;
- SAR bits: $4 \div 8\,\text{bits}$;
- Supply Voltage: $V_{DD} = 1.2\,\text{V}$;
- SNDR @ -36 dBFS (94 dBSPL): $40 \div 48\,\text{dBA}$;
- SNR @ 0 dBFS (140 dBSPL): $76 \div 84\,\text{dBA}$;
- THD @ Full-Scale: $\simeq 5\,\%$;
- Power $\simeq 10\,\mu\text{W}$;
- Group Delay $< 20\,\mu\text{s}$;
- Smallest area occupation possible;
- Technology: 65 nm BCDlite.

2.1 Preliminary Analysis

To approach a design from scratch, it is considered good practice to start with ideal models. Noise-Shaping SAR A/D converters are discrete time systems and they can be modeled in MATLAB® and Simulink® environments. Given the project specifications, it is necessary to evaluate a series of trade-offs in order to define the three main design parameters:

- The number of bits in the SAR quantizer;
- The OverSampling Ratio (OSR);
- The order of loop filter.

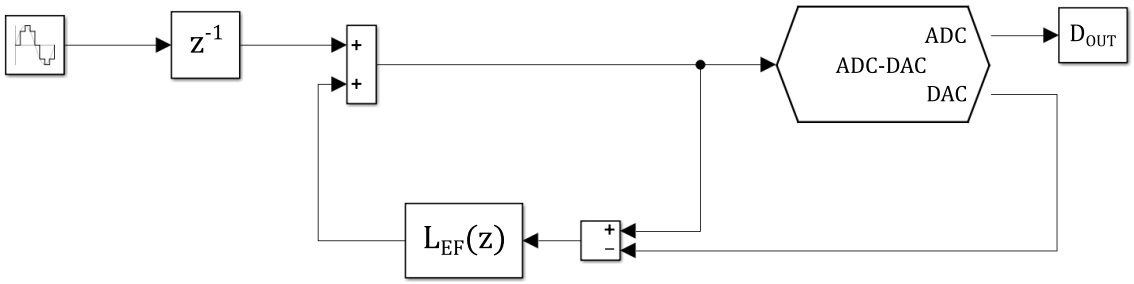


FIGURE 2.1: Simulink® block diagram of a generic error-feedback NS-SAR ADC.

An ideal Simulink® block diagram of a generic error-feedback NS-SAR converter, illustrated in Fig. 2.1, is employed to evaluate the system performance as a function of the previously defined design parameters. To model the behavior of the n-bit SAR quantizer, a custom block referred to as *ADC-DAC* is implemented. This block performs analog-to-digital conversion by mapping the analog input signal to a digital code, based on a specified set of threshold levels. Additionally, it reconstructs the analog signal from the digital code, thereby generating an output that inherently includes quantization error. The residue voltage, V_{res}, is obtained by subtracting this reconstructed analog output (denoted as *DAC* in the figure) from the original input signal. By applying a suitable loop filter characterized by the transfer function $L_{EF}(z)$, the final digital output word is computed as described in (1.12).

2.1.1 Trade-off Between Oversampling Ratio and Number of SAR bits

In traditional NS-SAR ADC architectures, a fundamental design trade-off arises between the oversampling ratio and the intrinsic resolution of the SAR quantizer, typically expressed in terms of its number of bits. This trade-off directly influences the overall resolution and signal fidelity of the converter. Understanding and strategically managing this trade-off is crucial for optimizing ADC performance under constraints such as power, area, and sampling frequency. As explained in Sec. 1.3, combining the benefits of oversampling with the noise-shaping technique, it is possible to increase the overall resolution of a n-bit SAR ADC. The oversampling ratio is defined as the ratio between the sampling frequency and twice the signal bandwidth. Increasing the OSR enhances the resolution by pushing more quantization noise outside the band of interest. For a first-order loop filter transfer function, the in-band noise power decreases roughly with the cube of OSR, leading to an SNDR improvement of approximately 9 dB per doubling of OSR. In a second-order NS-SAR converter, the improvement becomes more pronounced (around 15 dB per OSR doubling) due to the steeper high-pass filtering of the noise. The choice of the OSR is not straightforward but depends on other factors such as the number of the bits of the SAR itself or the maximum frequency reachable inside the circuit. On the other hand, each additional bit in the SAR quantizer theoretically reduces quantization noise by a factor of four, corresponding to an SNDR improvement of approximately 6.02 dB per bit. Unlike OSR-based improvements, which rely on shaping and decimation, SAR resolution enhancement is direct and deterministic, independent of digital post-processing. However, increasing SAR resolution implies more complex comparator control logic, longer conversion time, larger capacitive DAC arrays, and increased sensitivity to component mismatches and thermal noise, especially as designs approach 12–14 bits and beyond.

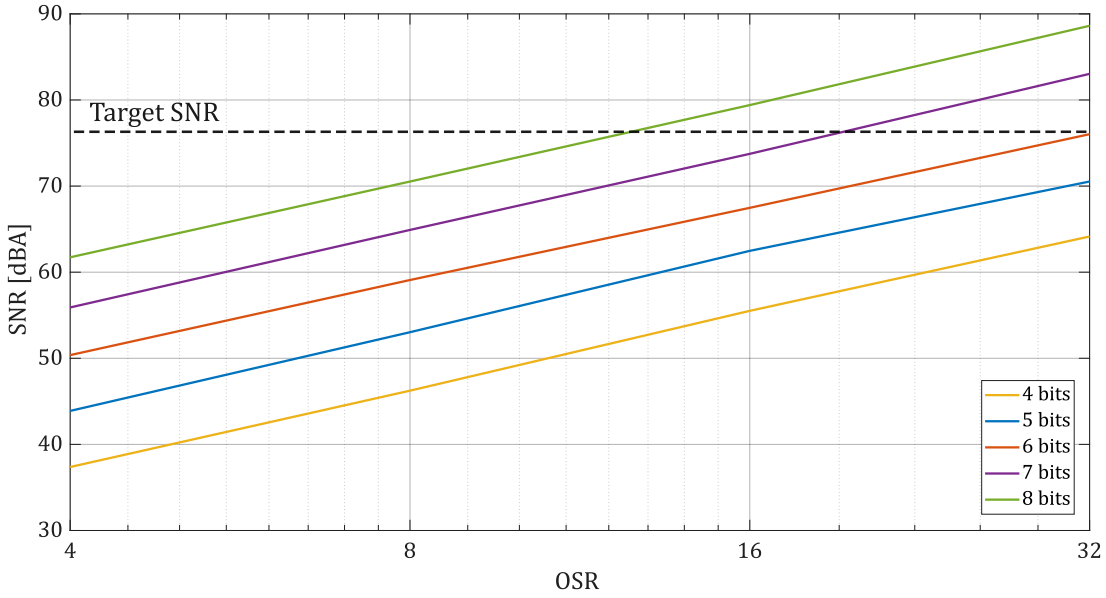


FIGURE 2.2: SNR of an ideal first order loop filter EF-NS-SAR as a function of OSR and the number of bits in the quantizer.

In this project, the input signal is characterized by a maximum bandwidth of 8 kHz. According to the Nyquist–Shannon sampling theorem, in order to accurately reconstruct the signal without aliasing, the sampling frequency (F_s) must be at least twice the maximum frequency component of the signal. Consequently, the minimum required sampling frequency is 16 kHz. However, to improve performance, oversampling is employed and the actual sampling frequency adopted is defined as follows:

$$F_s = OSR\,(2 \cdot BW). \tag{2.1}$$

To avoid clock frequencies that would exceed tens of megahertz, thus complicating the design and increasing power consumption, the oversampling ratio is limited to a maximum value of 32. For the purpose of clarity and analytical tractability, this section focuses exclusively on the analysis of active loop filters of first and second order. As previously discussed in Sections 1.3.1 and 1.3.3, by imposing first and second order differentiators for the noise transfer function, as defined in (1.13), the corresponding loop filter transfer functions can be derived, as presented in (1.16). These loop filter functions are then implemented within a Simulink® model to evaluate the resolution of the system as a function of both the oversampling ratio and the number of bits in the SAR quantizer. Figure 2.2 illustrates the resulting resolution, expressed in terms of signal-to-noise ratio, for a first order loop filter in the error-feedback noise-shaping SAR architecture. As anticipated, increasing either the OSR or the number of bits in the quantizer leads to an improvement in SNR. The design specifications require that, at full-scale input (0 dBFS), the analog-to-digital converter must achieve an SNR in the range of 76 dBA to 84 dBA (A-weighted decibels). To meet this requirement, a quantizer with at least 7 bits of resolution is necessary. It is important to emphasize that the analysis presented here is based on an idealized model, which neglects non-idealities such as electronic noise and distortion. As a result, in practical implementations, it is essential to incorporate appropriate design margins to prevent potential underestimation of the required specifications and to ensure robust system performance. Employing a second order transfer function, it is

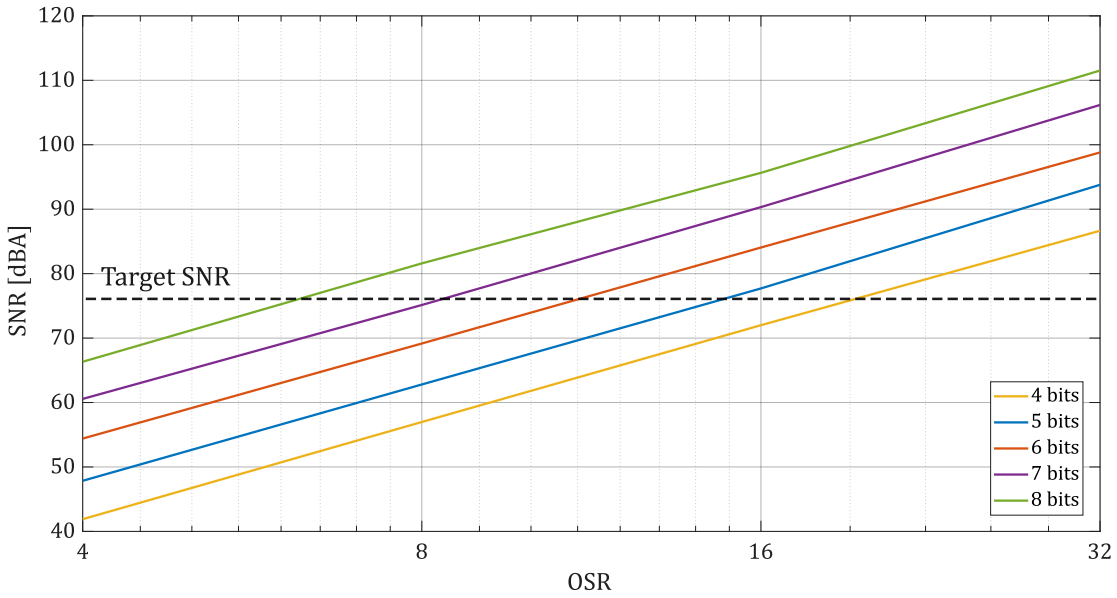


FIGURE 2.3: SNR of an ideal second order loop filter EF-NS-SAR as a function of OSR and the number of bits in the quantizer.

possible to observe an overall improvement of the resolution (Fig. 2.3). Choosing 16 or 32 as OSR, 6 or 5 bits are sufficient to achieve more than 76 dBA of SNR, respectively.

2.1.2 Jitter Tolerance and Group Delay Estimation

Another critical aspect to consider once the OSR is defined is the tolerance to clock jitter. In this section, an analysis of the robustness of both topologies with respect to jitter is presented. Jitter is defined as the deviation from true periodicity in a periodic signal. In the Simulink® model, it is possible to simulate the presence of jitter in the clock signal. Such random fluctuations can lead to an overall degradation of the final SNR, and consequently, of the ENOB. The maximum allowable clock frequency for the ADC is on the order of a few MHz, corresponding to a minimum clock period below 1 µs. As a result, jitter values exceeding several tens of nanoseconds are considered unlikely. Figure 2.4 illustrates the SNR degradation as a function of the jitter amplitude for a second-order error-feedback SAR ADC. It can be observed that a 6-bit SAR quantizer provides improved jitter tolerance; however, this improvement is insufficient to justify the additional bit, which would result in a doubling of the CDAC area. By inspecting the schematic of the topology shown in Fig. 2.1, the group delay of the signal path can be estimated. Considering that the signal transfer function is unitary, as demonstrated in (1.13), the overall delay is determined solely by the sampling period:

$$\tau_g = T_s = \frac{1}{f_s} = \frac{1}{2 \cdot OSR \cdot BW} \tag{2.2}$$

Since the bandwidth is fixed, the only variable affecting the group delay is the OSR, resulting in the following values:

$$\begin{aligned} \tau_g &\simeq 4\,\mu s \qquad for \quad OSR = 16 \\ \tau_g &\simeq 2\,\mu s \qquad for \quad OSR = 32. \end{aligned} \tag{2.3}$$

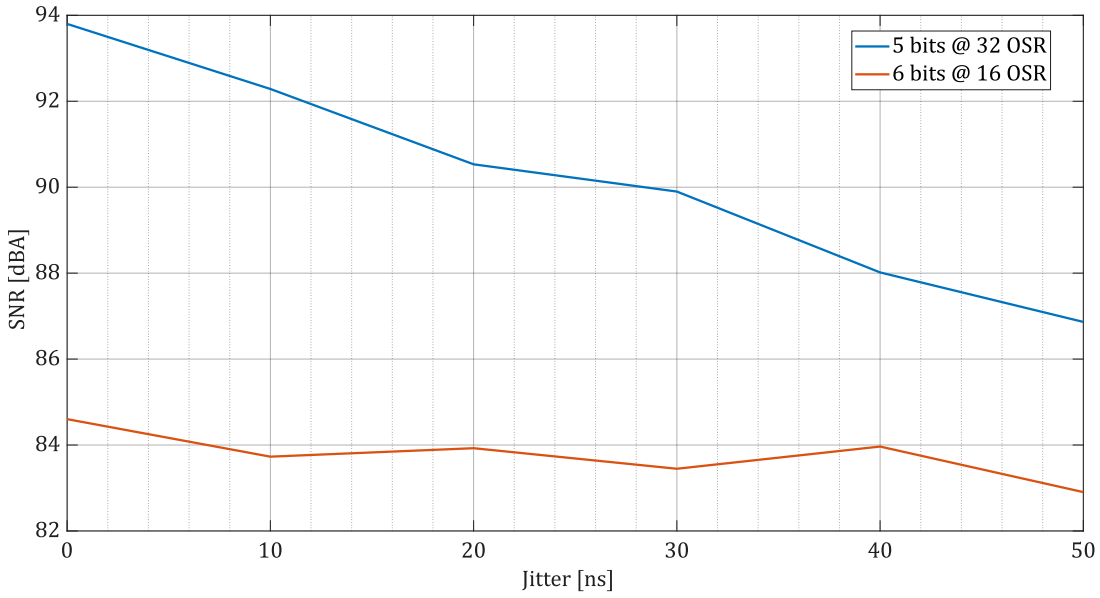


FIGURE 2.4: SNR degradation in an ideal second-order EF-NS-SAR architecture as a function of increasing clock jitter values.

2.1.3 Loop Gain Error

The proposed ADC adopts a closed-loop configuration. In this architecture, the residue signals processed by the loop filter must exhibit high accuracy, particularly when the target resolution exceeds 12 bits. As discussed in Sec. 1.3, the residue present at the top plate of the capacitor array corresponds to the quantization error, which, in the case of a conventional SAR ADC, lies within the range of $\pm LSB/2$. The least significant bit is defined by:

$$LSB = \frac{V_{FS}}{2^n} \tag{2.4}$$

where V_{FS} is the full-scale voltage and n denotes the resolution of the SAR ADC in bits. Given a full-scale voltage in the range of 200 mV to 600 mV and a resolution of 5 to 6 bits, the LSB falls within the order of a few millivolts. However, when oversampling and noise-shaping techniques are employed, the effective resolution increases significantly, leading to a substantial reduction in the quantization step size. Transitioning from an ENOB of $5 \div 6$ bits to more than 12 bits implies a reduction in the quantization noise by a factor of approximately $2^7 \div 2^6$. As a result, the loop filter must be capable of accurately processing signals with amplitudes in the sub-millivolt range. To assess the impact of loop gain mismatch on the overall signal-to-noise ratio, a controlled gain error was introduced into the loop transfer function. Starting from the nominal gain (0% error), which is required for a second-order EF-NS-SAR to maintain optimal filtering characteristics, the variation in SNR was analyzed up to a gain error of 10%, as illustrated in Figure 2.5. The results indicate that, using the target SNR is maintained for loop gain errors below 1.5%, a margin that is well within the capabilities of practical circuit implementations. This tolerance demonstrates the inherent robustness of the proposed converter topology against variations in loop gain.

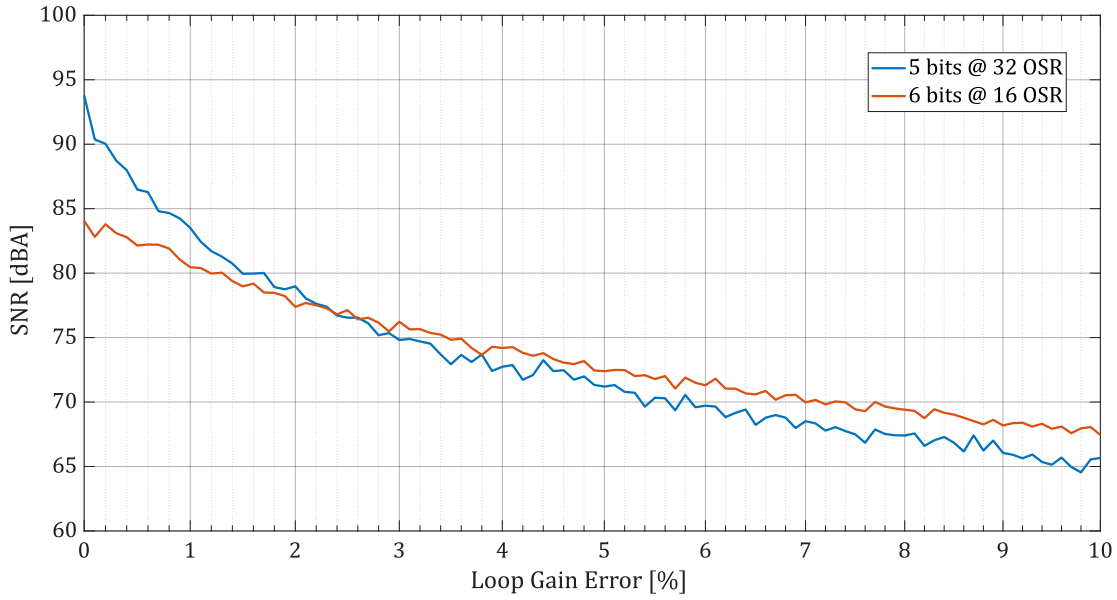


FIGURE 2.5: SNR degradation in an ideal second-order EF-NS-SAR architecture as a function of increasing loop gain error.

2.1.4 Matching Analysis

Robustness against mismatch is a significant parameter to take into account in CDAC SAR circuits. As explained in Section 1.2.2, in these type of converters, the main conversion operations rely on DAC capacitive ratios. As the number of bits increase, i.e. the resolution, the LSB voltage decrease according to (2.4). The lower the voltage the circuit must handle, the more precise the capacitive ratio must be. It becomes clear that if there are even very small variations of the capacitance values, the overall results will be wrong.

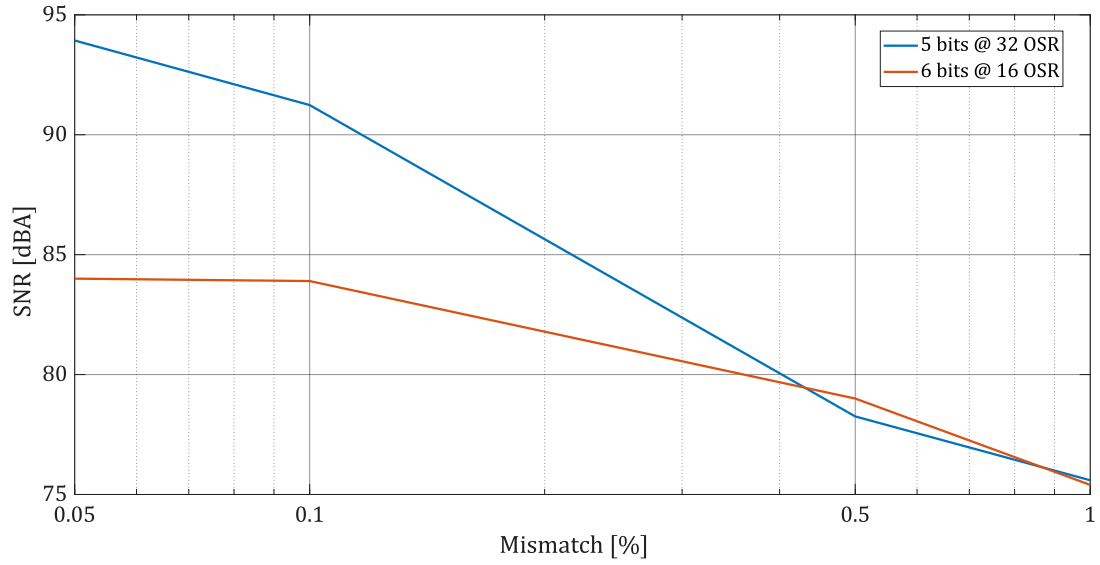


FIGURE 2.6: SNR degradation in an ideal second-order EF-NS-SAR architecture as a function of increasing mismatch on the DAC capacitors.

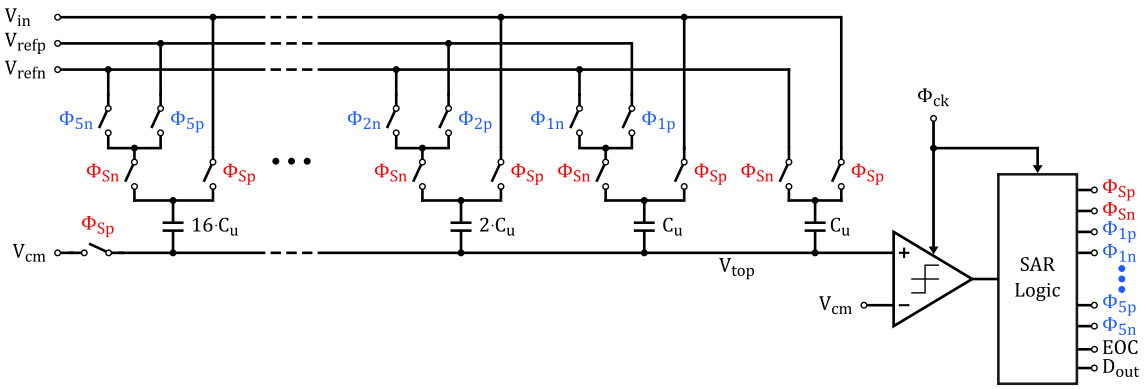


FIGURE 2.7: Schematic of a 5-bits bottom-sampling CDAC SAR.

In monolithic Integrated Circuits (IC), depending on the technology, mismatch between devices occurs systematically and can be reduced through proper design techniques. A preliminary study on the matching of capacitors is performed on the Simulink® model. The block ADC-DAC (Fig. 2.1) mimics the behaviour of a SAR converter and it also simulates a possible mismatch between the capacitors, generating random capacitance values according to the matching parameters provided.

This analysis allows understanding how much, in percentage, the capacitors can mismatch, independently of technology and total capacitance. Figure 2.6 shows the variation of the SNR given a mismatch between the capacitors of 0.05%, 0.1%, 0.5% and 1%. It is possible to observe that having an extra bit leads to a lower degradation for higher level of mismatch. In order to meet the specifications, a mismatch below 0.5% is required.

2.2 Proposed Architecture

After the preliminary analysis and simulations conducted in the previous section, a 5-bit capacitive digital-to-analog converter was selected as the core component of the oversampled noise-shaping analog-to-digital converter. Given that area occupancy is a critical design parameter, opting for a 5-bit instead of a 6-bit CDAC reduces the area by approximately half. While it is true that an additional bit can improve capacitor matching (as shown in Fig. 2.6) and reduce SNR degradation due to loop gain errors (Fig. 2.5) and clock jitter (Fig. 2.4), the specifications for the system are still met with the 5-bit DAC. Therefore, the significant area overhead associated with an extra bit is not justified.

2.2.1 5-bits Bottom-Sampling Capacitive DAC SAR Converter

In Fig. 2.7, the schematic of the 5-bit synchronous SAR architecture is presented in detail. This figure illustrates the overall structure of the converter, where each functional block plays a crucial role in enabling accurate and efficient analog-to-digital conversion. As already introduced in the earlier sections of this thesis, the design strategy has been carefully oriented toward minimizing both power consumption and silicon area, since these two parameters represent critical constraints in modern integrated circuit design, especially in applications targeting low-power portable devices and high-density system-on-chip implementations.

To achieve these objectives, a single-ended design approach is adopted. While differential architectures are generally preferred in high-performance ADCs due to their

Specs	V_{DD}	V_{SS}	V_{refp}	V_{cm}	V_{refn}	Full-scale	LSB	BW
Values	1.2 V	0	900 mV	600 mV	300 mV	600 mV_{pp}	18.75 mV	8 kHz

TABLE 2.1: Design specification sum-up.

robustness against common-mode noise and improved linearity, in this case the single-ended solution provides a significant reduction in occupied area and circuit complexity. This choice results in having only one array of capacitors in the CDAC, thereby simplifying the layout and minimizing parasitic effects. The CDAC itself is implemented as a straightforward binary-weighted 5-bit array of capacitors. Its operation relies on exploiting two reference voltages, symmetrically placed around the common-mode, to establish the desired full-scale range, denoted as V_{FS}. Considering the adopted technology, the nominal supply voltage for the digital core is set to 1.2 V. In order to guarantee proper analog operation and ensure symmetry in the voltage swing, the analog ground, hereafter referred to as the common-mode voltage V_{cm}, is chosen equal to half of the supply, i.e., 600 mV. The two reference voltages, V_{refp} and V_{refn}, are then symmetrically centered around this value. Specifically, they are set to 900 mV and 300 mV, respectively. This configuration leads to a full-scale range of $V_{FS} = 600\,mV$. Such a choice ensures that the input signal can swing around the common-mode without exceeding the supply limits, thereby guaranteeing linear behavior of the CDAC and reliable decisions from the comparator. From equation (2.4), the resolution step (LSB), can be calculated as:

$$LSB = \frac{V_{FS}}{2^n} = \frac{600\,mV}{32} = 18.75\,mV \tag{2.5}$$

This value represents the smallest voltage variation that can be distinguished by the converter, directly impacting its quantization error and overall accuracy. The main design specifications of the SAR converter are summarized in Tab. 2.1, where the trade-offs among resolution, speed, and power efficiency are clearly highlighted. The operation of the SAR is coordinated by the digital control block, known as the SAR logic. This unit governs the entire sequence of operations, ensuring that the timing requirements for correct DAC functionality are strictly met. As thoroughly explained in Sec. 1.2, the conversion procedure can be divided into two distinct phases: the sampling phase and the bit-cycling phase, where the actual binary search algorithm is performed. The timing behavior of the circuit is illustrated in Fig. 2.8, which depicts the complete sequence of events during a full conversion cycle. During the sampling interval, the switches Φ_{Sp} and its inverted counterpart Φ_{Sn} are driven to logic levels '1' and '0', respectively. This configuration connects the capacitor array of the DAC between the input signal V_{in} and the common-mode voltage V_{cm}, allowing the instantaneous value of the input signal to be properly sampled and stored as charge in the capacitors. Once the sampling phase is completed, the system transitions into the conversion phase. At this point, Φ_{Sp} is driven low ('0') while Φ_{Sn} is driven high ('1'), effectively disconnecting the input from

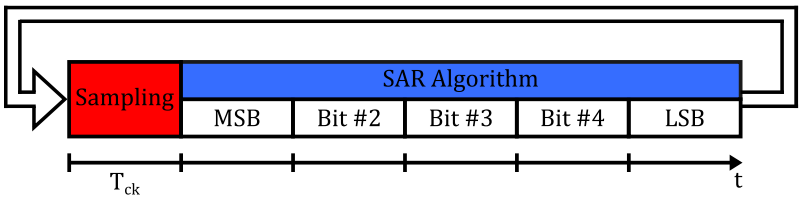


FIGURE 2.8: Timing diagram of a 5-bits SAR converter.

the CDAC and freezing the sampled charge. The conversion then begins by forcing the most significant bit to logic '1' through the control signal Φ_{5p}. This action redistributes the charge within the CDAC according to equation (1.7), thereby producing an analog output voltage that is compared with the sampled input by the comparator. The comparator generates a decision indicating whether the tentative DAC output is higher or lower than the actual input. Based on this result, the digital logic either confirms the MSB as '1' or resets it to '0'. The algorithm then continues in the same fashion for each subsequent bit, progressively refining the approximation of the input voltage. In each iteration, the corresponding capacitor is toggled according to the binary search procedure, and the comparator provides the decision needed to update the digital word. This iterative process is repeated until all 5 bits have been resolved, ultimately converging to the best digital approximation of the sampled input. At the conclusion of the conversion, the End Of Conversion (EOC) signal is asserted. This flag not only indicates that the conversion process has been successfully completed, but also validates the availability of the output digital word, D_{out}. The presence of the EOC signal is fundamental for synchronization with subsequent digital processing blocks or system-level controllers, as it ensures that the data is stable and ready for further use. In this way, the SAR ADC provides a robust, area-efficient, and low-power solution for moderate-resolution conversion tasks, demonstrating how careful architectural and design choices directly influence system performance.

2.2.2 Charge-sharing Based Architecture

In order to implement the noise-shaping architecture, an additional loop-filter circuit must be incorporated into the SAR converter to process the conversion residue and to shape the quantization error spectrum. In this work, a charge-sharing based, quasi-passive realization of the loop filter is proposed. The adopted topology is an hybrid solution that combine characteristics of both active and passive error-feedback loop filters discussed in Sec. 1.3.3 and Sec. 1.3.4 [37–42]. The architecture exploits a fully passive, charge-sharing technique to perform the filtering and inter-cycle residue transfer, while an active, Process-Voltage-Temperature (PVT) insensitive, open-loop amplifier is used to compensate for attenuation and to restore signal amplitude lost during the passive operations. This hybrid approach reduces the duty cycle and the active time of the amplifier (hence lowering power consumption), while still achieving the desired noise-shaping performance and preserving robustness against process, voltage, and temperature variations.

To clarify the operation and to motivate the circuit choices, it is convenient to proceed step-by-step from the desired discrete-time NTF to the switched-capacitor implementation of the corresponding loop transfer function. A second-order differentiator,

$$NTF(z) = (1 - z^{-1})^2, \tag{2.6}$$

is selected as the target NTF because it produces a second-order high-pass shaping of the quantization noise which is effective for improving in-band signal-to-noise ratio in low-to-moderate bandwidth converters. Using the error-feedback formalism introduced in (1.13), the relationship between the NTF and the second order error-feedback loop transfer function $L_{EF}(z)$ can be written as:

$$\begin{cases} NTF(z) = 1 - L_{EF}(z) \\ NTF(z) = (1 - z^{-1})^2 \end{cases} \quad \Rightarrow \quad L_{EF}(z) = 1 - (1 - z^{-1})^2 = 2z^{-1} - z^{-2}. \tag{2.7}$$

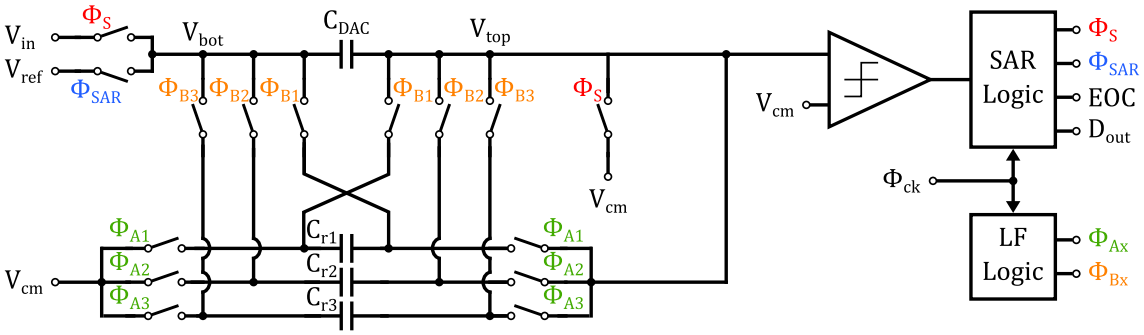


FIGURE 2.9: Simplified schematic of the converter with detail on the charge-sharing loop filter.

Equation (2.7) shows that the required transfer function is a causal, finite-impulse-response (FIR) polynomial composed of a $+2$ coefficient on the one-sample delayed residue and a -1 coefficient on the two-sample delayed residue. In other words, the filter must deliver a weighted combination of the residues from the previous two conversion cycles,

$$L_{EF}(z): \qquad +2 \cdot V_{res}[n-1] \; - \; 1 \cdot V_{res}[n-2]. \tag{2.8}$$

At the circuit level, the implementation of the desired transfer function requires explicit terms accounting for the charge-sharing process with the CDAC capacitance, C_{DAC}. Figure 2.9 shows the first draft of the converter schematic (the SAR CDAC is simplified in a single capacitor C_{DAC}) with the detailed loop filter charge-sharing circuit. The loop filter is composed by a network of three capacitors, C_{r1}, C_{r2}, and C_{r3}, and a digital logic (LF Logic), that dictates the timing of the switch phases. Capacitor C_{r1}, which is sized as twice the unit LF capacitance C_{LF}, stores the residue at the end of each conversion and transfers it to the CDAC in the subsequent cycle, thereby realizing the weighted contribution associated with $+2z^{-1}$. On the other side, capacitors C_{r2} and C_{r3}, each sized as C_{LF}, operate in an alternating (ping-pong) manner: while one stores the most recent residue sample, the other holds the previous one for an additional cycle before transferring it to the CDAC. In this way, the delayed contribution corresponding to z^{-2} is generated. The charge conservation equation at the V_{top} node can be expressed in the general form as

$$V_{res}[n] = \frac{C_{r1}\, V_{res}[n-1] \; - \; C_{rk}\, V_{res}[n-2]}{C_{DAC} + C_{r1} + C_{rk}}, \tag{2.9}$$

where C_{rk} denotes either C_{r2} or C_{r3}, depending on which of the two is active in the given cycle. By imposing the chosen capacitor ratios, namely $C_{r1} = 2C_{LF}$ and $C_{r2} = C_{r3} = C_{LF}$, and by introducing and factoring out the coefficient $\alpha = {}^{C_{LF}}/_{C_{DAC}}$, the above expression simplifies to:

$$\begin{aligned} V_{res}[n] &= \frac{2C_{LF} \cdot V_{res}[n-1] \; - \; C_{LF} \cdot V_{res}[n-2]}{C_{DAC} + 3C_{LF}} \\ &= \frac{2\frac{C_{LF}}{C_{DAC}} \cdot V_{res}[n-1] \; - \; \frac{C_{LF}}{C_{DAC}} \cdot V_{res}[n-2]}{\frac{C_{DAC}}{C_{DAC}} + 3\frac{C_{LF}}{C_{DAC}}} \\ &= \frac{2\alpha \cdot V_{res}[n-1] \; - \; \alpha \cdot V_{res}[n-2]}{1 + 3\alpha} \\ &= \frac{\alpha}{1+3\alpha} \cdot (2 \cdot V_{res}[n-1] \; - \; V_{res}[n-2]) \end{aligned} \tag{2.10}$$

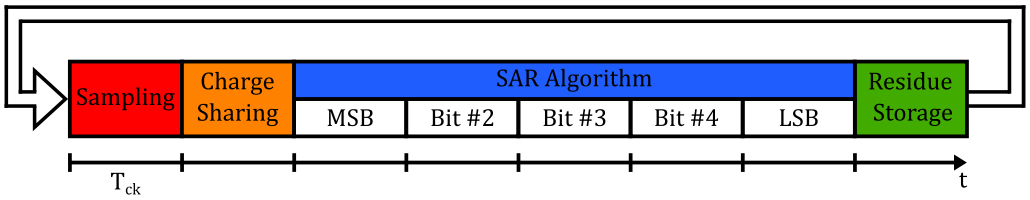


FIGURE 2.10: Timing diagram of the proposed converter.

This relation clearly shows that the loop filter produces a weighted combination of the past two residues, namely $2V_{res}[n-1] - V_{res}[n-2]$, normalized by the total capacitance used in the charge-sharing process. The ping-pong operation of C_{r2} and C_{r3} ensures that the two-cycle delayed sample $V_{res}[n-2]$ is always available when needed, without interfering with the direct $+2z^{-1}$ branch provided by C_{r1}. To better illustrate the dynamic behavior, in Fig. 2.10 the complete timing diagram is illustrated. To accommodate this residue manipulation, two more period must be included in a single conversion with respect to the simple Nyquist-rate 5 bits SAR converter. This eight period can be divided in four distinct phases, repeated every conversion cycle, are:

1. **Sampling phase:** at the beginning of the conversion cycle, the input signal is sampled on top of the CDAC capacitors;

2. **Charge sharing phase:** during this period the charge stored in C_{r1} is immediately transferred to the CDAC input node. Since C_{r1} has twice the unit capacitance, this transfer corresponds to applying a weight of $+2$ to the one-cycle delayed residue, thus realizing the $2z^{-1}$ term. While C_{r1} is transferring its charge, the pair C_{r2}–C_{r3} operate in ping-pong mode: the capacitor that was charged in the previous cycle remains floating, holding the residue value for one extra cycle, while the other is connected to the residue node and updated with the latest sample. In this way, the system continuously stores two different residues separated by one cycle;

3. **SAR Algorithm phase:** during this 5 clock periods, the binary search algorithm is performed leading to the generation of the output digital word;

4. **Residue Storage phase:** at the end of a conversion cycle, the residue generated by the SAR core is sampled and stored onto C_{r1}. Similarly, either C_{r2} or C_{r3} is also connected to the residue node, depending on the alternation scheme, in order to capture the current value for later use;

This explicit timing ensures that at every cycle the CDAC input receives both the $+2z^{-1}$ contribution from C_{r1} and, whenever available, the $-z^{-2}$ contribution from either C_{r2} or C_{r3}. The synchronization between these phases guarantees correct implementation of the NTF, and the following amplification phase restores the attenuated signal to the proper level for the next stage in the noise-shaping loop.

2.2.3 Charge-sharing Losses Regeneration

As previously anticipated, the charge-sharing operation between the loop filter and the CDAC inherently introduces non-negligible signal losses. This phenomenon arises because the charge stored on the loop filter capacitors is not transferred entirely to the CDAC node. Instead, according to the analytical expressions derived in (2.9) and (2.10), the transferred residue is effectively divided by a factor determined by the relative ratio between the loop filter capacitances and the DAC capacitance. This behavior is a direct

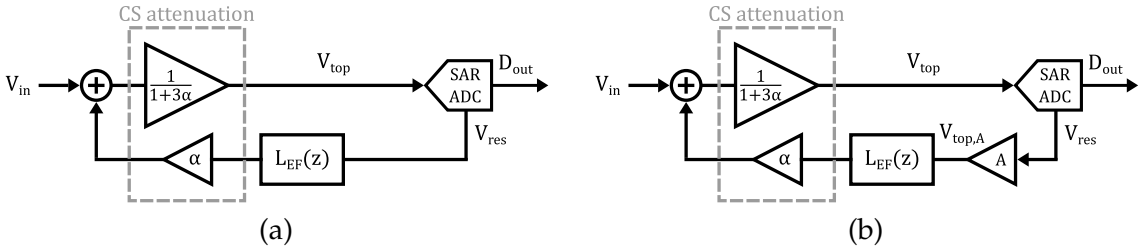


FIGURE 2.11: Block diagrams of (a) the error-feedback noise-shaping SAR with a fully-passive charge-sharing loop filter and (b) the proposed quasi-passive architecture.

consequence of the fundamental charge-sharing theory, which dictates that the resulting voltage after charge redistribution depends on the capacitive division of the involved elements. To compensate for these losses and restore the amplitude of the residue to its intended level, an amplification stage must be introduced within the feedback path of the converter. Such an amplification not only counterbalances the attenuation but also ensures that the implemented transfer function matches the ideal coefficients required by the noise-shaping loop. A conceptual illustration of this process is provided in Fig. 2.11. Specifically, in Fig. 2.11a, the block diagram of the SAR ADC with the fully-passive charge-sharing loop filter, as discussed so far, is reported. In this configuration, the signal losses introduced by the charge redistribution mechanism are explicitly highlighted with a dotted line, underlining their detrimental effect on the loop gain. Conversely, Fig. 2.11b shows the proposed quasi-passive solution, where the insertion of a dedicated amplification block within the loop restores the desired dynamics and rebalances the filter response. Rewriting the expression for V_{res} from (2.10) while including the amplification factor A, results in

$$V_{res}[n] = A \cdot \frac{\alpha}{1+3\alpha} \cdot \big(2 \cdot V_{res}[n-1] \; - \; V_{res}[n-2]\big), \tag{2.11}$$

where A denotes the voltage gain introduced in the feedback loop and α is the ratio between the loop filter capacitors and the CDAC capacitance, i.e., $\alpha = C_{LF}/C_{DAC}$. For completeness, by also including the contribution of the input signal V_{in}, the updated expression of the residue can be written as:

$$V_{res}[n] = \frac{V_{in}}{1+3\alpha} + A \cdot \frac{\alpha}{1+3\alpha} \cdot \big(2 \cdot V_{res}[n-1] \; - \; V_{res}[n-2]\big). \tag{2.12}$$

It is now evident that, if the amplification factor is chosen as

$$A = \frac{1+3\alpha}{\alpha}, \tag{2.13}$$

the attenuation introduced by charge sharing is exactly compensated. Under this condition, the final residue expression simplifies to:

$$V_{res}[n] = \underbrace{\frac{V_{in}}{1+3\alpha}}_{\text{input signal attenuation}} + \underbrace{2 \cdot V_{res}[n-1] \; - \; V_{res}[n-2]}_{\text{restored residue contribution}}. \tag{2.14}$$

From (2.14), it can also be observed that while the residue contributions are fully regenerated, the input signal undergoes an attenuation by a factor that directly depends on the

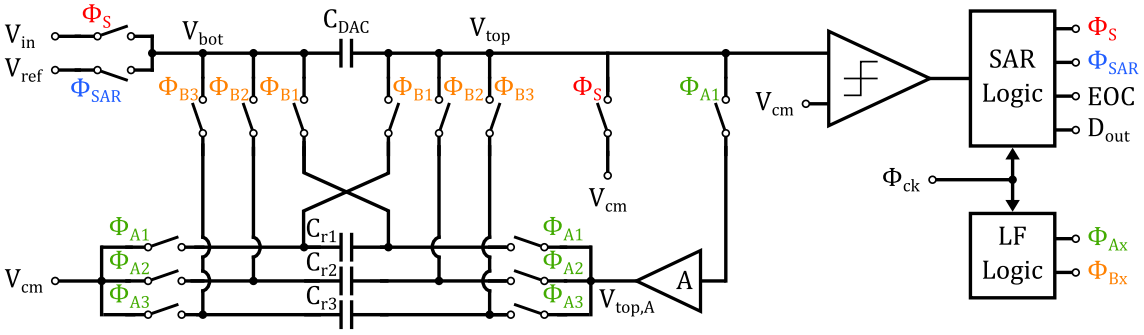


FIGURE 2.12: Simplified schematic of the proposed converter with detail on the quasi-passive loop filter.

ratio between the loop filter capacitors and the DAC capacitance (α). It is important to underline that this attenuation of the input signal does not represent a major drawback. In practice, the effect is equivalent to a simple re-scaling of the input range, which can be regarded as an adjustment of the overall full-scale value of the converter. As such, the impact on performance is negligible, and the operation of the ADC remains fully compliant with the intended design specifications.

In Fig. 2.12, the simplified schematic of the proposed quasi-passive converter is reported, while in Fig. 2.13 the complete timing diagram of the control phases governing its operation is illustrated. These two figures together provide a comprehensive view of both the circuit-level implementation and its temporal behavior. A number of important aspects can be highlighted in order to better understand the functioning of the system:

1. The phases ϕ_{A1} and ϕ_{B1}, which respectively control the charging and the subsequent charge-sharing of C_{r1}, are asserted at every single conversion cycle. In this way, capacitor C_{r1} is guaranteed to always store the most recent residue and transfer it during the following phase, thereby realizing the $+2z^{-1}$ term in the loop filter.

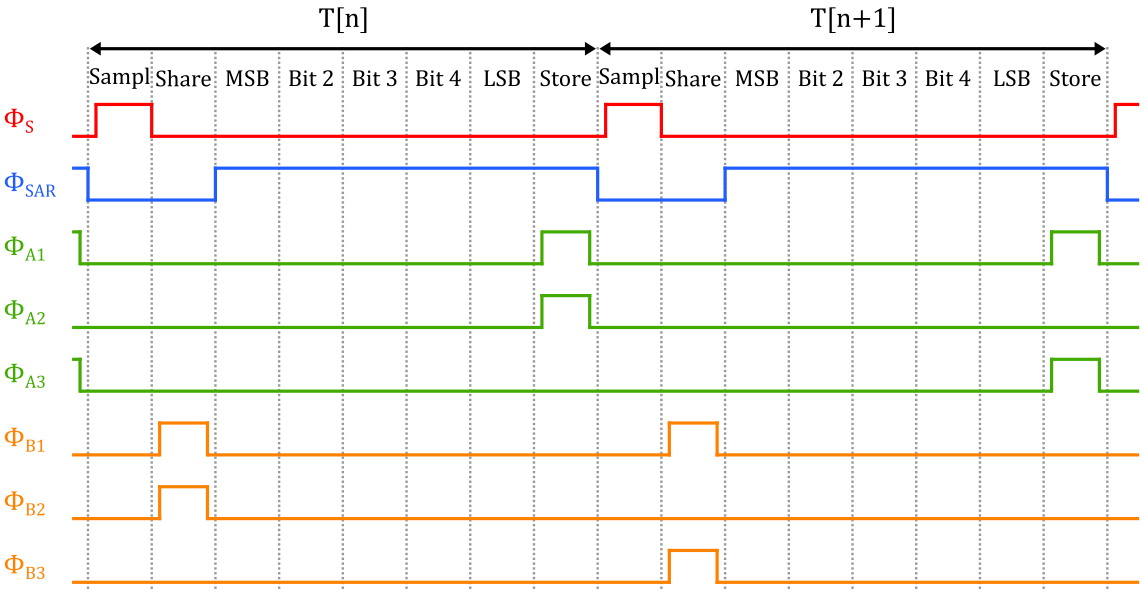


FIGURE 2.13: Complete timing diagram of the proposed converter phases.

The regular periodicity of these signals ensures a stable and predictable contribution to the overall transfer function. In contrast, the phases $\phi_{A2,3}$ and $\phi_{B2,3}$, which drive the charging and charge-sharing of capacitors C_{r2} and C_{r3}, are activated in an alternating manner. This ping-pong mechanism ensures that while one of the capacitors is being charged with the most recent residue, the other retains the previously sampled value for one additional cycle. The alternation between C_{r2} and C_{r3} is what enables the effective implementation of the two-cycle delay required for the z^{-2} term of the loop filter transfer function. Without this alternation, it would not be possible to realize the second-order differentiator using such a compact circuit structure;

2. The control signal ϕ_{SAR} is shown as a simplified global phase that conceptually represents the ensemble of all the DAC driving phases. Rather than detailing each bit-level switching event of the capacitor array, ϕ_{SAR} is introduced to emphasize the time interval during which the successive approximation process takes place. In other words, this phase highlights the conversion window, i.e., the period in which the SAR logic executes the binary search algorithm and successively updates the DAC configuration based on the comparator output. This abstraction simplifies the timing representation while still conveying the essential operation of the converter. It should be noted that, in practice, ϕ_{SAR} actually corresponds to a sequence of non-overlapping control signals, each one driving the capacitor array for a single bit decision. The use of a single symbolic phase in the diagram allows the reader to focus on the interplay between the SAR conversion process and the loop filter dynamics without being distracted by low-level switching details;

3. The loop filter amplifier, from now on called Residue Amplifier (RA), is enabled only when ϕ_{A1} is asserted. Since this condition occurs for only $1/8$ of the entire conversion period, the amplifier remains active for a very limited fraction of time. During the remaining portion of the cycle, the amplifier input is disconnected from the V_{top} node and the block can be safely turned off. This duty-cycled operation significantly reduces the average power consumption, as the amplifier is utilized only when strictly necessary. The result is an overall improvement in energy efficiency without compromising the accuracy or timing of the residue amplification. This design choice demonstrates how careful timing of the control signals can lead not only to performance recovery but also to meaningful energy savings in practical implementations.

The timing diagram therefore summarizes in a compact yet insightful manner the cooperation between the SAR conversion process, the loop filter operation, and the duty-cycled amplifier. Each phase is carefully scheduled in order to avoid overlap between incompatible operations, such as simultaneous charge storage and sharing, while guaranteeing that every capacitor involved in the loop filter is either storing or transferring charge at the appropriate moment.

In summary, the proposed phase arrangement provides a compact yet effective method to realize the desired noise-shaping functionality while simultaneously minimizing power consumption. The careful scheduling of the control signals allows both the correct implementation of the delay elements required by the transfer function and the exploitation of duty-cycling techniques to reduce the active time of the amplifier. This design strategy underlines the quasi-passive nature of the architecture, in which most of the signal processing is performed by passive charge-sharing, and active circuitry is employed only intermittently for signal restoration. The detailed circuit implementation will be presented in the following page (see Fig. 2.14).

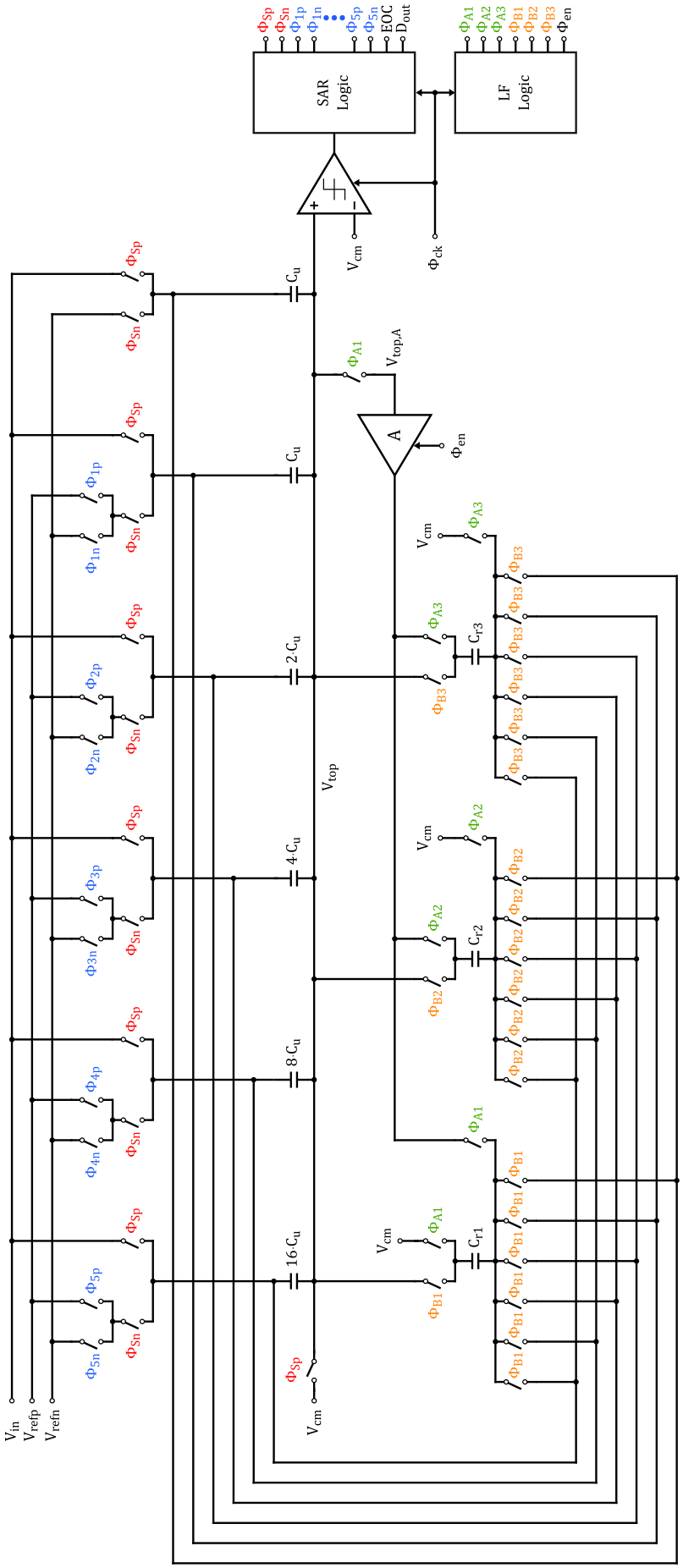


FIGURE 2.14: Detailed schematic of the proposed quasi-passive noise-shaping SAR converter.

2.3 Transistor Level Design

In this Section, the complete transistor-level description of all the circuital blocks that constitute the proposed converter is presented. Each block plays a fundamental role in guaranteeing the correct functionality, performance, and robustness of the overall architecture. A thorough understanding of their design choices is therefore crucial to fully appreciate the trade-offs that have been made. The blocks that compose this ADC can be summarized as follows:

1. **Capacitive DAC and Charge-Sharing Loop Filter:** the first one is responsible for sampling the input signal and algebraically combining it with a variable threshold that is updated at each conversion cycle, while the second one implements the desired NTF by storing and transferring the residue voltage across consecutive conversion cycles;

2. **Residue Amplifier:** amplifies the residue voltage in order to compensate for the losses inherently introduced by the charge-sharing process;

3. **Comparator:** performs the decision-making step by comparing the sampled input voltage with the variable threshold generated by the CDAC;

4. **SAR and LF Digital Logics:** the first one orchestrates the timing of the conversion process, enabling the binary search algorithm and ensuring the proper functioning of the CDAC, while the second one generates the non-overlapping phases that control all the switches within the loop filter, thereby enabling its correct operation;

5. **Reference Buffers:** provide decoupling, stability, and sufficient driving capability for the three voltage references required by the CDAC;

6. **Input Buffer:** provides decoupling and driving capability for the input signal, preventing loading effects and distortion.

Each of these blocks has been carefully designed at the transistor level to optimize performance under the typical constraints of low power and limited silicon area. In the following subsections, a detailed description of their structure and design considerations is provided.

2.3.1 Capacitive DAC

The Capacitive DAC (CDAC) constitutes the core element of the successive approximation register architecture, as it is directly responsible for both sampling the analog input and generating the reference thresholds required for conversion. Furthermore, it provides the residue voltage that is subsequently processed by the noise-shaping loop filter. In the proposed design, a 5-bit SAR ADC is considered, relying on a charge redistribution scheme that exploits a binary-weighted capacitor array. As discussed in Sec. 1.2.1, this type of DAC generates a set of output voltages that are directly proportional to the applied digital codes, exploiting the principle of charge conservation. In a 5-bit DAC, a total of $2^5 = 32$ digital codes can be represented, and therefore 32 quantization levels are mapped into equally spaced voltage steps. The overall voltage span is defined by the full-scale voltage (V_{FS}), which, according to the design specifications, has been set to 600 mV in order to maximize the exploitable dynamic range. Figure 2.15 shows the staircase input-output characteristic of such a DAC, highlighting the uniformity of the steps and the correct linear behavior having a 600 mV full-scale ranging from $V_{refn} = 300\,mV$ to $V_{refp} = 900\,mV$.

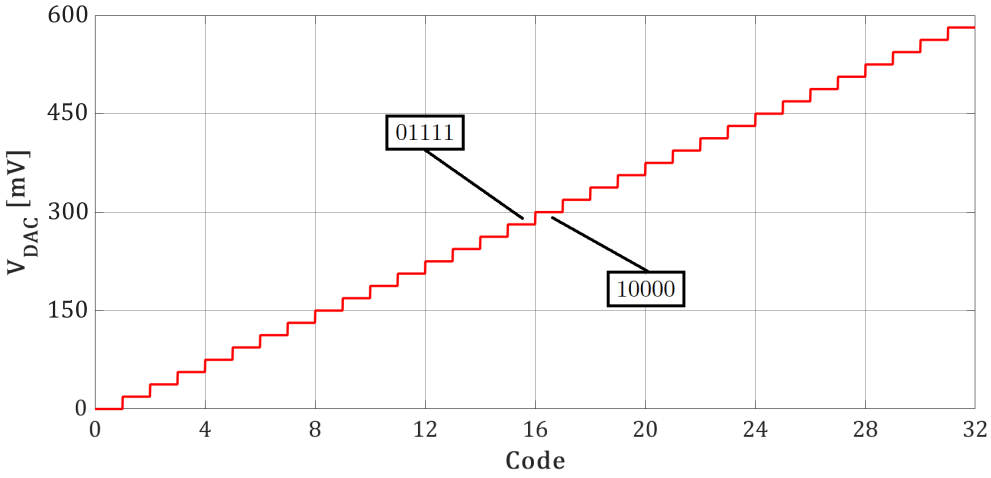


FIGURE 2.15: Transfer characteristic of a 5-bit 600 mV full-scale CDAC.

The dimensioning of the unit capacitance C_u represents the critical starting point for the entire design. As previously explained in Section 2.1.4, robustness against process variation is one of the most desirable features in integrated circuits, especially when accuracy and linearity are primary objectives. In the CDAC, any mismatch in the relative ratios of the capacitors translates directly into conversion errors, degrading the effective number of bits. In addition to mismatch, another limiting factor is the contribution of thermal noise. The mean square and the Root Mean Square (RMS) values of the thermal noise generated in an oversampled switched-capacitor structure can be expressed as:

$$\begin{aligned} \overline{v_n^2} &= \frac{k_B T}{OSR \cdot C_{DAC}} \\ v_n &= \sqrt{\frac{k_B T}{OSR \cdot C_{DAC}}} \end{aligned} \tag{2.15}$$

where $k_B = 1.380649 \times 10^{-23}\ J \cdot K^{-1}$ is the Boltzmann constant, T is the absolute temperature expressed in kelvin $[K]$, OSR is the oversampling ratio, and C_{DAC} is the total DAC capacitance value expressed in farads $[F]$. From these relations it is evident that the thermal noise sets a lower bound for the capacitance, below which the noise contribution dominates and irreparably limits the performance of the converter. In practice, for error-feedback SAR ADCs, a unit capacitance smaller than a few tens of femtofarads is not recommended, as it would compromise both noise and matching requirements. On the other hand, increasing the capacitor size improves matching and noise performance but inevitably leads to a larger silicon area and higher capacitive loading, thus increasing power consumption. The design task therefore consists in identifying the minimum capacitance value that satisfies both noise and matching constraints without unnecessarily penalizing area and power. Given 84 dBA as the target SNR at 0 dBFS for the proposed converter, it is possible to derive the minimum unit capacitance for the DAC starting

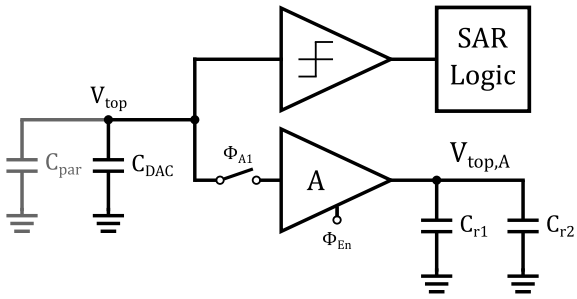


FIGURE 2.16: Simplified schematic of the converter with parasitic capacitance on node V_{top} highlighted.

from the total RMS noise ($V_{n,tot}$) required

$$\begin{aligned} SNR_{target} &= \frac{V_{sig,rms}}{v_{n,tot}} = 84\,dB \\ \Rightarrow \quad v_{n,tot} &= \frac{V_{sig,rms}}{SNR_{target}} = \frac{\frac{V_{FS}}{\sqrt{2}}}{SNR_{target}} = \frac{\frac{600\,mV}{\sqrt{2}}}{10^{84/20}} \approx 26.8\,\mu V, \end{aligned} \tag{2.16}$$

where $V_{sig,rms}$ is the RMS value of the maximum input signal (V_{FS}). Since the total noise is a contribution of several noise sources, it is better to oversize C_{DAC} to have some future margin over the other noise contributions. In this case, a 6 dB margin is enough. Defining $SNR_{target,DAC} = 90\,\text{dB}$ the new target for the SNR where only the DAC contributes for the noise, it is possible to derive maximum DAC noise contribution $V_{n,DAC}$ as:

$$\begin{aligned} SNR_{target,DAC} &= \frac{V_{sig,rms}}{v_{n,DAC}} = 90\,dB \\ \Rightarrow \quad v_{n,DAC} &= \frac{V_{sig,rms}}{SNR_{target,DAC}} = \frac{\frac{600\,mV}{\sqrt{2}}}{10^{90/20}} \approx 13.4\,\mu V. \end{aligned} \tag{2.17}$$

Substituting (2.17) in (2.15) the total minimum capacitance is obtained:

$$\begin{cases} v_{n,DAC} = \sqrt{\frac{k_B T}{OSR \cdot C_{DAC}}} \\ v_{n,DAC} = 13.4\,\mu V \end{cases} \quad \Rightarrow \quad C_{DAC} = \frac{k_B T}{OSR \cdot v_{n,DAC}^2} \approx 800\,fF. \tag{2.18}$$

Therefore the minimum unit capacitance is given by:

$$C_u = \frac{C_{DAC}}{2^n} = \frac{800\,fF}{2^5} = 25\,fF. \tag{2.19}$$

Another critical aspect to be taken into account is the parasitic capacitance at the V_{top} node. This node is directly connected to the input of the residue amplifier, which is a high-impedance node and therefore particularly sensitive to capacitive loading, as it can be seen in Fig. 2.16. In Fig. 2.17 it can be seen that even relatively small parasitic values can introduce significant attenuation of the residue and consequently degrade the resolution of the converter, here expressed in Signal-to-Quantization-Noise (SQNR) since noise contribution are neglected. Taking into account the parasitic capacitance C_p, the residue voltage can be rewritten as:

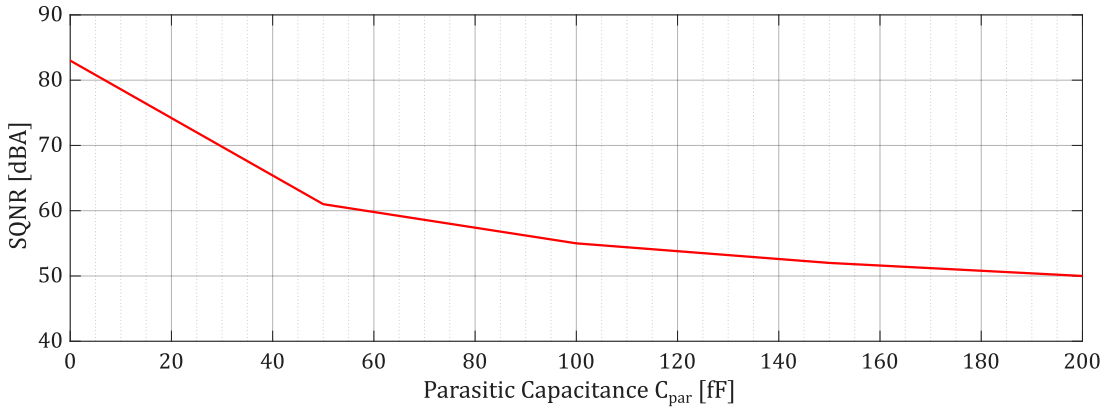


FIGURE 2.17: Converter SQNR degradation as a function of the parasitic capacitance on node V_{top}.

$$V_{res}[n] = A \cdot \frac{\alpha}{1 + 3\alpha + \frac{C_p}{C_{DAC}}} \cdot \left(2 \cdot V_{res}[n-1] \; - \; V_{res}[n-2]\right), \tag{2.20}$$

From this equation, it can be deduced that the presence of parasitic capacitance (highlighted in red) increases the attenuation factor, thereby worsening the transfer of the residue voltage. In other words, the additional capacitance effectively reduces the signal swing that is propagated to the next stage, thus degrading both the resolution and the noise-shaping behavior of the overall converter. To counteract this degradation, the gain A of the residue amplifier must be increased by a corresponding amount, thereby compensating for the undesired attenuation and ensuring that the effective residue propagation is preserved. This compensation strategy, however, introduces a serious drawback: the exact value of the parasitic capacitance is generally not known with sufficient accuracy prior to fabrication. Since post-layout parasitics strongly depend on layout geometry, routing, and proximity to other structures, their precise magnitude is difficult to predict during the design phase. As a result, designing an amplifier with a fixed gain that precisely cancels this effect is not advisable, because any mismatch between the actual and the estimated parasitic value would directly translate into a gain error and consequently into a performance penalty. In advanced technology nodes, this uncertainty is exacerbated by the variability of the process itself, making a purely compensation-based solution less reliable. An alternative and more robust approach consists in minimizing the parasitic contribution at its source by careful capacitor design. In particular, it is possible to adopt custom shielded capacitors that intrinsically present negligible parasitic coupling. As illustrated in Fig. 2.18a, 2.18b, and 2.18c, these devices are based on a layout in which a central plate, denoted as *Top*, is completely surrounded on all sides by a *Bottom* plate. The latter acts as an electrostatic shield, effectively isolating the sensitive node V_{top} from external influences such as substrate coupling or adjacent routing lines. In this way, the dominant parasitic paths are diverted to the shield, leaving the *Top* node capacitively well-defined and stable. Electromagnetic model extraction and post-layout simulations confirm the effectiveness of this approach, showing that the parasitic contributions from the *Top* node to the substrate are virtually negligible. At the same time, the *Top-Bottom* unity capacitance remains well controlled and is set to the minimum allowed value of C_u obtained from (2.19), approximately 25 fF. Moreover this value has been identified as the minimum capacitance at which capacitor mismatch becomes negligible, according to Monte Carlo sampling simulations reported in Fig. 3.5 where the DAC output voltage

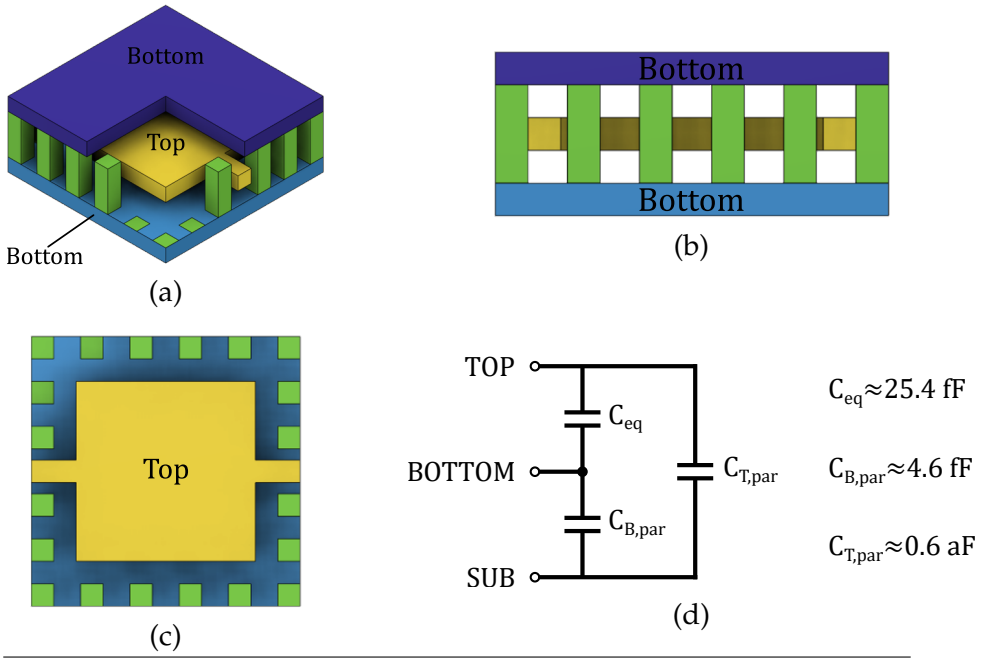


FIGURE 2.18: Custom shielded capacitor (a) 3D view, (b) cross section, (c) top view, and (d) equivalent extracted model.

spread for the two middle codes, that in a 5-bit SAR are 15 (01111) and 16 (10000), is shown. Therefore, the adoption of custom shielded capacitors not only suppresses the detrimental effect of parasitics but also ensures high matching accuracy and stable operation across process variations. This solution represents a balanced trade-off between robustness, area efficiency, and design simplicity, thereby enabling the CDAC to achieve the required resolution without relying on uncertain gain compensation in the residue amplifier.

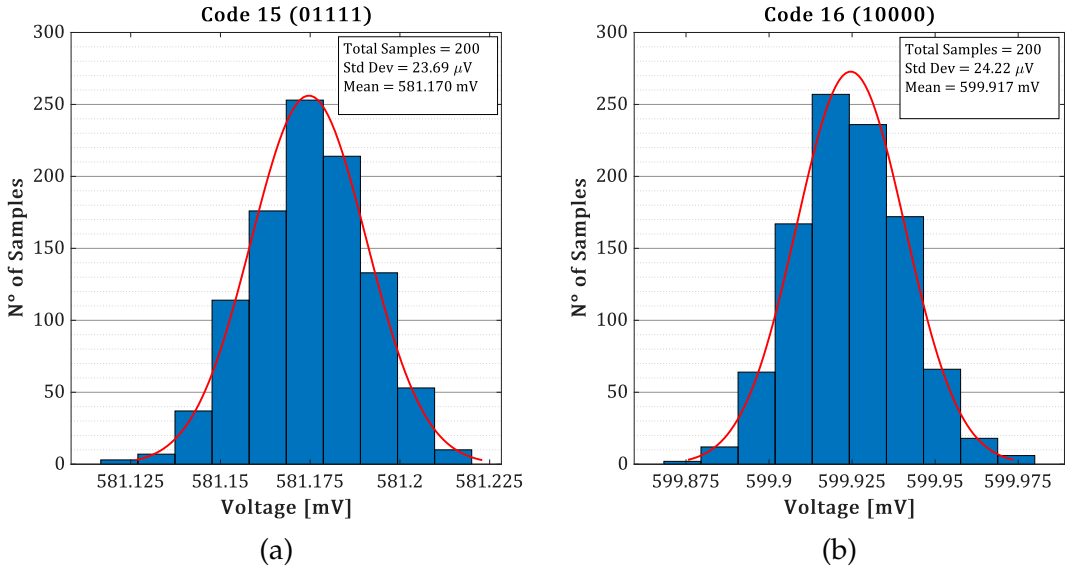


FIGURE 2.19: DAC output voltage spread for (a) 01111 and (b) 10000 code configurations.

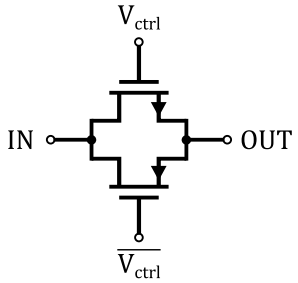


FIGURE 2.20: Scheme of a transmission gate CMOS switch.

In a switched-capacitor circuit, once the capacitance values are properly defined, the correct sizing of the switching devices becomes the second critical design aspect. A switch is an electronic component whose role is to either establish or break the connection between two electrical nodes. In an ideal case, when the switch is in the ON state, it would allow the flow of arbitrarily large currents without introducing any voltage drop across its terminals. Conversely, in the OFF state, it would exhibit an infinite resistance, thereby completely blocking any current flow. Clearly, such ideal behavior cannot be achieved in practice. Real switches inevitably exhibit non-idealities, which must be carefully accounted for in the design process of precision circuits. In integrated circuits, a switch is typically realized by either a single MOS transistor or, more commonly, by a complementary pair of transistors, forming what is referred to as a CMOS transmission gate. These devices control the conduction path depending on an external control signal. Figure 2.20 illustrates the schematic representation of a CMOS switch. The ON and OFF states are enforced by applying appropriate voltages to the gates of the two MOSFETs. For an n-channel device, a sufficiently positive control voltage V_{ctrl}, such that $V_{gs} > V_{th}$, drives the transistor into the conduction (triode) region, enabling current flow. In contrast, for a p-channel device, the control signal must be complementary ($\overline{V_{ctrl}}$), ensuring $V_{gs} < V_{th}$. As a result, a CMOS switch is usually driven by two complementary control signals, as depicted in Fig. 2.20. When a practical switch operates in the ON state, both transistors enter the triode region, and the conduction is limited by the finite on-resistance of the devices. This resistance is not negligible and directly impacts the switching speed and the settling accuracy of the switched-capacitor network. The on-resistance of a MOS transistor in the linear region can be expressed as [43]:

$$R_{on} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})}, \tag{2.21}$$

where μ is the carrier mobility, C_{ox} the oxide capacitance per unit area, and W/L the aspect ratio of the device. Clearly, the sizing of the transistors plays a decisive role in determining the effective resistance of the switch. In the case of a SAR ADC, the switches controlling the capacitive DAC must be dimensioned so as to guarantee that its capacitors are fully charged or discharged within the allocated time window. At the same time, oversizing the devices is not advisable, since it increases parasitic capacitances and exacerbates charge-injection effects, which arise when the channel charge of the MOS transistor is redistributed to the surrounding nodes at the switching instant. This phenomenon introduces voltage errors on the capacitors, directly degrading the conversion accuracy. Therefore, the design requires a careful trade-off between low on-resistance for fast charging and minimal charge injection.

In synchronous SAR architectures, the capacitors must settle before the comparator

decision, which occurs during the falling edge of the clock signal. Considering an oversampling ratio of 32 and a signal bandwidth of 8 kHz, the sampling period of the converter can be derived from (2.1) as:

$$T_s = \frac{1}{OSR \cdot (2 \cdot BW)} = \frac{1}{32 \cdot 16\,kHz} \approx 1.95\,\mu s. \tag{2.22}$$

As explained in Sec. 2.2.2, one complete conversion requires eight clock periods, leading to:

$$T_{ck} = \frac{T_s}{8} \approx 244\,ns \qquad \text{or} \qquad F_{ck} = 8 \cdot F_s = 4.096\,MHz. \tag{2.23}$$

In general, the charging and discharging transients must settle within less than $T_{ck}/2$. Using the minimum device dimensions allowed by the technology ($W = 120\,nm$ and $L = 60\,nm$), the resulting on-resistance is approximately $10\,k\Omega$. The characteristic time constant for charging a capacitor is given by $\tau = R_{on}C$, and full settling is typically assumed after approximately 5τ. For the largest capacitor in the DAC array, i.e., the MSB capacitor (16 times the unit capacitance), the time constant is:

$$\tau = R_{on} \cdot C_{MSB} = 10\,k\Omega \cdot 16 \cdot 25\,fF \approx 4\,ns \qquad \Rightarrow \qquad 5 \cdot \tau \approx 20\,ns, \tag{2.24}$$

which is significantly smaller than $T_{ck}/2$, ensuring reliable settling. As can be inferred from these equations, the minimum-size switches employed in this design not only provide sufficient charging and discharging speed, but also inherently minimize charge-injection effects thanks to their reduced channel area, thereby improving overall conversion accuracy.

2.3.2 Residue Amplifier

The residue amplifier plays a fundamental role in the overall operation of the converter, as it restores the residue signal that would otherwise be corrupted by charge-sharing

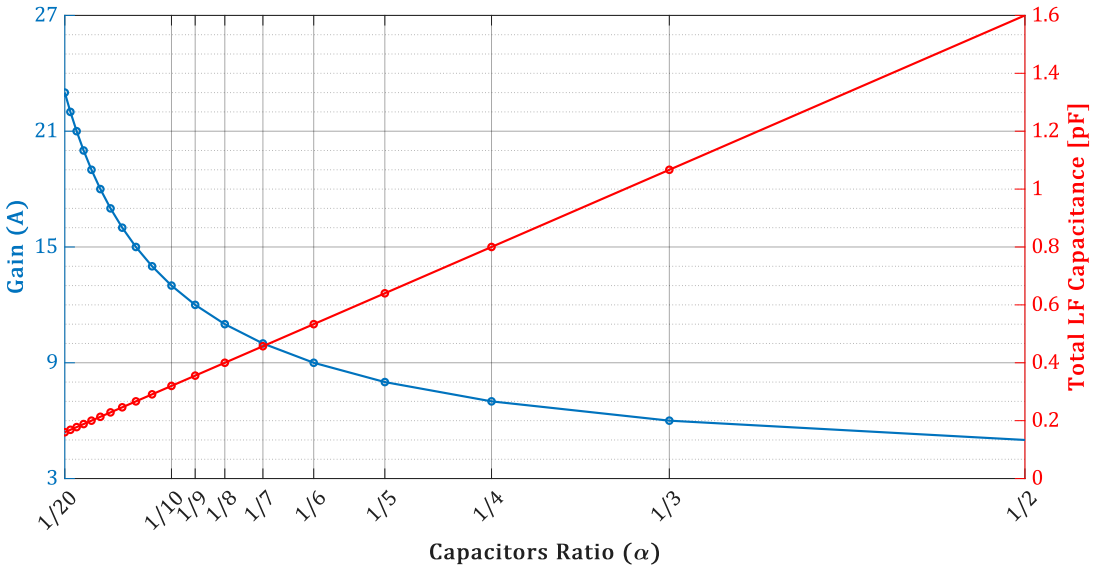


FIGURE 2.21: Dependence of loop filter amplifier gain (A) and total capacitance on the capacitor ratio α.

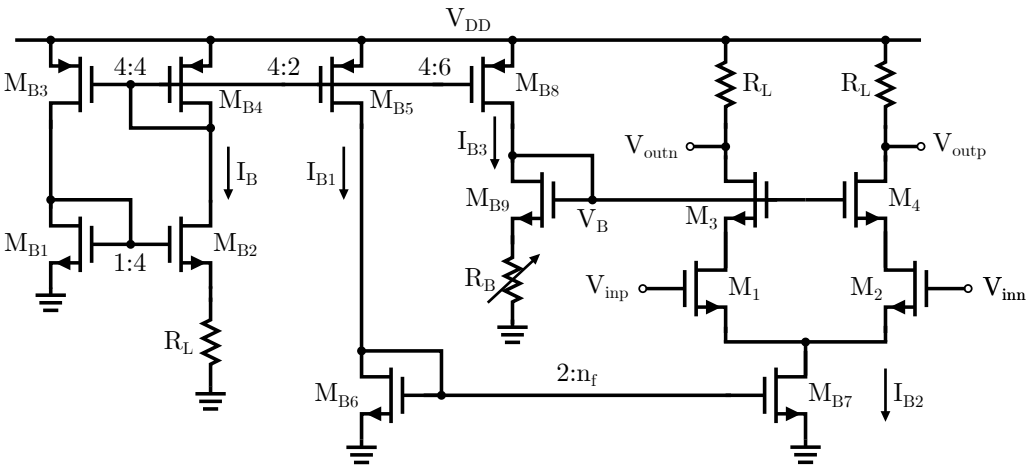


FIGURE 2.22: Residue amplifier schematic.

losses within the capacitive network. Without such amplification, the accuracy and linearity of the conversion process would be severely compromised. Before analyzing the details of the circuit implementation, it is necessary to discuss the coefficient α, introduced in Sec. 2.3.1, which is defined as the ratio between C_{LF} and C_{DAC}. This coefficient directly determines the required amplification for the residue amplifier and thus represents a key parameter in the design. The choice of α is a non-trivial design decision, as it establishes a balance between the gain of the residue amplifier and the total capacitance of the loop filter. Since the loop filter capacitance directly impacts both the occupied silicon area and the amplifier power consumption, the value of α strongly affects the overall efficiency of the system. Formally, the coefficient is given by

$$\alpha = \frac{C_{LF}}{C_{DAC}}, \tag{2.25}$$

and the total loop filter capacitance can be expressed as

$$C_{LF,tot} = C_{r1} + C_{r2} + C_{r3} = 2C_{LF} + C_{LF} + C_{LF} = 4C_{LF} = 4\alpha C_{DAC}. \tag{2.26}$$

It is therefore evident that there is a direct proportionality between α and $C_{LF,tot}$. Increasing α entails two major drawbacks. First, larger capacitance values lead to greater silicon area occupation, which is undesirable in this design due to integration constraints. Second, since the loop filter capacitance constitutes the load of the amplifier, increasing it inevitably raises the power consumption of the residue amplifier, thereby reducing the overall energy efficiency. On the other hand, the amplifier gain, defined in Eq. (2.13), is inversely proportional to α. In practical terms, reducing the required amplification implies an increase in the capacitor ratio. This introduces a clear trade-off: a higher α reduces the required gain but increases capacitance (and thus area and power), whereas a lower α minimizes capacitance but demands higher amplification. This relationship is illustrated in Fig. 2.21. To mitigate this trade-off, in this work a value of $\alpha = 1/8$ was chosen, which leads to:

$$C_{LF,tot} = \frac{C_{DAC}}{2} \qquad \text{and} \qquad A = 11. \tag{2.27}$$

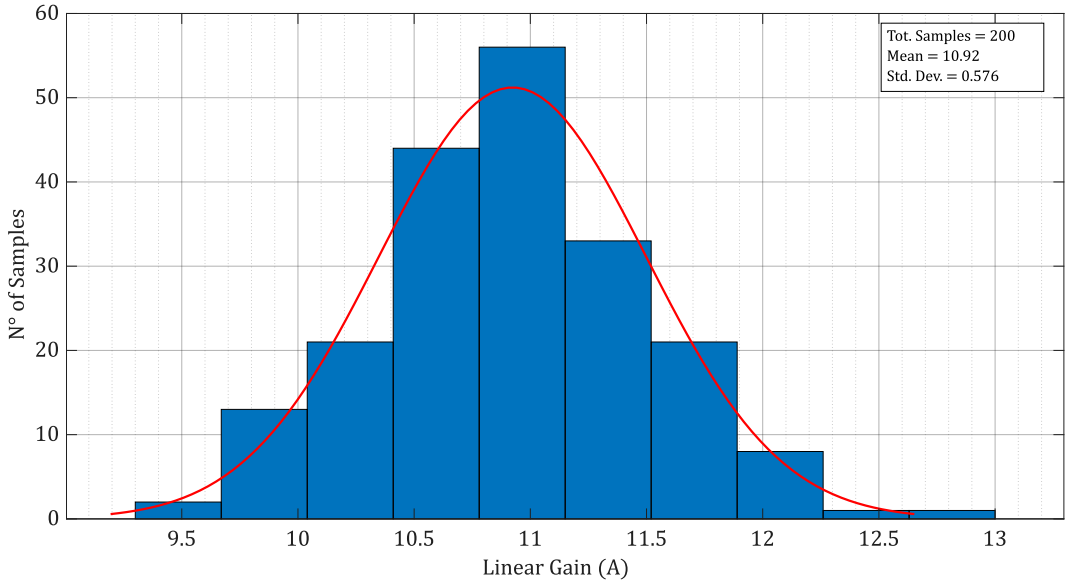


FIGURE 2.23: Simulated residue amplifier gain in mismatch conditions.

This design choice ensures that the total capacitance of the loop filter remains smaller than the DAC capacitance itself while keeping the required amplifier gain relatively modest. In this way, both silicon area occupation and power consumption are constrained, while the accuracy of residue amplification is preserved.

Given the stringent power constraints of AAD applications, an open-loop differential architecture was adopted for the residue amplifier. The implemented topology, shown in Fig. 2.22, is based on a $g_m \cdot R$ configuration with a cascoded input stage. The cascoding helps to stabilize the static gain across the entire input range, ensuring consistent performance even in the presence of process variations. A dedicated biasing network generates a compensation current that mitigates first-order dependencies on supply voltage and temperature, thereby maintaining a constant overall gain. The compensation principle exploits the operation of transistors M_{B1} and M_{B2} in the subthreshold region. Under this biasing condition, a current inversely proportional to R_L is generated, resulting in the following relationships:

$$\begin{cases} I_B = \dfrac{nV_T \ln(k)}{R_L} \\ g_{m1,2} \propto \dfrac{I_B}{nV_T} = \dfrac{\ln(k)}{R_L} \\ A = g_{m1,2} \cdot R_L = \text{constant} \end{cases} \tag{2.28}$$

where n denotes the inversion coefficient, V_T is the thermal voltage, and k represents the scaling factor between M_{B2} and M_{B1}. This formulation shows that the gain becomes effectively independent of R_L, providing intrinsic robustness against temperature variations.

To further counteract process-induced mismatches, a trimming mechanism was integrated into the design. The first level of trimming acts on the tail current source of the differential pair (M_{B7}). By modifying the number of transistor fingers (n_f), the bias current in the output branches can be finely tuned. Additionally, a second trimming stage is implemented by adjusting the number of resistor segments in R_B, which modifies the

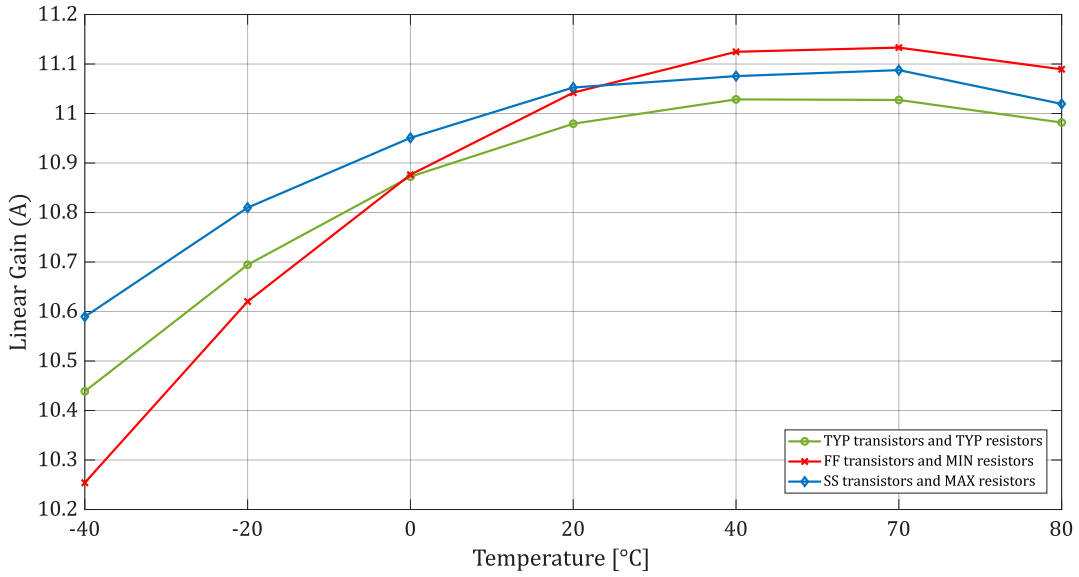


FIGURE 2.24: Simulated residue amplifier gain as a function of temperature and process.

bias voltage V_B of the cascode devices. This two-step trimming strategy enables compensation of fabrication variations while preserving amplifier stability and gain accuracy. The effectiveness of the proposed design was verified through simulations, which demonstrated a robust behavior across process, voltage, and temperature (PVT) variations. In Fig. 2.23 the spread of the linear gain in mismatch conditions is shown. The 200 points Monte Carlo sampling simulation illustrates how the gain, thanks to the circuital solutions described above, remains close to the typical value allowing the correct restore of the residue and avoiding degradation in the final converter resolution. Furthermore, in Fig. 2.24, is it possible to observe that, thanks to the two-steps trimming, the gain remains also stable across the whole commercial temperature range ($-40\,°C$ to $80\,°C$) independently from process variations.

The amplifier specifications as well as the transistor dimensions employed in the final implementation are summarized in Tables 2.2 and 2.3, respectively. It is worth noting that was done a layout oriented design in order to minimize devices mismatch and area occupation. For transistor M_{B7} as well as for resistor R_B the table reports the minimum and maximum values they can assume depending on the trimming applied.

Specification	Gain	BW @ -3 dB	G_m	R_L	R_B	IRN	V_B	I_B	I_{tot}
Value	11	5.9 MHz	275 µS	44 kΩ	8÷16	30 µV	900 µV	1 µA	25 µA

TABLE 2.2: Specifications of the residue amplifier transistors.

Transistor	M_{B1}	M_{B2}	M_{B3}	M_{B4}	M_{B5}	M_{B6}	M_{B7}	M_{B8}	M_{B9}	M_1	M_2	M_3	M_4
Width [µm]	4	16	0.6	0.6	0.3	1	36÷44	0.9	1	80	80	40	40
Length [µm]	1	1	10	10	10	2	1	20	20	0.4	0.4	2	2

TABLE 2.3: Sizing of the residue amplifier transistors.

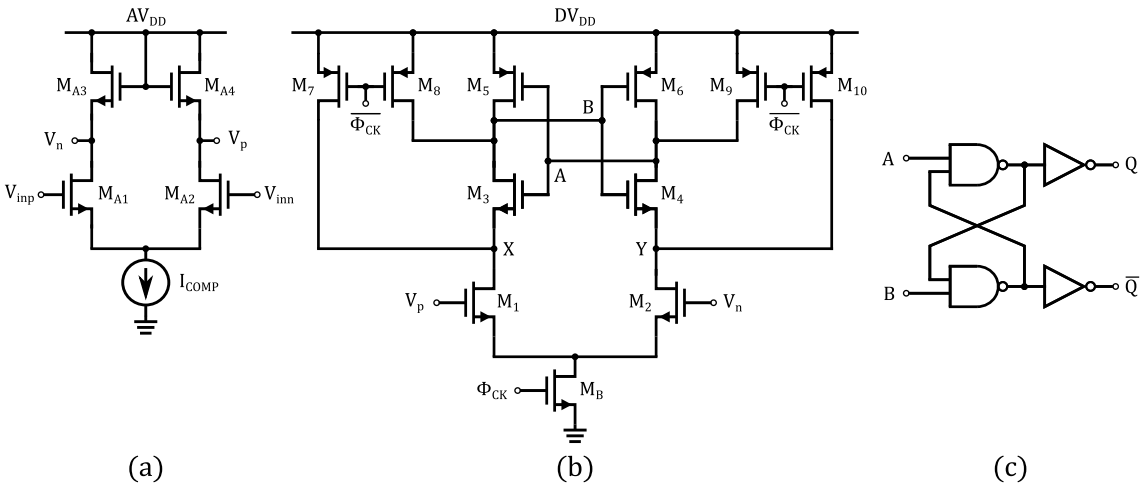


FIGURE 2.25: Schematic of (a) the preamplifier, (b) the strong ARM core and (c) the set-reset latch.

2.3.3 StrongARM Comparator

The implemented comparator follows a synchronous StrongARM architecture with an additional preamplifier stage. StrongARM comparators, also known as dynamic latched comparators, represent one of the most widely adopted topologies in high-speed and low-power analog-to-digital conversion systems. Their popularity arises from the absence of static current paths during steady-state operation, which leads to a negligible static power consumption, and from their ability to provide rail-to-rail logic-level outputs directly from small differential input signals. These properties make the StrongARM topology particularly well-suited for applications such as successive approximation register ADCs, flash ADCs, and other mixed-signal front-end circuits, where both speed and power efficiency are critical. The operation of a StrongARM comparator can be divided into two main phases, controlled by a clock signal: a *reset* (or *precharge*) phase and an *evaluation* phase. During the reset phase, internal nodes are precharged to well-defined voltages, ensuring that the comparator starts each evaluation from a symmetric metastable condition. During the subsequent evaluation phase, the differential input drives a current imbalance in the input differential pair. This imbalance is then amplified by the regenerative latch, which relies on strong positive feedback to resolve the metastability and quickly drive the outputs to valid logic levels. The speed of this decision process depends on the input differential voltage, the device sizing, and the regenerative gain of the latch. In practice, however, a major limitation of the conventional StrongARM comparator is its relatively large input-referred offset, which results from device mismatches in the input transistors and from parasitic asymmetries in the regenerative latch. To mitigate this effect and to improve the sensitivity for small input signals, it is common to introduce a *preamplifier* stage in front of the StrongARM core. The preamplifier serves two purposes: first, it reduces the input-referred offset by attenuating device mismatch through voltage amplification; second, it isolates the comparator input from kickback noise generated during the latch regeneration. Although the preamplifier contributes additional power consumption and latency, its inclusion significantly enhances the robustness of the decision-making process, especially in high-resolution applications. The overall scheme of the implemented comparator is reported in Fig. 2.25. The front-end preamplifier (Fig. 2.25a) provides a differential gain to the input signal and reduces sensitivity to kickback, while the subsequent StrongARM latch (Fig. 2.25b) performs the main

Transistor	M_{A1}	M_{A2}	M_{A3}	M_{A4}
Width [µm]	2	2	0.3	0.3
Lenght [µm]	1	1	12	12

TABLE 2.4: Sizing of the comparator preamplifier transistors.

regenerative decision. To minimize possible mismatches and reduce system as well as layout complexity, a g_m over g_m scheme is implemented for the preamplifier. In this topology, the effective small-signal gain is given by

$$A_v = -\frac{g_{m,in}}{g_{m,load}} = -\frac{g_{mA1,A2}}{g_{mA3,A4}}, \tag{2.29}$$

where $g_{m,in} = g_{mA1,A2}$ is the transconductance of the input pair (transistors M_{A1} and M_{A2}) and $g_{m,load} = g_{mA3,A4}$ corresponds to the diode-connected load (transistors M_{A3} and M_{A4}). Such a ratio-based expression makes the gain largely independent of process or bias current variations, relying instead on transistor sizing. Furthermore, the use of diode-connected devices ensures a well-defined load impedance $R_{out} \approx 1/g_{m,load}$, which stabilizes the operation of the preamplifier while maintaining compact design. One possible drawback is that the area of the input MOSFETs increase with the square of gain. Given

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}, \tag{2.30}$$

equation (2.29) can be rewritten as:

$$A_v = -\sqrt{\frac{\frac{W_{in}}{L_{in}}}{\frac{W_{load}}{L_{load}}}} \quad \Rightarrow \quad \frac{W_{in}}{L_{in}} = A_v^2 \cdot \frac{W_{load}}{L_{load}}. \tag{2.31}$$

From this equation it is possible to observe the quadratic dependence of the input from the voltage gain. However, for this application, $A_v = 9$ is sufficient to speed up the decision time of the strongARM latch while reducing kickback noise and keeping low its power consumption (1 µA drawn from I_{COMP}). In Tab. 2.4 are reported all the MOS dimensions of the preamplifier. The latch core consists of two cross-coupled transistor pairs, namely M_3–M_4 and M_5–M_6, which are responsible for exploiting positive feedback to drive the outputs to rail-to-rail levels as quickly as possible. Owing to this strong positive feedback, once the regenerative phase begins, the latch rapidly resolves the metastable state and ensures a robust digital output. The clock signal ϕ_{CK} governs the two operating phases of the comparator. During the precharge phase (ϕ_{CK} high), transistors M_7, M_8, M_9, and M_{10} reset the circuit: nodes A and B are precharged to V_{DD} through M_8 and M_9, while transistors M_9 and M_{10} precharge nodes X and Y to the supply voltage. This ensures that the latch starts from a well-defined and symmetric initial condition. When ϕ_{CK} transitions low, the reset transistors turn off and the evaluation phase begins. The input differential pair M_1–M_2 generates a current imbalance according to the applied input voltage. This imbalance perturbs the potentials at nodes X and Y, which in turn

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}
Width [µm]	16	16	8	8	8	8	4	4	4	4
Lenght [nm]	60	60	60	60	60	60	60	60	60	60

TABLE 2.5: Sizing of the comparator strongARM latch transistors.

Specification	A_v	Delay	P_{stat}	P_{dyn}
Value	9	3.5 ns	1.2 µW	0.9 µW

TABLE 2.6: Simulated performance of the strongARM comparator.

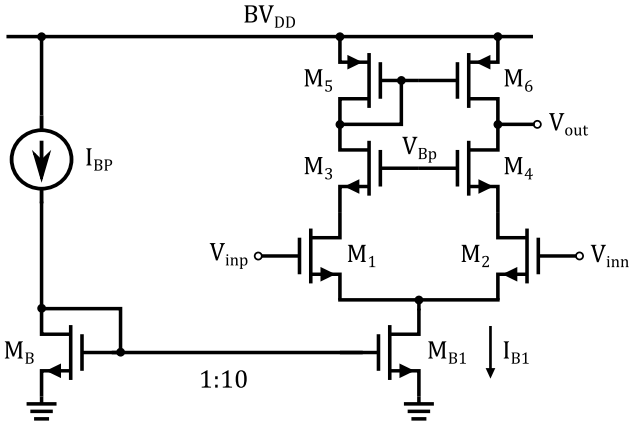
destabilize the cross-coupled structure and trigger the regeneration process. The latch then forces node A towards either V_{DD} or ground, while node B transitions to the complementary value. The final decision is stored and stabilized by a Set-Reset (SR) latch implemented with two NAND gates and two inverters (Fig. 2.25c). This stage ensures that the outputs Q and $\overline{Q}$ are always valid and complementary, avoiding the forbidden state that could otherwise occur during the reset phase, when both nodes A and B are forced to logic '1'. In addition, this stage provides a clean digital interface compatible with subsequent logic processing stages. Table 2.5 summarizes the transistor sizing employed in the strongARM design while in Tab. 2.6 are reported its simulated performance.

2.3.4 Digital Logics

The correct operation of the proposed noise-shaping SAR ADC is guaranteed by two distinct but strictly coordinated digital control units: the *SAR Logic* and the *Loop Filter Logic*. Both blocks were custom-designed in order to ensure precise timing relationships, low complexity, and seamless integration with the mixed-signal nature of the architecture.

The SAR logic implements a 5-bit successive approximation routine, generating the control signals that drive the binary-weighted capacitive DAC. This logic is implemented in Verilog to be easily sinthesized, placed and routed with digital layout tool. The full code is visible in Appendix A. For each bit decision, four complementary signals are produced, namely $MxPOS$, $MxPOS\_n$, $MxNEG$, and $MxNEG\_n$, where $x \in [1,5]$ denotes the bit index ($x = 5$ is the MSB, $x = 1$ the LSB). These signals control the switching network of the DAC array, selecting whether each capacitor is connected to the positive or negative reference during the binary search. The conversion cycle is orchestrated by a finite-state machine driven by the clock. The sequence begins with a sampling phase, followed by residue transfer, and then proceeds through a series of bit trials from MSB to LSB. At each trial, the DAC is reconfigured to test the current bit, and the comparator output is sampled to confirm or reject the tentative decision. The result of each decision is stored in internal registers (B_5, B_4, B_3, B_2, B_1), which ultimately form the digital output word at the end of the cycle. An *EOC* (End-of-Conversion) flag is also generated to signal the availability of valid data. In addition to orchestrating the SAR procedure, the same logic provides duty-cycle control for the residue amplifier. Two external bits (*DUTYSEL0*, *DUTYSEL1*) allow selecting among four different duty-cycle modes: amplifier permanently disabled (only for testing purposes), enabled for $3/8$ of the conversion cycle, enabled for $4/8$ of the cycle, or permanently active. The corresponding complementary signals *AMP_EN* and *AMP_DIS* are derived from the internal timing of the SAR sequence and ensure glitch-free switching of the amplifier. This flexibility enables a trade-off between power consumption and linearity, depending on the operating conditions.

The LF logic is responsible for the generation of the non-overlapping control phases that drive the switched-capacitor loop filter. Two 8-step counters, clocked with phase-shifted versions of the system clock, are employed to generate the required signals. This dual-counter scheme introduces a carefully controlled disoverlap between the phases, thereby preventing short-circuit conditions due to simultaneous switch conduction. The resulting control signals are $\phi_{A1}, \phi_{A2}, \phi_{A3}, \phi_{B1}, \phi_{B2}$, and ϕ_{B3}, which govern the storing and charge-sharing operations of the three filter capacitors. The design ensures that ϕ_{A1} and

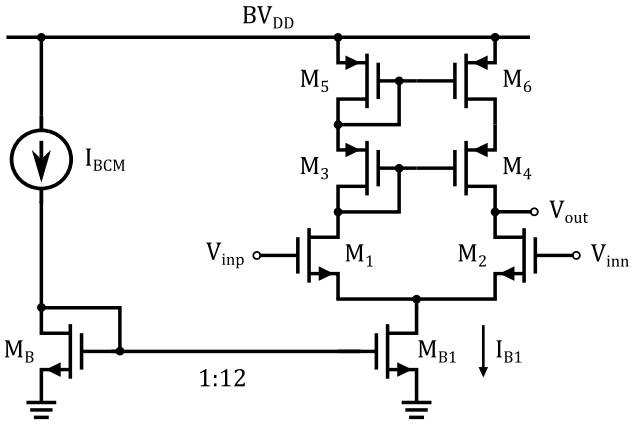


Specification	Value
Loop Gain	39 dB
BW @ 0 dB	3 MHz
G_m	71 µS
R_{out}	1.3 MΩ
Total In-Band Noise	70 µV
V_{Bp}	900 mV
I_{BP}	1 µA
I_{tot}	10 µA

FIGURE 2.26 & TABLE 2.7: Schematic and specifications of the positive reference buffer.

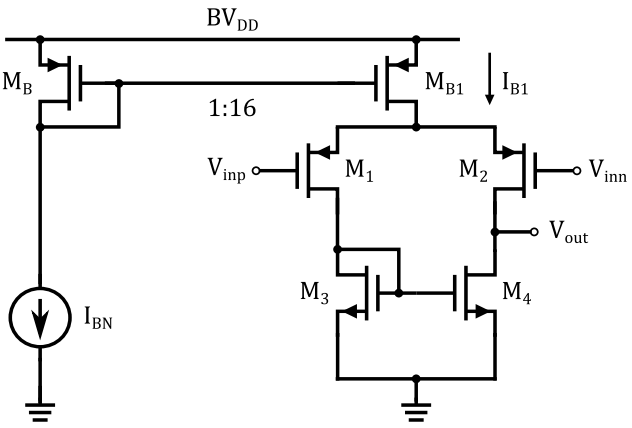
ϕ_{B1} are asserted at every conversion cycle, whereas $\phi_{A2,3}$ and $\phi_{B2,3}$ operate in an alternating manner, implementing the required two-cycle memory for the z^{-2} term of the loop filter. The explicit use of two independent counters provides precise timing resolution, while avoiding overlap between consecutive switching events.

The cooperation between the SAR and LF logics ensures both correct binary search operation and the realization of the noise-shaping loop filter. The SAR logic guarantees that the DAC array is properly updated at each bit decision, while the LF logic schedules the charge transfer between filter capacitors without cross-conduction. Furthermore, the integration of duty-cycled amplifier control into the SAR timing highlights the energy-efficient nature of the architecture: the active blocks are used only when strictly required, and otherwise remain disabled, thereby minimizing static power dissipation. Overall, these digital control units provide the necessary synchronization between the analog and digital domains, enabling robust noise-shaping behavior with reduced implementation cost.



Specification	Value
Loop Gain	41 dB
BW @ 0 dB	3.2 MHz
G_m	133 µS
R_{out}	830 kΩ
Total In-Band Noise	40 µV
I_{BCM}	1 µA
I_{tot}	12 µA

FIGURE 2.27 & TABLE 2.8: Schematic and specifications of the common-mode reference buffer.



Specification	Value
Loop Gain	39 dB
BW @ 0 dB	4.5 MHz
G_m	105 µS
R_{out}	880 kΩ
Total In-Band Noise	44 µV
I_{BN}	1 µA
I_{tot}	16 µA

FIGURE 2.28 & TABLE 2.9: Schematic and specifications of the negative reference buffer.

2.3.5 Auxiliary Buffers

To effectively deliver the externally supplied reference voltages as well as the input audio signal to the internal circuits, three dedicated single-stage MOS operational amplifiers configured as unity-gain buffers are employed. Voltage buffers represent a fundamental building block in high-performance analog and mixed-signal integrated circuits, as they ensure that reference nodes remain stable, accurate, and immune to unwanted perturbations. Their primary role is to provide electrical isolation and driving capability: they decouple the external reference sources from the internal circuitry while actively reproducing the input voltage at the output with negligible static error and minimal dynamic distortion. This prevents loading effects, minimizes the propagation of supply or pad-induced noise, and guarantees proper signal integrity throughout the signal chain.

In the proposed test-chip, the three reference voltages V_{refp}, V_{cm}, and V_{refn} are externally provided to the integrated circuit through dedicated input pads. The accuracy and stability of these references are of paramount importance, as they directly determine the linearity and dynamic range of the DAC core. In order to suppress effects of pad capacitance, package parasitics, and supply-induced fluctuations, on-chip buffering is introduced as a fundamental design requirement. The inclusion of dedicated unity-gain buffers ensures that each reference node exhibits low output impedance and high immunity to transient disturbances, while providing the driving capability needed to the CDAC to properly work. To meet these constraints, three distinct buffer architectures have been developed and optimized, each tailored to the specific electrical characteristics and biasing requirements of the corresponding reference voltage. All three are implemented as single-stage MOS operational amplifiers closed in unity-gain feedback configuration, but they differ in transistor-level topology and biasing strategies to maximize performance within the limited 1.2-V supply headroom.

- **Positive reference buffer (V_{refp}):** implemented with a differential n-MOS input pair and a cascoded p-MOS active load. The gate of the cascode device is biased with the same 900-mV reference input voltage, ensuring proper biasing of the active load. The single-ended output provides a stable reproduction of the positive reference voltage and offers high power-supply rejection and enhanced common-mode disturbance rejection (Fig. 2.26).

- **Common-mode buffer (V_{cm}):** also based on a differential n-MOS input stage with a cascoded p-MOS active load. In this implementation, the cascode transistor is

Transistor	M_B	M_{B1}	M_1	M_2	M_3	M_4	M_5	M_6
Width [µm]	2	20	12	12	12	12	40	40
Lenght [µm]	2	2	1	1	2	2	1	1

TABLE 2.10: Sizing of the positive buffer transistors.

Transistor	M_B	M_{B1}	M_1	M_2	M_3	M_4	M_5	M_6
Width [µm]	4	24	48	48	40	40	40	40
Lenght [µm]	2	2	4	4	0.6	0.6	0.6	0.6

TABLE 2.11: Sizing of the common-mode buffer transistors.

Transistor	M_B	M_{B1}	M_1	M_2	M_3	M_4
Width [µm]	4	32	32	32	12	12
Lenght [µm]	2	2	2	2	6	6

TABLE 2.12: Sizing of the negative buffer transistors.

diode-connected, which simplifies the biasing scheme and enhances stability for the common-mode. The buffer tracks the 600-mV common-mode input voltage and delivers it as a low-impedance single-ended output node, ensuring reliable biasing of the subsequent analog blocks (Fig. 2.27).

- **Negative reference buffer (V_{refn}):** realized with a p-MOS differential input stage and an NMOS active load. The choice of a p-type input differential couple is dictated by biasing reason. Since the input voltage is closer to GND than the supply, having p-type input transistors ensure high voltage dynamic and proper pinch-off region operation (Fig. 2.28).

Through the combination of these three buffer designs, the reference voltages V_{refp}, V_{cm}, and V_{refn} are accurately delivered with the required low output impedance, high linearity, and robustness against external disturbances. This guarantees proper biasing conditions and maximized performance for the DAC. In Tables 2.10, 2.11, and 2.12 are reported all the transistor sizing employed in the positive, common-mode, and negative buffers, respectively.

In addition to their nominal operating mode, all three buffers can be selectively bypassed during testing. This feature allows direct access to the internal reference nodes for characterization and debugging purposes without interference from the buffer circuitry. The bypassing mechanism is controlled by an external digital signal, *BUFFMODE*. When it is asserted high, all buffers are enabled and operate in their nominal unity-gain configuration, thereby propagating the input voltages through their corresponding amplifier stages. Conversely, when *BUFFMODE* is deasserted low (i.e., its complement signal *BUFFMODE_n* is high), the buffers are disabled: the unity-gain feedback loop is opened, and the input node is directly shorted to the output node, effectively bypassing the amplifier. In this test configuration, the load capacitor remains connected to the output node to preserve the same capacitive loading conditions and to ensure proper low-pass filtering of high-frequency noise components. This bypass capability facilitates a flexible testing environment, enabling both buffered and unbuffered operation modes for comprehensive performance evaluation of the DAC core and associated reference network.

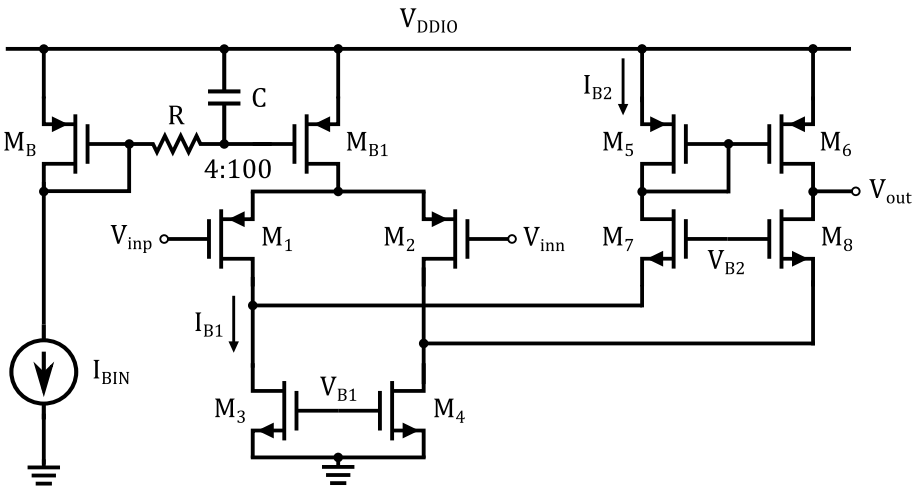


FIGURE 2.29: Schematic of the input buffer.

2.3.6 Input Buffer

In a conventional audio signal acquisition chain, the external analog signal must undergo appropriate conditioning prior to the conversion process. This conditioning stage is typically accomplished through a PreAmplifier (PA), which adjust the signal amplitude, establish impedance matching, and suppress undesired noise components before the signal is presented to the converter. In the proposed testchip, an input buffer has been integrated to fulfill a similar function. Nevertheless, the buffer is architecturally independent of the converter core and is intended primarily as an auxiliary interface to improve signal conditioning during specific measurement scenarios. For this reason, the circuit can be completely disabled and bypassed. Furthermore, the buffer has been intentionally overdesigned to guarantee robustness and linearity across a wide range of operating conditions. As a result, its power consumption has been neglected in the overall chip power estimation as it serve only for testing purpose.

Following these preliminary remarks, the circuit implementation of the input buffer is presented. Figure 2.29 illustrates the complete transistor-level schematic of the input stage. The architecture employs a folded-cascode operational amplifier topology, which is widely recognized for its excellent trade-off between gain, bandwidth, and dynamic range. The choice of a folded-cascode structure was primarily motivated by the following advantages:

- a high intrinsic gain-bandwidth product, enabling accurate reproduction of audio signals;
- a relatively large output voltage swing compared to conventional cascode configurations, improving the available dynamic range;
- enhanced Power Supply Rejection Ratio (PSRR), which mitigates sensitivity to supply perturbations and substrate noise;
- an extended input common-mode range, allowing compatibility with diverse input signal amplitudes and biasing conditions;
- improved stability and reduced susceptibility to process, voltage, and temperature variations.

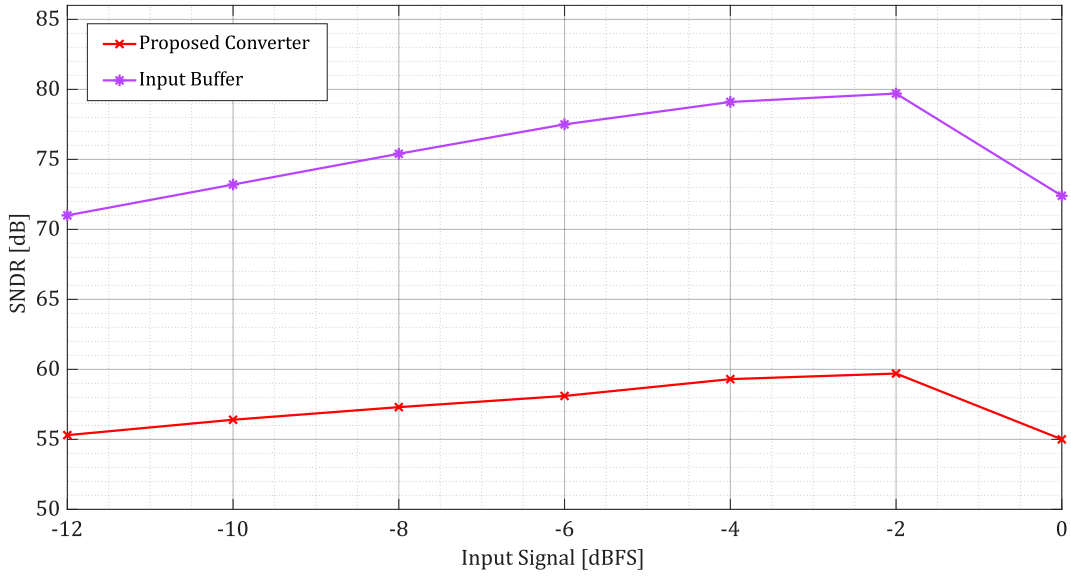


FIGURE 2.30: Simulated SNDR of the input buffer and the proposed testchip as a function of input signal amplitude at 1-kHz input frequency.

These advantages make the folded-cascode architecture particularly suitable for precision analog front-end applications, where both linearity and spectral purity are critical performance metrics. The primary design objective of this stage is to provide a low-distortion interface capable of driving the subsequent CDAC input of the converter while preserving the integrity of the incoming signal. To this end, the circuit was optimized to achieve minimal total harmonic distortion and noise contribution over the entire audio frequency band. To obtain the above mentioned optimizations, the supply voltage V_{DDIO} was set to 1.8 V leading to a more relaxed voltage headroom for the transistor. An RC low pass filter is applied on $M_B - M_{B1}$ gates to suppress thermal noise coming from the current mirror master MOS. From a layout perspective, careful matching techniques were employed, including common-centroid placement and interdigitated structures for the differential input pair, to mitigate mismatch-induced distortion. Parasitic capacitances were minimized to preserve bandwidth and phase margin, while dedicated guard rings were introduced to suppress substrate coupling effects. To validate its design, simulation results in Fig. 2.30 show the comparison of the SNDR between the input buffer and the proposed quasi-passive noise-shaping converter alone as a function of the input signal amplitude. It can be observed that the amplifier exhibits an SNDR that is nearly 20 dB higher than the ADC across the upper limit of dynamic range (from -12 dBFS to 0 dBFS). Therefore, the amplifier linearity can be considered significantly superior, and its contribution to overall distortion becomes negligible when cascaded with the converter. In summary, the inclusion of a fully bypassable folded-cascode input buffer provides the test chip with a flexible and high-performance signal conditioning stage. Its careful

Specification	Loop Gain	BW @ 0 dB	PM	Total In-Band Noise	I_{tot}	Supply Voltage
Value	68 dB	11 MHz	66°	24 µV	700 µA	1.8 V

TABLE 2.13: Simulated performance of the input buffer.

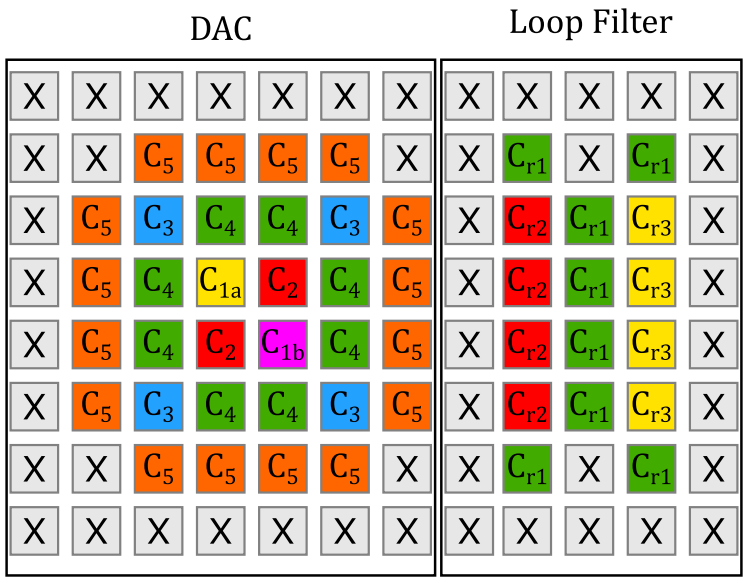


FIGURE 2.31: DAC and LF capacitors displacement.

design ensures excellent linearity, low noise, and robust isolation from external disturbances, thereby enhancing the overall measurement accuracy and versatility of the integrated system. The simulated performance of the input buffer are reported in Tab. 2.13.

2.4 Layout and Fabrication

After the completion of the schematic design and circuit-level verification phases, the next critical step in the integrated circuit development flow is the physical implementation, or layout design, of the chip. The layout process translates the verified electrical schematics into a geometrical representation composed of layers corresponding to the various materials and fabrication steps used in CMOS technology. This stage bridges the gap between the abstract circuit description and the actual physical realization of the silicon device, ensuring that all transistors, interconnections, and passive components are properly instantiated, dimensioned, and arranged within the available silicon area. During this phase, particular attention is devoted to device matching, parasitic minimization, and Layout-Dependent Effects (LDEs), which play a crucial role in determining the final circuit performance. Techniques such as common-centroid placement, interdigitated device structures, and symmetric routing are employed to enhance mismatch immunity and to preserve signal integrity. Furthermore, Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verifications are systematically performed to ensure full compliance with the foundry technological constraints and to guarantee electrical consistency with the original schematic. Once the layout is finalized and all verification steps are successfully passed, the design is submitted for fabrication through the semiconductor foundry.

A significant emphasis was placed on the layout of both the capacitive digital-to-analog converter and the loop filter, as these components are particularly sensitive to fabrication-induced variations. Both capacitive mismatch and parasitic capacitances can severely degrade the effective resolution of the system, as discussed in Sections 2.1.4 and 2.3.1, respectively. To mitigate these effects, two layout strategies were implemented for both the CDAC and the loop filter. The primary approach adopted for the CDAC is a

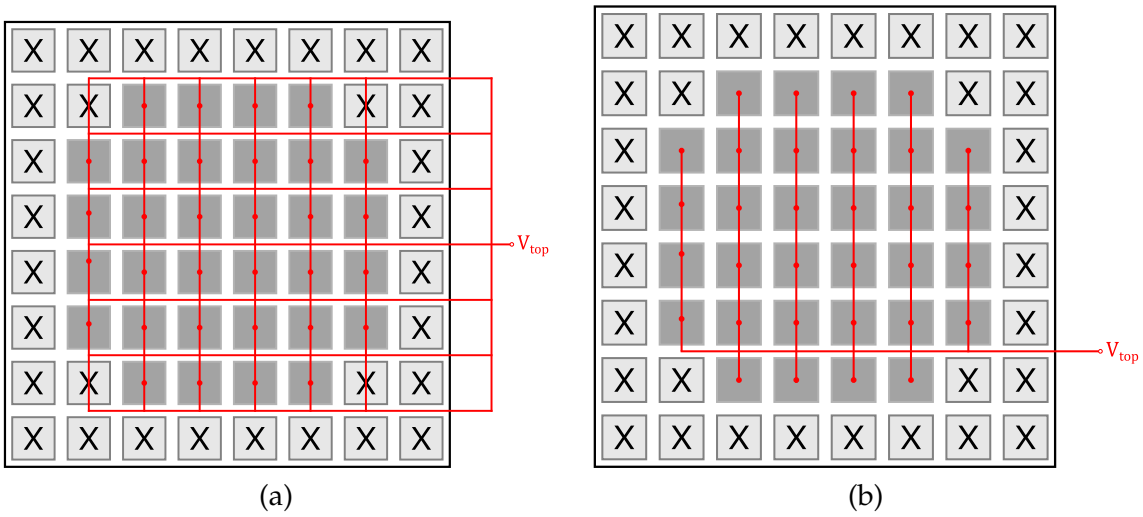


FIGURE 2.32: Scheme of (a) a symmetric V_{top} node CDAC routing and (b) the employed asymmetric CDAC routing for the V_{top} node.

common-centroid arrangement of the unit capacitors. As illustrated in Fig. 2.31, the 32 capacitors are organized to minimize the impact of process gradients and local fabrication non-uniformities. Specifically, the smallest unit capacitors, denoted as C_{1a} and C_{1b}, corresponding to the least significant bit and the fixed reference capacitor, respectively, are positioned at the geometric center of the array. The larger capacitors, namely C_2, C_3, C_4, and C_5, representing bits 2 through 5 (with C_5 being the MSB), are arranged symmetrically around the central capacitors. This hierarchical spatial distribution serves to evenly distribute potential gradient-induced variations, temperature effects, and process fluctuations across the array, thereby improving linearity and matching performance across all bits. For the loop filter, a slightly different layout strategy is adopted, reflecting its distinct capacitance values and electrical requirements. The largest capacitor, C_{r1}, is placed at the center to reduce gradient sensitivity, while the smaller capacitors, C_{r2} and C_{r3}, each half the size of C_{r1}, are symmetrically positioned on either side of the central element. In both CDAC and LF arrays, all capacitors are aligned on a regular grid and equidistantly spaced to ensure uniform electric field distribution and to minimize parasitic coupling. To further improve matching and reduce edge effects, a peripheral ring of dummy capacitors is placed around both arrays. These dummy elements are identical in size to the functional capacitors but remain electrically unconnected, preserving structural continuity. However, albeit the employed custom mom effectively shield the node V_{top} from parasitic couplings toward the substrate, the routing of this node represented a critical aspect during the layout phase and required careful optimization. An example of a symmetric routing strategy is shown in Fig. 2.32a. This approach allows an even distribution and balancing of parasitic components across all DAC capacitors, which is beneficial from a matching perspective; however, it leads to a significant increase in the overall parasitic capacitance associated with the TOP node. Post-layout simulation results indicate that the adoption of an asymmetric layout solution, such as the one illustrated in Fig. 2.32b, while introducing a higher degree of imbalance (and thus distortion) in the distribution of parasitic capacitances toward the substrate, yields a less pronounced degradation of the SNDR. Compared to a fully symmetric routing strategy, this asymmetric approach therefore represents a more favorable trade-off between parasitic capacitance, matching accuracy, and overall dynamic performance.

Fabricated in 65 nm GlobalFoundries (GF) CMOS technology the active core occupies

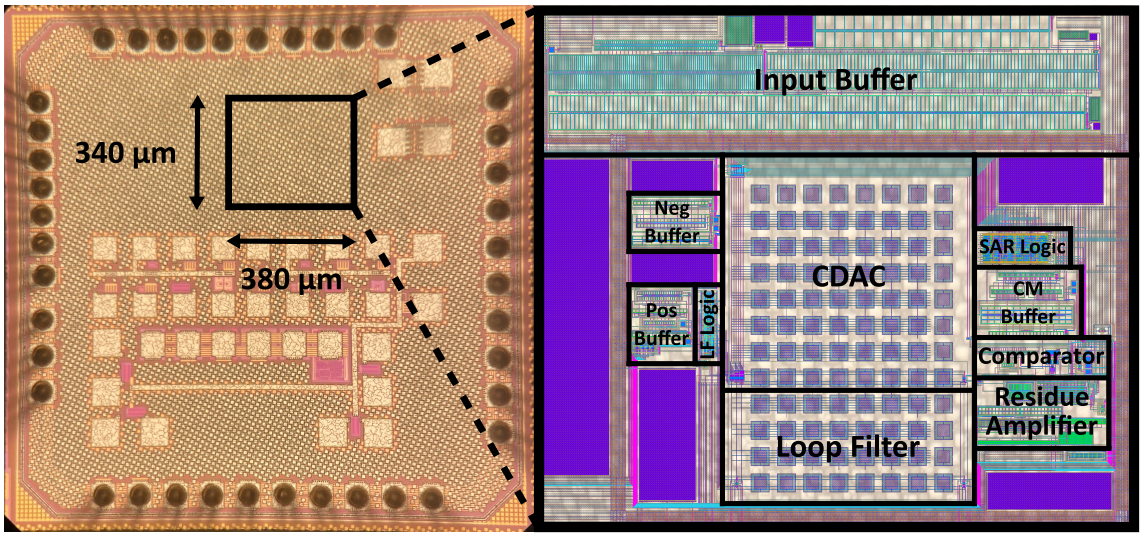


FIGURE 2.33: Die micro-graph and detail of the layout.

380 µm x 340 µm for a total silicon area of 0.129 mm^2. Figure 2.33 presents the final chip layout alongside the micrograph of the fabricated test chip. The CDAC and loop filter structures occupy a central position within the core region, surrounded by the remaining analog and digital blocks. On the right-hand side of the layout, the SAR logic, comparator, residue amplifier, and common-mode reference buffer are located, whereas the left side hosts the loop filter logic along with the positive and negative reference buffers. Residual layout gaps are filled with buffer load capacitors (highlighted in violet in the figure). The input buffer is positioned at the top of the layout, providing convenient routing for incoming signals while maintaining signal integrity across the core. Through careful

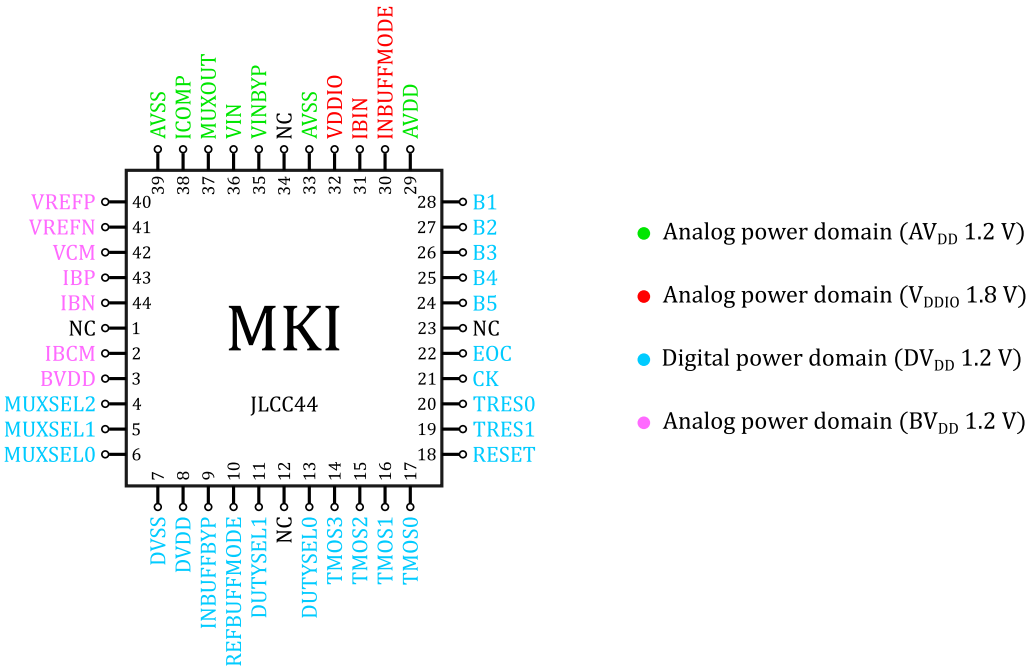


FIGURE 2.34: Pinout diagram of the proposed testchip.

attention to placement, symmetry, and hierarchical arrangement, the layout ensures that both the CDAC and the loop filter maintain high linearity, low mismatch, and robustness against process-induced variations, thereby maximizing the overall performance of the fabricated test chip.

For testing purpose, a ceramic JLCC44 is chosen as package. This packaging solution offers superior thermal stability, mechanical robustness, and low parasitic effects, enabling precise electrical evaluation. Figure 2.34 shows the pinout diagram of the *MKI* testchip. It can be seen how the four power domain are separated in order keep divided and well organized the padring supplies. The complete list of the 44 pins, including their descriptions and corresponding power domains, can be found in Tab. B.1 in the Appendix B.

Chapter 3

MKI Test Chip Measurements Results

COMPREHENSIVE characterization of the *MKI* testchip is presented in this chapter. The experimental activities were conducted to validate the functionality and assess the electrical performance of the integrated circuit under various operating conditions. The measurement campaign aimed to verify the design correctness and to evaluate the impact of process and temperature variations on the overall performance of the device. To enable accurate and repeatable measurements, a dedicated measurement setup was assembled. A custom printed circuit board (PCB) was designed and fabricated to interface the testchip with the laboratory instrumentation. The PCB provides controlled impedance signal routing, decoupling capacitors for power supply stabilization, test access points for monitoring critical nodes, and component redundancy in order to provide a large flexibility for different types of tests.

The *MKI* testchip, fabricated in 65 nm GlobalFoundries CMOS technology, was packaged in a JLCC44 ceramic package. This package was mounted on a socketed interface, allowing for convenient replacement and testing of multiple dies without the need for re-soldering, thus facilitating extensive parametric and functional analysis. The measurement environment was carefully configured to ensure stable and low-noise operation. High-precision audio signal generator, digital oscilloscopes, and logic analyzer were employed to perform voltage, current, and timing characterizations. The setup further supports temperature-controlled testing, enabling systematic investigation of the device behavior across a wide temperature range.

In summary, this chapter describes the complete methodology adopted for the electrical characterization of the *MKI* testchip, detailing the hardware setup. The obtained results, presented in the following sections, provide valuable insights into the performance and reliability of the design, and form the foundation for further optimization and design validation.

3.1 PCB Design and Layout

To provide an accurate interface between the IC and the external signals, a PCB was design and fabricated. Its role is to correctly deliver stable and low-noise signal and supplies voltages and provide the interface circuitry to allow the proper reading and evaluation of the output signals.

3.1.1 PCB Design

In Fig. 3.1, the complete schematic of the PCB is shown and its pin by pin description, following the pin list reported in Appendix B, is presented:

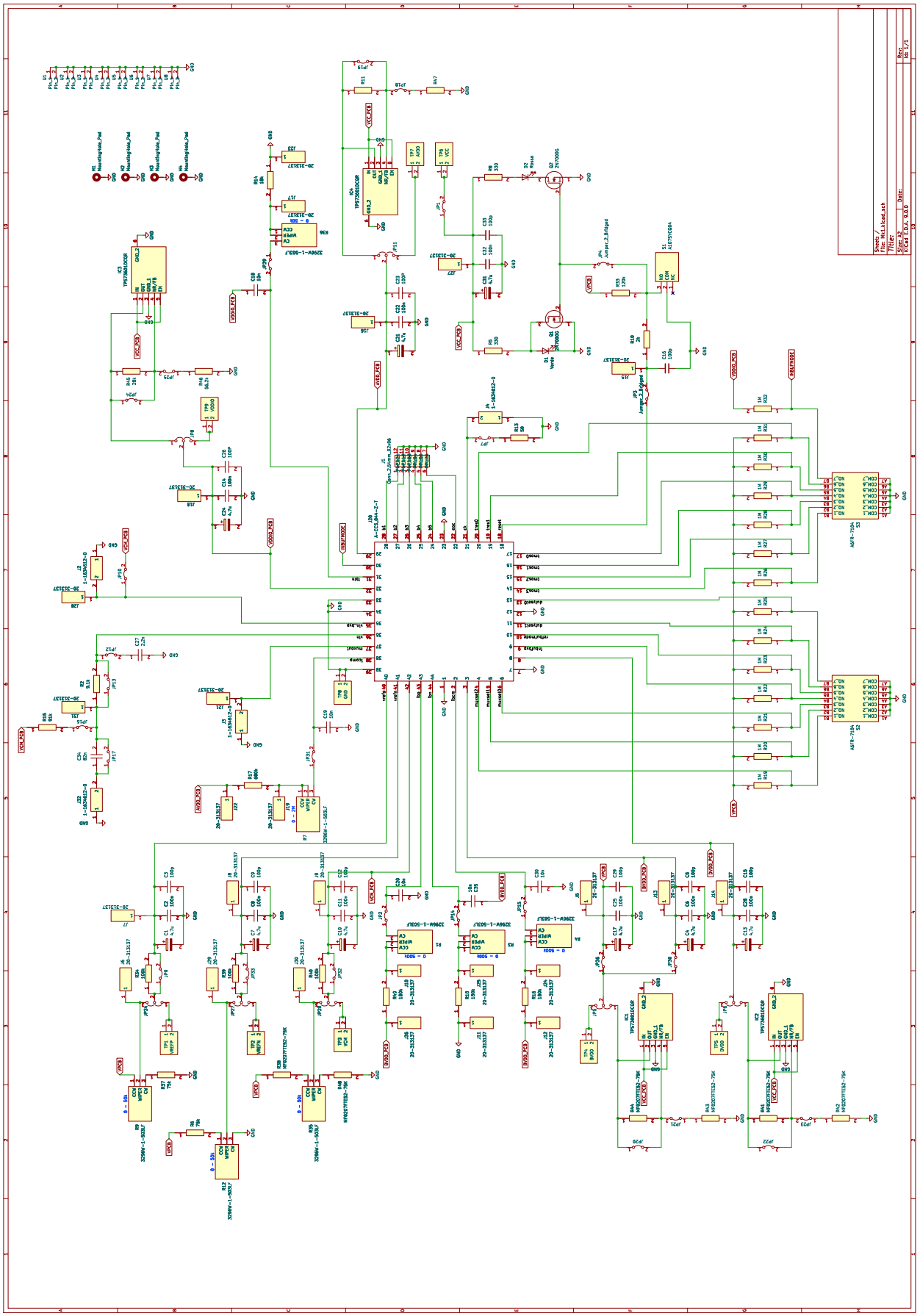


FIGURE 3.1: Complete schematic of the PCB.

- **NC [Pin 1]**: Not connected.
- **IBCM [Pin 2]**: The current reference for the common-mode buffer (I_{BCM}) is delivered through a cascade of a fixed and a variable resistor. This method allows an easy and fine tuning of the current by simply monitoring the voltage drop on the fixed 180 kΩ resistor (R_{16}) and by modifying the 0÷500 kΩ trimmer (R_4) to obtain the desired current. The fixed resistor sets the maximum allowable current that can be drawn from the supply. A 10 nF capacitor (C_{30}) is placed near the testchip IBMC input pin to filter out high frequency noise.
- **BVDD [Pin 3]**: The buffer supply voltage (BV_{DD}) is delivered in two ways for redundancy. The first method exploits an on-board Texas Instrument TPS73601DCQ high-accuracy ultra-low dropout (LDO) linear voltage regulator ($IC1$) to generate the 1.2-V voltage [44]. Resistors R_{43} and R_{44} set the voltage divider ratio to the NR/FB pin of the LDO to allow the correct generation of BV_{DD}. The second method consists in applying the voltage from an external DC supply generator through a banana connector (TP_4) on the board. The two methods were implemented for redundancy, as only one can operate at a time. However, this redundancy allows for selecting the most suitable method depending on the type of measurement to be performed. While the voltage supplied by the LDO is more accurate and exhibits lower noise, it is not finely adjustable. The second method, on the other hand, enables the observation of how variations in BV_{DD} affect the circuit. This voltage is used for two different purpose. Filtering it through C_{17}, C_{25} and C_{29} of 4.7 µF, 100 nF and 100 pF respectively, V_{PCB} is created, which is the on-board 1.2-V auxiliary supply voltage. On the other hand, BV_{DD}, after being filtered by C_4, C_6 and C_5 of 4.7 µF, 100 nF and 100 pF respectively, become BV_{DD_PCB} which is the actual input voltage for pin #3.
- **MUXSEL2 [Pin 4]**: The MSB of the digital input signal MUXSEL (MUXSEL2) is provided through an external Dual In-line Package (DIP) switch (S_2) and a pull-up resistor (R_{19}). The combination of these two elements ensures that the signal is reliably driven, so that both the logical 0 and logical 1 levels are well-defined. MUXSEL is a 3-bit control signal that drives an internal multiplexer implemented for Design-For-Testability (DFT) functionality. Its purpose is to connect a desired internal node to a dedicated pad in order to be able to access and measure internal nodes. The accessible nodes and the MUXSEL truth table is reporter in Tab. C.1 in Appendix C.
- **MUXSEL1 [Pin 5]**: The second bit of the digital input signal MUXSEL (MUXSEL1) is provided through an external DIP switch (S_2) and a pull-up resistor (R_{20}).
- **MUXSEL0 [Pin 6]**: The LSB of the digital input signal MUXSEL (MUXSEL0) is provided through an external DIP switch (S_2) and a pull-up resistor (R_{21})
- **DVSS [Pin 7]**: The digital ground DV_{SS} is connected to the PCB common ground.
- **DVDD [Pin 8]**: The digital supply voltage (DV_{DD}) is delivered in two ways for redundancy. The first method exploits an on-board Texas Instrument TPS73601DCQ high-accuracy ultra-low dropout linear voltage regulator ($IC2$) to generate the 1.2-V voltage. Resistors R_{41} and R_{42} set the voltage divider ratio to the NR/FB pin of the LDO to allow the correct generation of DV_{DD}. The second method consists in just applying the voltage from an external DC supply generator through a banana connector (TP_5) on the board. Capacitors C_{13}, C_{28} and C_{15} of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.

- **INBUFBYP [Pin 9]**: The bypass and disable digital signal of the input buffer (INBUFBYP) is provided through an external DIP switch (S_2) and a pull-up resistor (R_{22}). This active-high signal enables the input buffer bypass in order to give the possibility to provide directly from outside the input audio signal.
- **REFBUFMODE [Pin 10]**: The digital input signal REFBUFMODE is provided with an external DIP Switch (S_2) and a pull-up resistor (R_{23}). This active-high signal enables all three buffers. When set to '0' it turns off the buffers and enable their bypass in order to give the possibility to provide directly from outside the references signals.
- **DUTYSEL1 [Pin 11]**: The MSB of the digital input signal DUTYSEL (DUTYSEL1) is provided through an external DIP switch (S_2) and a pull-up resistor (R_{24}). The DUTYSEL signal controls the duty-cycle of the residue amplifier and its truth table is reporter in Tab. C.2 in Appendix C.
- **NC [Pin 12]**: Not connected.
- **DUTYSEL0 [Pin 13]**: The LSB of the digital input signal DUTYSEL (DUTYSEL1) is provided through an external DIP Switch (S_2) and a pull-up resistor (R_{25}).
- **TMOS3 [Pin 14]**: The MSB of the digital input signal TMOS (TMOS3) is provided through an external DIP switch (S_3) and a pull-up resistor (R_{26}). TMOS is a 4-bit control signal that trims transistor M_{B7} of the residue amplifier to counteract process-induced mismatches (2.3.2). Its truth table ad the trimming specifications are reported in Tab. C.3 in Appendix C.
- **TMOS2 [Pin 15]**: The second bit of the digital input signal TMOS (TMOS2) is provided through an external DIP switch (S_3) and a pull-up resistor (R_{27}).
- **TMOS1 [Pin 16]**: The third bit of the digital input signal TMOS (TMOS1) is provided through an external DIP Switch (S_3) and a pull-up resistor (R_{28}).
- **TMOS0 [Pin 17]**: The LSB of the digital input signal TMOS (TMOS0) is provided through an external DIP switch (S_3) and a pull-up resistor (R_{29}).
- **RESET [Pin 18]**: The digital input signal RESET is delivered through an external switch (S_1), a pull-up resistor (R_{33}) and an RC debounce circuit. The debounce circuit employs a 2 kΩ series resistor and a 100 pF parallel capacitor that filter out the unwanted physical bounce of the switch contacts that can cause multiple false transitions. The RESET signal is an active-high signal that resets both SAR and LF digital logics.
- **TRES1 [Pin 19]**: The MSB of the digital input signal TRES (TRES1) is provided through an external DIP switch (S_3) and a pull-up resistor (R_{30}). TRES is a 2-bit control signal that trims resistor R_B of the residue amplifier to counteract process-induced mismatches (2.3.2). Its truth table ad the trimming specifications are reported in Tab. C.4 in Appendix C.
- **TRES0 [Pin 20]**: The LSB of the digital input signal TRES (TRES0) is provided through an external DIP switch (S_3) and a pull-up resistor (R_{31}).
- **CK [Pin 21]**: The CK input signal is provided externally through a coaxial BNC connector (J_4). A 50 Ω matching resistor (R_{13}) is also added to ensure line matching.

- **EOC [Pin 22]**: The digital output signal EOC is routed to a single pin of the 12-pin connector (J_1).
- **NC [Pin 23]**: Not connected.
- **B5 [Pin 24]**: The MSB of the digital output signal B (B5) is routed to a single pin of the 12-pin connector (J_1). Signal B is the 5-bit output digital stream of the converter.
- **B4 [Pin 25]**: The second bit of the digital output signal (B4) is routed to a single pin of the 12-pin connector (J_1).
- **B3 [Pin 26]**: The third bit of the digital output signal (B3) is routed to a single pin of the 12-pin connector (J_1).
- **B2 [Pin 27]**: The fourth bit of the digital output signal (B2) is routed to a single pin of the 12-pin connector (J_1).
- **B1 [Pin 28]**: The LSB of the digital output signal (B1) is routed to a single pin of the 12-pin connector (J_1).
- **AVDD [Pin 29]**: The analog supply voltage (AV_{DD}) is delivered in two ways for redundancy. The first method exploits an on-board Texas Instrument TPS73601DCQ high-accuracy ultra-low dropout linear voltage regulator ($IC4$) to generate the 1.2-V voltage. Resistors R_{11} and R_{47} set the voltage divider ratio to the NR/FB pin of the LDO to allow the correct generation of AV_{DD}. The second method consists in just applying the voltage from an external DC supply generator through a banana connector (TP_7) on the board. Capacitors C_{21}, C_{22} and C_{23} of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.
- **INBUFMODE [Pin 30]**: The digital input signal INBUFMODE is provided through an external DIP switch (S_3) and a pull-up resistor (R_{32}). This active-high signal enables the input buffer.
- **IBIN [Pin 31]**: The input buffer reference current (I_{BIN}) is delivered through a cascade of a fixed and a variable resistor. Monitoring the voltage drop on the fixed 18 kΩ resistor (R_{14}) and modifying the $0 \div 50$ kΩ trimmer R_{36}, allows to obtain the desired current. The fixed resistor sets the maximum allowable current that can be drawn from the supply. A 10 nF capacitor (C_{18}) is placed near the testchip IBIN input pin to filter out high frequency noise.
- **VDDIO [Pin 32]**: The analog supply voltage for the input buffer and for the pad ring (V_{DDIO}) is delivered in two ways for redundancy. The first method exploits an on-board Texas Instrument TPS73601DCQ high-accuracy ultra-low dropout linear voltage regulator ($IC3$) to generate the 1.8-V voltage. Resistors R_{45} and R_{46} set the voltage divider ratio to the NR/FB pin of the LDO to allow the correct generation of V_{DDIO}. The second method consists in applying the voltage from an external DC supply generator through a banana connector (TP_9) on the board. Capacitors C_{24}, C_{14} and C_{26} of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.
- **AVSS [Pin 33]**: The analog ground AV_{SS} is connected to the PCB common ground.
- **NC [Pin 34]**: Not connected.
- **VINBYP [Pin 35]**: When the input amplifier is not employed, the audio input signal is directly delivered to the IC through a coaxial BNC connector (J_2).

- **VIN [Pin 36]**: When the input amplifier is employed, the audio input signal is delivered to the IC through a coaxial BNC connector (J_{32}) and a band-pass filter made of a 82 nF capacitor (C_{34}), a 91 kΩ resistor (R_{15}), a 9.1 kΩ resistor (R_2), and a 2.2 nF capacitor (C_{27}).

- **MUXOUT [Pin 37]**: The analog/digital multiplexer output signal MUXOUT is routed to a coaxial BNC connector (J_3).

- **ICOMP [Pin 38]**: The comparator reference current (I_{COMP}) is delivered through a cascade of a fixed and a variable resistor. Monitoring the voltage drop on the fixed 680 kΩ resistor (R_{17}) and modifying the 0÷2 MΩ trimmer R_7, allows to obtain the desired current. The fixed resistor sets the maximum allowable current that can be drawn from the supply. A 10 nF capacitor (C_{19}) is placed near the testchip ICOMP input pin to filter out high frequency noise.

- **AVSS [Pin 39]**: The analog ground AV_{SS} is connected to the PCB common ground.

- **VREFP [Pin 40]**: The positive reference voltage (V_{refp}) is delivered in two ways to provide redundancy. The first method exploits a cascade of a 0÷50 kΩ trimmer R_9) and a 75 kΩ fixed resistor R_{37} to generate the 0.9-V voltage. The fixed resistor sets the minimum allowable voltage while the trimmer allows its fine tuning. The second method consists in applying the voltage from an external DC supply generator through a banana connector (TP_1) on the board. A 100 kΩ resistor R_{34} and three capacitors C_1, C_2 and C_3 of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.

- **VREFN [Pin 41]**: The negative reference voltage (V_{refn}) is delivered in two ways to provide redundancy. The first method exploits a cascade of a 0÷50 kΩ trimmer R_{12} and a 75 kΩ fixed resistor R_6 to generate the 0.3-V voltage. The fixed resistor sets the maximum allowable voltage while the trimmer allows its fine tuning. The second method consists in applying the voltage from an external DC supply generator through a banana connector (TP_2) on the board. A 100 kΩ resistor R_{39} and three capacitors C_7, C_8 and C_9 of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.

- **VCM [Pin 42]**: The common-mode reference voltage (V_{cm}) is delivered in two ways to provide redundancy. The first method exploits a cascade of a 75 kΩ fixed resistor R_{38}, a 0÷50 kΩ trimmer R_{35} and a second 75 kΩ fixed resistor R_{48} to generate the 0.6-V voltage. The two fixed resistors set the minimum and maximum allowable voltage while the trimmer allows its fine tuning. The second method consists in just applying the voltage from an external DC supply generator through a banana connector (TP_3) on the board. A 100 kΩ resistor R_{40} and three capacitors C_{10}, C_{11} and C_{12} of 4.7 µF, 100 nF and 100 pF respectively, are used to filter out high frequency noise.

- **IBP [Pin 43]**: The positive buffer reference current (I_{BP}) is delivered through a cascade of a fixed and a variable resistor. Monitoring the voltage drop on the fixed 180 kΩ resistor (R_{49}) and modifying the 0÷500 kΩ trimmer R_1, allows to obtain the desired current. The fixed resistor sets the maximum allowable current that can be drawn from the supply. A 10 nF capacitor (C_{20}) is placed near the testchip IBP input pin to filter out high frequency noise.

- **IBN [Pin 44]**: The negative buffer reference current (I_{BN}) is delivered through a cascade of a fixed and a variable resistor. Monitoring the voltage drop on the fixed

180 kΩ resistor (R_{18}) and modifying the 0÷500 kΩ trimmer R_3, allows to obtain the desired current. The fixed resistor sets the maximum allowable current that can be drawn from the supply. A 10 nF capacitor (C_{35}) is placed near the testchip IBN input pin to filter out high frequency noise.

3.1.2 PCB Layout

After the completion of the schematic design phase, the finalized printed circuit board layout is presented. In Fig. 3.2, the complete topology of the double–sided PCB, designed on an FR-4 substrate, is depicted. The board layout has been developed with particular attention to signal integrity, Electro-Magnetic Compatibility (EMC), and minimization of parasitic elements that may degrade analog performance. Since the integrated circuit pinout is already partitioned into distinct power and functional domains, the PCB interconnections follow the same separation guidelines. All digital signals associated with pins 4 through 28 are primarily static logic signals, which inherently present negligible risk of crosstalk or dynamic interference. Consequently, these lines can be routed without strict high-speed layout constraints. The only exception is the Clock Signal (CK), which is a high-frequency dynamic signal; special care has been taken to route CK with controlled impedance and minimal loop area to prevent unwanted coupling with adjacent analog or sensitive digital lines. In the lower–right quadrant, the routing of the complete 1.8-V domain is placed, along with the auxiliary on-board 5-V supply (V_{CC}), to ensure clear isolation from the sensitive analog front-end. The right side accommodates the input audio signal and the multiplexer output, where careful trace length equalization and minimization of loop areas have been implemented to reduce susceptibility to external noise sources. The upper region of the PCB hosts the power regulation stages, including linear regulators, local decoupling networks, and filtering structures. To reduce voltage

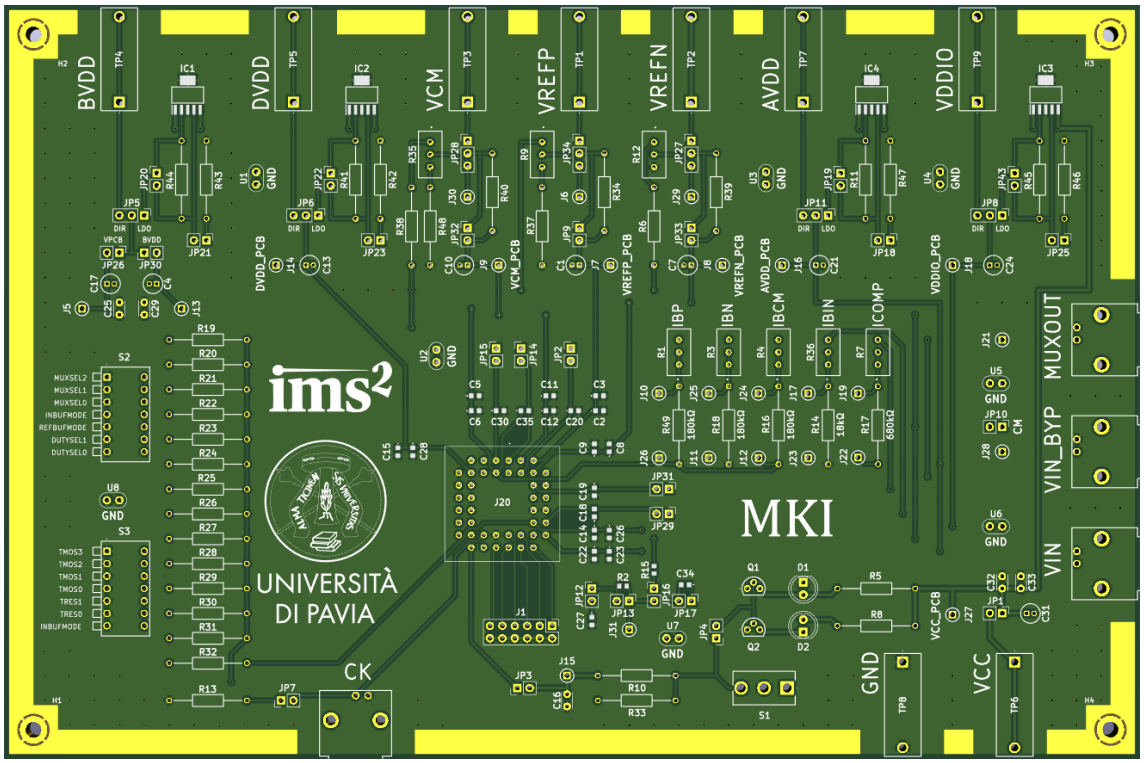


FIGURE 3.2: Layout rendering of the PCB.

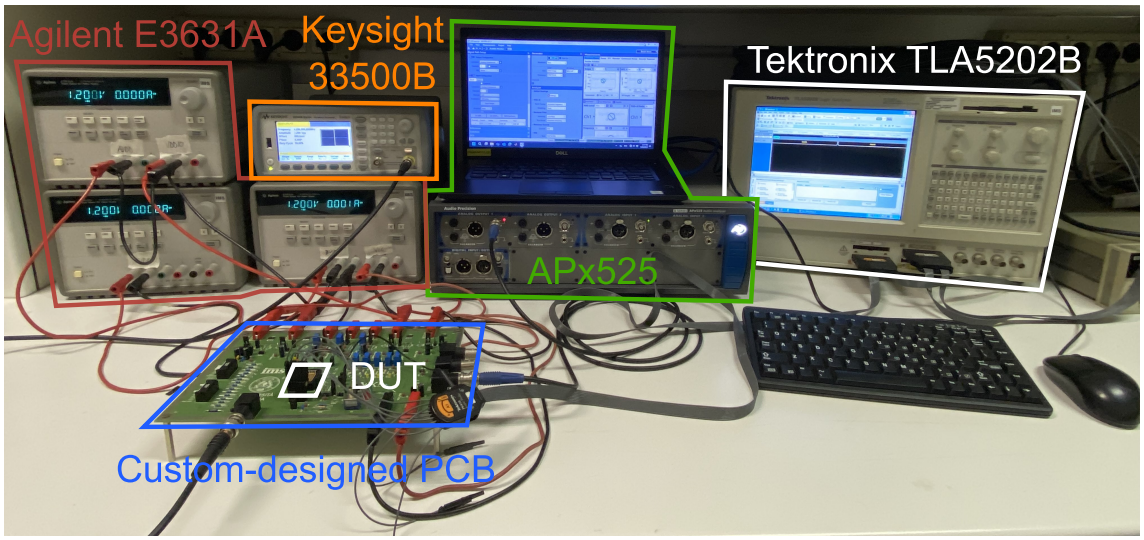


FIGURE 3.3: Measurement setup.

ripple and supply impedance, all decoupling capacitors are placed according to best practice guidelines, ensuring the shortest possible paths to the IC pins. A continuous common ground plane is distributed across both copper layers, guaranteeing low-impedance grounding and maximizing equipotentiality. Strategic stitching vias have been inserted to further suppress ground discontinuities and to reinforce shielding effectiveness. To facilitate laboratory debugging, in-circuit testing, and performance validation, a total of 30 measurement nodes are implemented and labeled as test points (J_x, where $x \in [2, 31]$). In addition, 8 dedicated ground reference access points (U_x, where $x \in [1, 8]$) are provided to ensure accurate probing and noise-free reference accessibility during diagnostics. Regarding component assembly, Through-Hole Technology (THT) discrete components are primarily chosen for simplicity and to simplify manual soldering. Surface-Mounted Devices (SMDs), such as filtering resistors and capacitors located in close proximity to the IC pins, are employed to minimize lead inductance and reduce parasitic coupling.

3.2 Measurement

Two measurement campaigns were conducted to fully characterize the MK1 test chip. The complete measurement setup of the first campaign is shown in Fig. 3.3. The PCB, containing the Device Under Test (DUT), was connected to three Agilent E3631A DC power supplies, providing the five required supply voltages: 1.2 V for the analog (AV_{DD}), digital (DV_{DD}), and buffer (BV_{DD}) domains; 1.8 V for the input buffer and pad ring supplies (V_{DDIO}); and 5 V for the auxiliary on-board supply (V_{CC}). The 4.096 MHz clock signal was generated by a Keysight 33500B waveform generator. With a jitter below 40 ps, a total harmonic distortion lower than 0.04%, and a 16-bit resolution, the generator ensures a precise and low-jitter clock signal, thereby improving measurement reliability and accuracy. To further minimize external interference and ensure that the measured results reflected only the intrinsic performance of the IC, the input audio signal was generated using an Audio Precision® APx525 audio analyzer. This modular, two-channel instrument exhibits extremely low noise (typical THD+N < –110 dB), wide bandwidth (>1 MHz), and a broad frequency range (0.1 Hz ÷ 80.1 kHz), allowing the generation of a high-fidelity audio signal. The digital output data were captured using a Tektronix TLA5202B logic analyzer. Post-processing of the input data were done in MATLAB®.

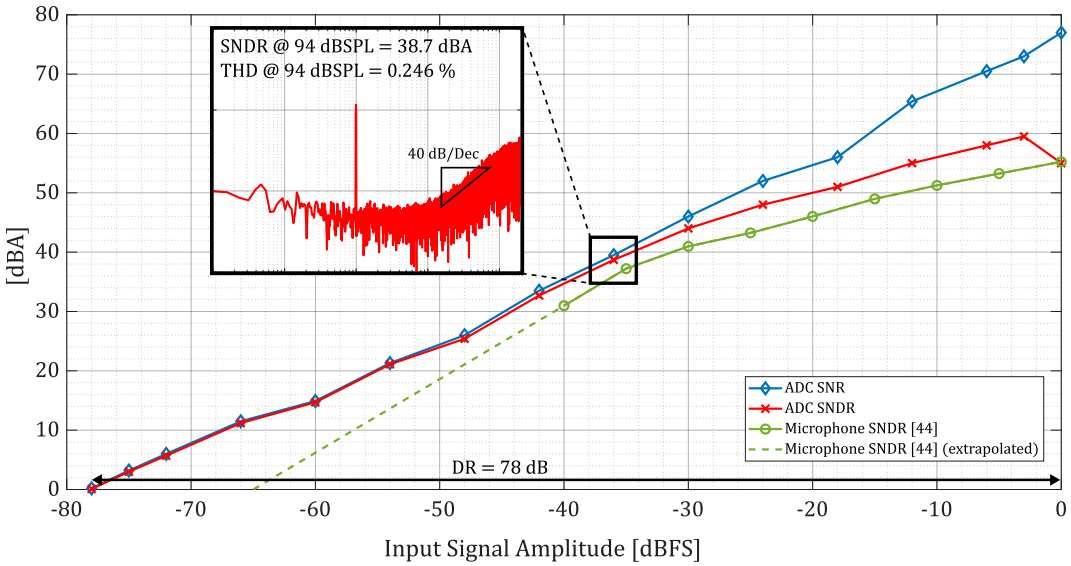


FIGURE 3.4: Measured A-Weighted ADC SNR/SNDR and microphone [45] SNDR as a function of the input signal amplitude at 1-kHz input frequency.

This consisted in performing the decimation and Fast Fourier Transform (FFT) analysis. The first operation consists in applying a digital low-pass filter to remove the out-of-band noise that was spread across the wider frequency band. Then, the sample rate is reduced by the decimation factor, which is often achieved by averaging or downsampling the filtered data. After this, on the reconstructed signal is applied an FFT in order to extract its Power Spectral Density (PSD) and evaluate its SNR, SNDR, and THD.

The second measurement campaign employed the same instrumentation. However, the PCB and DUT were placed inside an ACS DY110 C-model climatic chamber to evaluate device performance over different ambient temperatures. In this setup, supply voltages were generated on board using Texas Instruments TPS73601DCQ high-accuracy ultra-low-dropout linear voltage regulators. All the previous test were repeated across a temperature range that spans from $-40\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$.

The results obtained from both measurement campaigns are discussed in the following subsection.

3.2.1 Measurement Results

Due to the intrinsic gain attenuation showed in (2.14), the input signal range of this converter is set to $800\,\mathrm{mV_{pp}}$ centered around a common mode voltage of 600 mV. The maximum input signal (0 dBFS), which corresponds to the 140 dBSPL ADC Full-Scale (FS), is reached when V_{in} ranges from 200 mV to 1 V. As shown in Fig. 3.4, sweeping the input signal from the minimum value that produces a quantificable output (-78 dBFS) to the FS, the proposed converter reaches a peak Signal-to-Noise-and-Distortion-Ratio (SNDR) at -3 dBFS of 59.5 dBA (A-weighted). With a standard 94-dBSPL 1-kHz sinusoidal input tone, which correspond to -36 dBFS ($12.5\,\mathrm{mV_{pp}}$), the frequency spectrum shows a second order noise-shaping with a 40 dB/decade slope and the measured SNDR and THD are 38.7 dBA and 0.246 %, respectively. For comparison purpose, in the graph is also reported the performance of typical commercial analog microphones (green curve) [45]. It is possible to observe that the SNDR degradation for large input signals is consistent

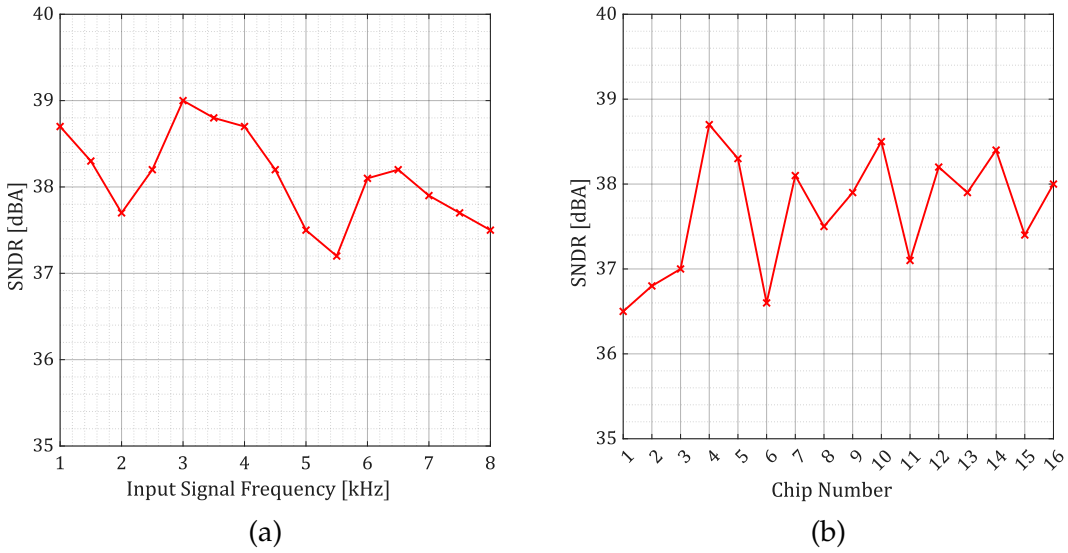


FIGURE 3.5: Measured SNDR at 94 dBSPL as (a) a function of the input signal frequency and (b) a function of the fabricated microchips.

with the performance of the microphone in this range. Figure 3.5a depicts the measured SNDR variation as a function of the frequency or the sinusoidal input. Throughout the whole input bandwidth, that ranges from 20 Hz to 8 kHz, no appreciable degradation in the SNDR occurs. The converter performance was verified experimentally considering a batch of 16 samples, taken from the same wafer lot. In Fig. 3.5b are reported the values of SNDR measured with a 94 dBSPL, 1 kHz input signal for all the available samples. Thanks to the trimming operations performed on the residue amplifier, the measured SNDR spread between the samples is less than 3 dB.

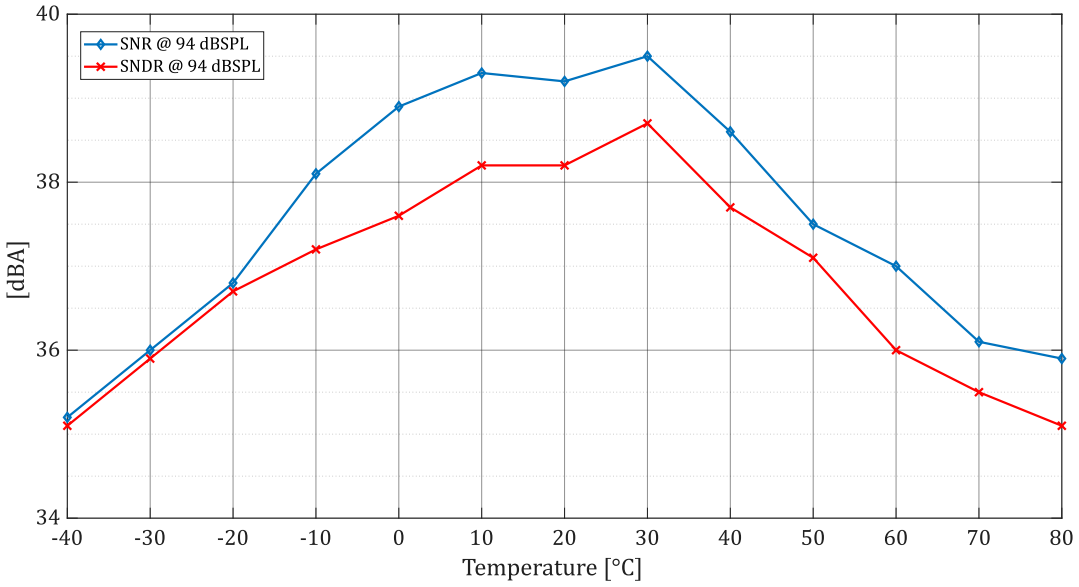


FIGURE 3.6: Measured SNDR as a function of the operating temperature at 94 dBSPL.

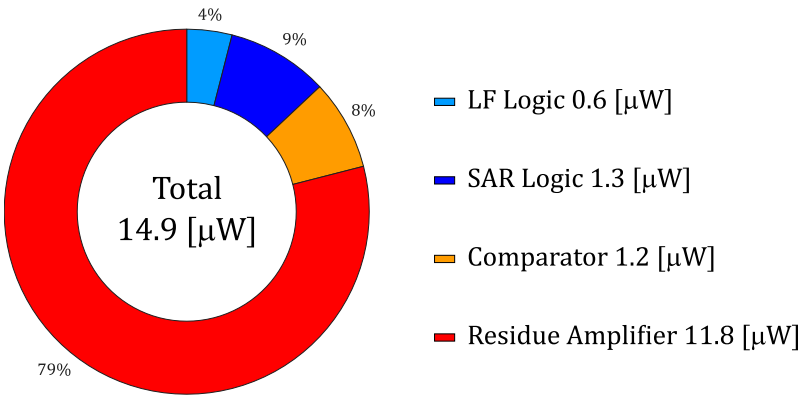


FIGURE 3.7: Core power consumption breakdown.

Using a climatic chamber, it was possible to perform measurements at different temperatures. As reported in Fig. 3.6, both SNR and SNDR of the A/D converter maintain excellent values from $-40\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$. The complete ADC core, during a conversion, draws 14.9 µW from a 1.2-V supply. Figure 3.7 exhibits how the total power consumption is divided among the most important blocks that compose the ADC. Most of the power is consumed by the residue amplifier, followed by the SAR logic and the comparator.

Chapter 4

Conclusions

OVERALL, this doctoral thesis, presents the study, design and validation of an ultra-low power analog-to-digital converter especially suited for audio activity detection applications. The proposed architecture relies on a simple yet highly effective hybrid quasi-passive error-feedback topology that leverages oversampling and noise-shaping techniques to enhance the intrinsic performance of a 5-bit successive approximation register converter. Through this combination, the system achieves high resolution and low noise while simultaneously reducing overall power consumption, a key requirement for always-on devices. The converter was designed and fabricated in a 65-nm BCD technology and a comprehensive summary of the design choices together with the silicon measurement results is provided in Tab. 4.1. The input audio bandwidth spans from DC up to 8 kHz, matching the requirements of low-power acoustic front-ends used in voice-trigger and ambient-sound recognition systems. The core of this converter is a 600 mV_{pp} full-scale 5-bits bottom-sampling SAR, with a second-order quasi-passive noise-shaping loop filter. Thanks to the combination of quasi-passive filtering and a 32 OSR oversampling, a final resolution of 12.61 bits of ENOB are reached. At an input level of 94 dBSPL (commonly adopted as the standard reference operating point for audio devices) the measured SNDR reaches 38.7 Given a total core power consumption of only 14.9 µW, drawn from a 1.2-V supply, this converter achieves a Schreier Figure-of-Merit (FoM_s) of 165.3 dB.

Specifications		**Design Choices and Results**
Input Signal Bandwidth	4 ÷ 8 kHz	**8 kHz**
SAR Bits		**5**
Oversampling Ratio		**32**
Sampling Frequency		**512 kHz**
Clock Frequency		**4.096 MHz**
Full-Scale		**600 mV_{pp}**
Supply Voltage	1.2 V	**1.2 V**
Resolution (ENOB)	12 ÷ 14 bits	**12.61 bits**
SNDR @ -36 dBFS (94 dBSPL)	40 ÷ 48 dBA	**38.7 dBA**
DR @ 0 dBFS (140 dBSPL)	76 ÷ 84 dBA	**78 dBA**
Core Power Consumption	≃ 10 µW	**14.9 µW**
Schreier Figure of Merit (FoM_s)		**165.3 dB**
Total Area		**380 µm x 340 µm = 0.129 mm^2**

$FoM_s = DR + 10 \cdot \log_{10}(^{BW}/_{Power})$

TABLE 4.1: Specifications, design choices and measurement results comparison.

	This Work	ISSCC 20 [46]	ISOCC 23 [47]	TCAS II 22 [48]	ISSCC 18 [49]	JSSC 19 [50]	SSCL 20 [51]	JSSC 19 [52]	JSSC 18 [53]
Technology [nm]	**BCD 65**	CMOS 110	CMOS 180	CMOS 65	CMOS 130	CMOS 65	CMOS 130	CMOS 40	CMOS 40
Architecture	**NS-SAR**	SD-CT	SD-DT	SD-DT	SD-DT	IADC	VCO	NS-SAR	NS-SAR
Supply [V]	**1.2**	1	1.8	1	1.2	1.2	1.2	1.1	1.1
Area [mm^2]	**0.129**	0.078	0.540	0.040	0.900	0.130	0.040	0.04	0.024
Bandwidth [kHz]	**8**	10	25	19.5	7	20	20	262	625
OSR	**32**	64	64	256	25	-	60	16	8
Power Consumption [µW]	**14.9**	6.5	851	43.5	4.4	550	240	143	84
Dynamic Range [dB]	**78**	81	89.9	91.7	54	101.8	97	79.8	80.5
ENOB	**12.61**	13.12	14.67	14.93	8.68	16.63	15.81	12.7	13
FoM_s [dB]	**165.3**	172.8	164	178.2	154.4	177.4	176	171	178

$FoM_s = DR + 10 \cdot \log_{10}(^{BW}/_{Power})$

TABLE 4.2: Proposed ADC performance summary and comparison with audio-band converters state-of-the-art.

The performance of the ADC are summarized in Tab. 4.2 and compared with other recent audio-band converters with similar features. Among these ADCs, the proposed quasi-passive error-feedback topology achieves the optimal trade off between power consumption and area occupation that are the two key aspects for AAD applications. Its performance is further strengthened by the insensitivity of the residue amplifier design to process, voltage and temperature, which ensures stable and repeatable operation across the full industrial temperature range ($-40\,^{\circ}C$ to $80\,^{\circ}C$) and across device-to-device variations. The degradation of SNDR is primarily attributable to the layout decisions adopted to mitigate parasitic effects, rather than to the single-ended architecture itself. As discussed in Chapter 2, an asymmetric routing strategy was implemented in order to prevent a more pronounced degradation of resolution. During experimental measurements, this design choice manifested itself as an increase in distortion, which consequently led to an unavoidable deterioration of the overall SNDR performance.

In conclusion, the proposed hybrid error-feedback architecture has the potential to serve as a foundation for subsequent advancements in precision data-converter design. When integrated with mismatch mitigation strategies for capacitive DACs, such as Dynamic Element Matching (DEM) or Data-Weighted Averaging (DWA), this framework could achieve even higher effective resolution, albeit with an associated increase in power consumption. Moreover, this combined approach may open additional research paths, including the exploration of adaptive calibration schemes or architecture-level optimizations that can balance resolution and energy efficiency.

Appendix A

SAR Logic Verilog Code

```
module SAR_Logic (DUTYSEL0, DUTYSEL1, B1, B2, B3, B4, B5, AMP_DIS,
    EOC, AMP_EN, M1NEG, M1NEG_n, M1POS, M1POS_n, M2NEG, M2NEG_n,
    M2POS, M2POS_n, M3NEG, M3NEG_n, M3POS, M3POS_n, M4NEG, M4NEG_n,
    M4POS, M4POS_n, M5NEG, M5NEG_n, M5POS,
M5POS_n, CK, DVDD, DVSS, OUTCOMP, RESET);

  input CK;
  input RESET;
  input OUTCOMP;
  input DUTYSEL0;
  input DUTYSEL1;

  input DVDD;
  input DVSS;

  output B5;
  output B4;
  output B3;
  output B2;
  output B1;
  output EOC;
  output M5POS;
  output M5POS_n;
  output M5NEG;
  output M5NEG_n;
  output M4POS;
  output M4POS_n;
  output M4NEG;
  output M4NEG_n;
  output M3POS;
  output M3POS_n;
  output M3NEG;
  output M3NEG_n;
  output M2POS;
  output M2POS_n;
  output M2NEG;
  output M2NEG_n;
  output M1POS;
  output M1POS_n;
  output M1NEG;
  output M1NEG_n;
  output AMP_EN;
  output AMP_DIS;

  reg B5;
```

```
43    reg B4;
44    reg B3;
45    reg B2;
46    reg B1;
47    reg EOC;
48    reg M5POS;
49    reg M5POS_n;
50    reg M5NEG;
51    reg M5NEG_n;
52    reg M4POS;
53    reg M4POS_n;
54    reg M4NEG;
55    reg M4NEG_n;
56    reg M3POS;
57    reg M3POS_n;
58    reg M3NEG;
59    reg M3NEG_n;
60    reg M2POS;
61    reg M2POS_n;
62    reg M2NEG;
63    reg M2NEG_n;
64    reg M1POS;
65    reg M1POS_n;
66    reg M1NEG;
67    reg M1NEG_n;
68    reg ENABLE_3_8;
69    reg DISABLE_3_8;
70    reg ENABLE_4_8;
71    reg DISABLE_4_8;
72    reg [4:0] MASTER_COUNTER;
73    reg DUMMY;
74
75    reg AMP_EN;
76    reg AMP_DIS;
77
78  always @(posedge RESET or posedge CK)
79  begin
80    if (RESET)
81      begin
82        B5=0;
83        B4=0;
84        B3=0;
85        B2=0;
86        B1=0;
87        MASTER_COUNTER=0;
88        DUMMY=0;
89        EOC=1;
90        ENABLE_3_8=0;
91        DISABLE_3_8=1;
92
93        ENABLE_4_8=0;
94        DISABLE_4_8=1;
95
96        M5POS=0;
97        M5POS_n=1;
98
99        M5NEG=0;
```

```
100       M5NEG_n=1;
101
102       M4POS=0;
103       M4POS_n=1;
104
105       M4NEG=0;
106       M4NEG_n=1;
107
108       M3POS=0;
109       M3POS_n=1;
110
111       M3NEG=0;
112       M3NEG_n=1;
113
114       M2POS=0;
115       M2POS_n=1;
116
117       M2NEG=0;
118       M2NEG_n=1;
119
120       M1POS=0;
121       M1POS_n=1;
122
123       M1NEG=0;
124       M1NEG_n=1;
125     end
126   else
127     begin
128       case (MASTER_COUNTER)
129         0:  begin          //0 sampling
130             DUMMY=0;
131             EOC=1;
132             ENABLE_3_8=0;
133             DISABLE_3_8=1;
134
135             ENABLE_4_8=0;
136             DISABLE_4_8=1;
137
138             M5POS=0;
139             M5POS_n=1;
140
141             M5NEG=0;
142             M5NEG_n=1;
143
144             M4POS=0;
145             M4POS_n=1;
146
147             M4NEG=0;
148             M4NEG_n=1;
149
150             M3POS=0;
151             M3POS_n=1;
152
153             M3NEG=0;
154             M3NEG_n=1;
155
156             M2POS=0;
```

```
157             M2POS_n=1;
158
159             M2NEG=0;
160             M2NEG_n=1;
161
162             M1POS=0;
163             M1POS_n=1;
164
165             M1NEG=0;
166             M1NEG_n=1;
167
168             MASTER_COUNTER=MASTER_COUNTER+1;
169           end
170
171         1:  begin          //1 Residue transfer
172             EOC=0;
173             ENABLE_3_8=0;
174             DISABLE_3_8=1;
175
176             ENABLE_4_8=0;
177             DISABLE_4_8=1;
178
179             M5POS=0;
180             M5POS_n=1;
181
182             M5NEG=0;
183             M5NEG_n=1;
184
185             M4POS=0;
186             M4POS_n=1;
187
188             M4NEG=0;
189             M4NEG_n=1;
190
191             M3POS=0;
192             M3POS_n=1;
193
194             M3NEG=0;
195             M3NEG_n=1;
196
197             M2POS=0;
198             M2POS_n=1;
199
200             M2NEG=0;
201             M2NEG_n=1;
202
203             M1POS=0;
204             M1POS_n=1;
205
206             M1NEG=0;
207             M1NEG_n=1;
208
209             MASTER_COUNTER=MASTER_COUNTER+1;
210           end
211
212         2:  begin          //2 MSB guess (M5)
213             ENABLE_3_8=0;
```

```
214             DISABLE_3_8=1;
215
216             ENABLE_4_8=0;
217             DISABLE_4_8=1;
218
219             M5POS=1;
220             M5POS_n=0;
221
222             M5NEG=0;
223             M5NEG_n=1;
224
225             M4POS=0;
226             M4POS_n=1;
227
228             M4NEG=1;
229             M4NEG_n=0;
230
231             M3POS=0;
232             M3POS_n=1;
233
234             M3NEG=1;
235             M3NEG_n=0;
236
237             M2POS=0;
238             M2POS_n=1;
239
240             M2NEG=1;
241             M2NEG_n=0;
242
243             M1POS=0;
244             M1POS_n=1;
245
246             M1NEG=1;
247             M1NEG_n=0;
248
249             MASTER_COUNTER=MASTER_COUNTER+1;
250           end
251
252         3:  begin          //3 MSB confirm (M5), Bit#2 guess (M4)
253             ENABLE_3_8=0;
254             DISABLE_3_8=1;
255
256             ENABLE_4_8=0;
257             DISABLE_4_8=1;
258
259             if (OUTCOMP)
260               begin
261                 M5POS=0;
262                 M5POS_n=1;
263
264                 M5NEG=1;
265                 M5NEG_n=0;
266
267                 M4POS=1;
268                 M4POS_n=0;
269
270                 M4NEG=0;
```

```
271                 M4NEG_n=1;
272               end
273             else
274               begin
275                 M4POS=1;
276                 M4POS_n=0;
277
278                 M4NEG=0;
279                 M4NEG_n=1;
280               end
281
282             MASTER_COUNTER=MASTER_COUNTER+1;
283           end
284         4:  begin          //4 Bit#2 confirm (M4), Bit#3 guess (M3)
285             ENABLE_3_8=0;
286             DISABLE_3_8=1;
287
288             ENABLE_4_8=1;
289             DISABLE_4_8=0;
290
291             if (OUTCOMP)
292               begin
293                 M4POS=0;
294                 M4POS_n=1;
295
296                 M4NEG=1;
297                 M4NEG_n=0;
298
299                 M3POS=1;
300                 M3POS_n=0;
301
302                 M3NEG=0;
303                 M3NEG_n=1;
304               end
305             else
306               begin
307                 M3POS=1;
308                 M3POS_n=0;
309
310                 M3NEG=0;
311                 M3NEG_n=1;
312               end
313
314             MASTER_COUNTER=MASTER_COUNTER+1;
315           end
316         5:  begin          //5 Bit#3 confirm (M3), Bit#4 guess (M4)
317             ENABLE_3_8=1;
318             DISABLE_3_8=0;
319
320             ENABLE_4_8=1;
321             DISABLE_4_8=0;
322
323             if (OUTCOMP)
324               begin
325                 M3POS=0;
326                 M3POS_n=1;
327
```

```
328                 M3NEG=1;
329                 M3NEG_n=0;
330
331                 M2POS=1;
332                 M2POS_n=0;
333
334                 M2NEG=0;
335                 M2NEG_n=1;
336               end
337             else
338               begin
339                 M2POS=1;
340                 M2POS_n=0;
341
342                 M2NEG=0;
343                 M2NEG_n=1;
344               end
345
346             MASTER_COUNTER=MASTER_COUNTER+1;
347           end
348         6:  begin          //6 Bit#4 confirm (M2), Bit#5 guess (M1)
349             ENABLE_3_8=1;
350             DISABLE_3_8=0;
351
352             ENABLE_4_8=1;
353             DISABLE_4_8=0;
354
355             if (OUTCOMP)
356               begin
357                 M2POS=0;
358                 M2POS_n=1;
359
360                 M2NEG=1;
361                 M2NEG_n=0;
362
363                 M1POS=1;
364                 M1POS_n=0;
365
366                 M1NEG=0;
367                 M1NEG_n=1;
368               end
369             else
370               begin
371                 M1POS=1;
372                 M1POS_n=0;
373
374                 M1NEG=0;
375                 M1NEG_n=1;
376               end
377
378             MASTER_COUNTER=MASTER_COUNTER+1;
379           end
380         7:  begin          //7 Bit#5 confirm, Output creation
381             ENABLE_3_8=1;
382             DISABLE_3_8=0;
383
384             ENABLE_4_8=1;
```

```
385             DISABLE_4_8=0;
386
387             if (OUTCOMP)
388               begin
389                 M1POS=0;
390                 M1POS_n=1;
391
392                 M1NEG=1;
393                 M1NEG_n=0;
394
395                 B5=M5POS;
396                 B4=M4POS;
397                 B3=M3POS;
398                 B2=M2POS;
399                 B1=M1POS;
400               end
401             else
402               begin
403                 B5=M5POS;
404                 B4=M4POS;
405                 B3=M3POS;
406                 B2=M2POS;
407                 B1=M1POS;
408               end
409
410             MASTER_COUNTER=0;
411           end
412
413         default: begin
414                DUMMY=1;
415              end
416       endcase
417     end
418   end
419
420 always@(RESET, DUTYSEL0, DUTYSEL1, ENABLE_3_8, DISABLE_3_8,
    ENABLE_4_8, DISABLE_4_8)
421   begin
422     if (RESET)
423       begin
424         AMP_EN=0;
425         AMP_DIS=1;
426       end
427     else if ((!DUTYSEL0) && (!DUTYSEL1))
428       begin
429         AMP_EN=0;
430         AMP_DIS=1;
431       end
432     else if ((DUTYSEL0) && (!DUTYSEL1))
433       begin
434         AMP_EN=ENABLE_3_8;
435         AMP_DIS=DISABLE_3_8;
436       end
437     else if ((!DUTYSEL0) && (DUTYSEL1))
438       begin
439         AMP_EN=ENABLE_4_8;
440         AMP_DIS=DISABLE_4_8;
```

```
441       end
442     else if ((DUTYSEL0) && (DUTYSEL1))
443       begin
444         AMP_EN=1;
445         AMP_DIS=0;
446       end
447   end
448 endmodule
```

Appendix B

Pin List

Pin Name	Pin n°	Pin Description	Pin Type	Power domain
NC	1	Not connected	/	/
IBCM	2	Common mode buffer bias current	Input current	BV_{DD} (1.2 V)
BVDD	3	Buffer V_{DD}	Power	BV_{DD} (1.2 V)
MUXSEL2	4	Multiplexer selection bit	Digital input voltage	DV_{DD} (1.2 V)
MUXSEL1	5	Multiplexer selection bit	Digital input voltage	DV_{DD} (1.2 V)
MUXSEL0	6	Multiplexer selection bit	Digital input voltage	DV_{DD} (1.2 V)
DVSS	7	Digital GND	GND	DV_{DD} (1.2 V)
DVDD	8	Digital V_{DD}	Power	DV_{DD} (1.2 V)
INBUFFBYP	9	Input buffer bypass enable signal	Digital input voltage	DV_{DD} (1.2 V)
REFBUFMODE	10	References buffers bypass selection bit	Digital input voltage	DV_{DD} (1.2 V)
DUTYSEL1	11	Amplifier duty-cycle selection bit	Digital input voltage	DV_{DD} (1.2 V)
NC	12	Not connected	/	/
DUTYSEL0	13	Amplifier duty-cycle selection bit	Digital input voltage	DV_{DD} (1.2 V)
TMOS3	14	Amplifier MOS trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
TMOS2	15	Amplifier MOS trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
TMOS1	16	Amplifier MOS trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
TMOS0	17	Amplifier MOS trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
RESET	18	Reset signal	Digital input voltage	DV_{DD} (1.2 V)
TRES1	19	Amplifier resistors trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
TRES0	20	Amplifier resistors trimming selection bit	Digital input voltage	DV_{DD} (1.2 V)
CK	21	Clock signal	Digital input voltage	DV_{DD} (1.2 V)
EOC	22	End Of Conversion signal	Digital output voltage	DV_{DD} (1.2 V)
NC	23	Not connected	/	/
B5	24	Output signal bus	Digital output voltage	DV_{DD} (1.2 V)
B4	25	Output signal bus	Digital output voltage	DV_{DD} (1.2 V)
B3	26	Output signal bus	Digital output voltage	DV_{DD} (1.2 V)
B2	27	Output signal bus	Digital output voltage	DV_{DD} (1.2 V)
B1	28	Output signal bus	Digital output voltage	DV_{DD} (1.2 V)
AVDD	29	Analog V_{DD}	Power	AV_{DD} (1.2 V)
INBUFMODE	30	Input buffer enable signal	Digital input voltage	V_{DDIO} (1.8 V)
IBIN	31	Input buffer bias current	Input current	V_{DDIO} (1.8 V)
VDDIO	32	Input buffer V_{DD}	Power	V_{DDIO} (1.8 V)
AVSS	33	Analog GND	GND	AV_{DD} (1.2 V)
NC	34	Not connected	/	/
VINBYP	35	Input buffer bypass input signal	Analog Input Voltage	AV_{DD} (1.2 V)
VIN	36	Input signal	Analog Input Voltage	AV_{DD} (1.2 V)
MUXOUT	37	Multiplexer output	Mixed signal	AV_{DD} (1.2 V)
ICOMP	38	Comparator bias current	Input current	AV_{DD} (1.2 V)
AVSS	39	Analog GND	GND	AV_{DD} (1.2 V)
VREFP	40	Positive reference voltage	Analog Input Voltage	BV_{DD} (1.2 V)
VREFN	41	Negative reference voltage	Analog Input Voltage	BV_{DD} (1.2 V)
VCM	42	Common mode voltage	Analog Input Voltage	BV_{DD} (1.2 V)
IBP	43	Positive reference buffer bias current	Input current	BV_{DD} (1.2 V)
IBN	44	Negative reference buffer bias current	Input current	BV_{DD} (1.2 V)

TABLE B.1: Detailed pin list of the *MKI* testchip.

Appendix C

Truth Tables

MUXSEL2	MUXSEL1	MUXSEL0	MUXOUT	Output Connection Description
0	0	0	Do Nothing	Not connected
0	0	1	V_{out_comp}	Comparator output voltage
0	1	0	V_{refp}	Positive reference voltage supply
0	1	1	V_{cm}	Common-mode reference voltage supply
1	0	0	V_{refp}	Negative reference voltage supply
1	0	1	ϕ_{EN}	Amplifier enable phase
1	1	0	ϕ_{A1}	Loop filter ϕ_{A1} phase
1	1	1	ϕ_{B1}	Loop filter ϕ_{A1} phase

TABLE C.1: Truth table of the multiplexer for DFT functionality.

DUTYSEL1	DUTYSEL0	Residue Amplifier Duty-cycle	Duty-cycle Description
0	0	0%	Amplifier always disabled
0	1	37.5%	Amplifier enabled 3 clock periods out of 8
1	0	50%	Amplifier enabled 4 clock periods out of 8
1	1	100%	Amplifier always disabled

TABLE C.2: Truth table of the residue amplifier duty-cycle.

TMOS3	TMOS2	TMOS1	TMOS0	M_{B7} number of fingers
0	0	0	0	72
0	0	0	1	73
0	0	1	0	74
0	0	1	1	75
0	1	0	0	76
0	1	0	1	77
0	1	1	0	78
0	1	1	1	79
1	0	0	0	80
1	0	0	1	81
1	0	1	0	82
1	0	1	1	83
1	1	0	0	84
1	1	0	1	85
1	1	1	0	86
1	1	1	1	87

TABLE C.3: Truth table of the trimming transistor M_{B7} for the residue amplifier tail current I_{B2}.

TRES1	**TRES0**	**Number of Unitary R_u Segments**	**R_B Value [kΩ]**
0	0	8	8
0	1	16	16
1	0	16	16
1	1	24	24

TABLE C.4: Truth table of the trimming resistor R_B for the cascode voltage of the amplifier V_B.

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List of Abbreviations

AAD	**A**udio **A**ctivity **D**etection
ADC	**A**nalog-to-**D**igital **C**onverter
AFE	**A**nalog **F**ront-**E**nd
AR	**A**ugmented **R**eality
ASR	**A**utomatic **S**peech **R**ecognition
A/D	**A**nalog to **D**igital
BCD	**B**ipolar **C**MOS **D**MOS
BJT	**B**ipolar **J**unction **T**ransistor
BNC	**B**ayonett **N**eill-**C**oncelman
BW	**B**and**W**idth
CDAC	**C**apacitive **D**igital-to-**A**nalog **C**onverter
CK	**C**loc**K**
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CTAT	**C**omplementary-**T**o-**A**bsolute-**T**emperature
DAC	**D**igital-to-**A**nalog **C**onverter
DEM	**D**ynamic **E**lement **M**atching
DFT	**D**esign **F**or **T**estability
DIP	**D**ual **I**n-line **P**ackage
DRC	**D**esign **R**ule **C**hecking
DSP	**D**igital **S**ignal **P**rocessing
DR	**D**ynamic **R**ange
DUT	**D**evice **U**nder **T**est
DWA	**D**ata **W**eighted **A**veraging
EF	**E**rror-**F**eedback
EMC	**E**lectro-**M**agnetic **C**ompatibility
ENOB	**E**ffective **N**umber **O**f **B**its
EOC	**E**nd **O**f **C**onversion
FIR	**F**inite **I**mpulse **R**esponse
FF	**F**eed-**F**orward
FFT	**F**ast **F**ourier **T**ransform
FoM	**F**igure **o**f **M**erit
FS	**F**ull-**S**cale
GBW	**G**ain **B**and**W**idth product
HMD	**H**ead **M**ounted **D**isplay
JLCC	**J**-**L**eades **C**hip **C**arrier
IC	**I**ntegrated **C**ircuit
IIR	**I**nfinite **I**mpulse **R**esponse
INL	**I**ntegral **N**on**L**inearity
I/O	**I**nput/**O**utput
IoT	**I**nternet **o**f **T**hings
IRN	**I**nput **R**eferred **N**oise
LF	**L**oop-**F**ilter

LDE	**L**ayout **D**ependent **E**ffect
LDO	**L**ow **D**rop **O**ut
LSB	**L**east **S**ignificant **B**it
LVS	**L**ayout **V**ersus **S**chematic
MEMS	**M**icro-**E**lectro-**M**echanical **S**ystem
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
MSB	**M**ost **S**ignificant **B**it
NN	**N**eural **N**etwork
NS	**N**oise **S**haping
NTF	**N**oise **T**ransfer **F**unction
OSR	**O**ver**S**ampling **R**atio
PA	**P**re**A**mplifier
PCB	**P**rinted **C**ircuit **B**oard
PM	**P**hase **M**argin
PSD	**P**ower **S**pectral **D**ensity
PSRR	**P**ower **S**upply **R**ejection **R**atio
PTAT	**P**roportional-**T**o-**A**bsolute-**T**emperature
PVT	**P**rocess **V**oltage **T**emperature
QP	**Q**uasi-**P**assive
RA	**R**esidue **A**mplifier
REF	**REF**erence
RFID	**R**adio-**F**requency **ID**entification
RMS	**R**oot **M**ean **S**quare
SAR	**S**uccessive **A**pproximation **R**egister
SFF	**S**ingle **F**requency **F**iltering
SFS	**S**equential **F**requency **S**canning
SMD	**S**urface **M**ounted **D**evice
SNDR	**S**ignal to **N**oise and **D**istortion **R**atio
SNR	**S**ignal to **N**oise **R**atio
SQNR	**S**ignal to **Q**uantization-**N**oise **R**atio
SotA	**S**tate **O**f **T**he **A**rt
STF	**S**ignal **T**ransfer **F**unction
S/H	**S**ample and **H**old
THD	**T**otal **H**armonic **D**istortion
THD+N	**T**otal **H**armonic **D**istortion + **N**oise
THT	**T**hrough **H**ole **T**echnology
TWS	**T**rue **W**ireless **S**tereo
VAD	**V**oice **A**ctivity **D**etection
VR	**V**irtual **R**eality
ZCR	**Z**ero **C**rossing **R**ate

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I A. Gemelli, **M. Tambussi**, S. Fusetto, A. Aprile, E. Moisello, E. Bonizzoni, and P. Malcovati, "Recent Trends in Structures and Interfaces of MEMS Transducers for Audio Applications: A Review," Micromachines, vol. 14, no. 4, 2023, ISSN: 2072-666X, DOI: 10.3390/mi14040847.

II **M. Tambussi**, M. Grassi, E. Bonizzoni, and P. Malcovati, "Trade-offs in Active and Passive NS-SAR ADCs Architectures for Ultra-Low Power Audio Activity Detection Applications," in 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2023, pp. 165–168. DOI: 10.1109/PRIME58259.2023.10161952.

III **M. Tambussi**, M. Grassi, E. Bonizzoni e P. Malcovati, "A/D Converter Architectures for Always-On AAD Applications", in Atti della Riunione Annuale GMEE, Bologna, Italy, set. 2023, pp. 417–418.

IV **M. Tambussi**, M. Grassi, G. Rocca, S. Valle, M. Grandi, E. Bonizzoni, and P. Malcovati, "A 14.9-µW Quasi-Passive Error-Feedback Noise-Shaping SAR Converter with 78-dB Dynamic Range for Audio Activity Detection," in 2025 IEEE International Symposium on Circuits and Systems (ISCAS), 2025, pp. 1-5, DOI: 10.1109/ISCAS56072.2025.11043999.

V **M. Tambussi**, M. Grassi, G. Rocca, S. Valle, M. Grandi, E. Bonizzoni, and P. Malcovati, "A Quasi-Passive 78-dB DR 14.9-µW Noise-Shaping SAR A/D Converter for Audio Activity Detection Applications," IEEE Transactions on Circuits and Systems II: Express Briefs, pp. 1-1, DOI: 10.1109/TCSII.2025.3590625.

VI **M. Tambussi**, M. Grassi, E. Bonizzoni e P. Malcovati, "Characterization of a Low-Power Quasi-Passive Error-Feedback Noise-Shaping SAR ADC For Always-On Audio Activity Detection", in Atti della Riunione Annuale GMEE, Napoli, Italy, set. 2025, pp. 419-420.