UNIVERSITÀ DEGLI STUDI DI PAVIA

FACOLTÀ DI INGEGNERIA

Dipartimento di Ingegneria Industriale e dell'Informazione

Doctoral Thesis in Microelectronics
CICLO: XXXV

Mach-Zehnder Modulator Driver Designs in 28 nm CMOS Technology for Coherent Optical Systems

Supervisor:
Chiar.mo Prof. Danilo Manstretta

Coordinator:
Chiar.mo Prof. Piero Malcovati

Ph.D. Dissertation of
Nicola Cordioli

February 2023

Declaration of Authorship

I, Nicola Cordioli, declare that this thesis titled *Mach-Zehnder Modulator Driver Designs in 28 nm CMOS Technology for Coherent Optical Systems*, and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed: Nicola Cordioli

Date: 13/02/2023

UNIVERSITÀ DEGLI STUDI DI PAVIA

Abstract

Facoltà di Ingegneria

Dipartimento di Ingegneria Industriale e dell'Informazione

Mach-Zehnder Modulator Driver Designs in 28 nm CMOS Technology for Coherent Optical Systems

by Nicola Cordioli

Since the beginning of the Internet, the number of connected devices has experienced an exponential growth. While increasing in users number, also an huge amount of services and applications have been made available through the network. The forecasts tell us that we are still at the beginning of this journey, even if the numbers are already hard to catch. In order to satisfy these demands, always more capable networks have been developed. Optical links have been proven to be the best candidates for long reach backbone connections, given the low losses introduced. The final target of a link is to deliver the highest amount of signals for a given bit error rate (BER). So, coherent modulations move towards this direction, providing better spectral efficiency compared with other schemes. Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) can be exploited, but linearity and phase become crucial both for the electrical and optical design. Electro-optical modulators (EOM) are used to combine laser beams with different amplitudes and phases to provide such complex schemes. CMOS technology is not so widely spread through coherent applications, mainly because of the higher break-down voltage and g_m/I_D of BiCMOS devices. Yet CMOS has some interesting features, such as scalability and integration between analog and digital circuits, that might result in a reduction on the overall system costs. Furthermore in the latest technology knots, p- and n-type MOS transistors have very similar performance, making available complementary structures which can compensate for the poor MOS transconductance efficiency. The required electrical signal at the EOM input should be large enough to fully steer the light phase, linear to preserve phase and amplitude, and broad-band to achieve the highest bit rate. This thesis reports two CMOS designs. A first driver has been designed, fabricated and tested. The proposed structure is a four stages chain, with two

gain blocks, a pre-driver and a main driver. To reach good linearity, cascoded pseudo-differential structures have been implemented, apart for the pre-driver. The cascode transistor allows to bias the common source (CS) in triode region, resulting in a linear voltage-to-current conversion. Working in triode region means a lower transistor efficiency, and a stronger relation between transconductance and biasing. In this way gain variability can be introduced relying on the g_m dependency by the drain-to-source voltage. The pre-driver is a pn source follower, which feeds the main driver without impairing the gain at high frequency. This solution is capable to provide 1.5 $V_{pp\text{-}diff}$, with a total harmonic distortion (THD) lower than 1.8%. The gain variation over frequency is always below 3 dB up to 58 GHz.
A second design has been realized and sent for fabrication, but at the moment of this dissertation not yet available. The first stage of this design is a transconductor, which provides a first voltage-to-current conversion, since the amplitude involved is small, the amount of distortion introduced (which is proportional to the voltage swing) is very poor. Part of the gain is provided in current domain through a current mirror-like structure, allowing, at least in principle, self cancellation of spurious components. Then, the output current-to-voltage conversion is realized over a closed-loop transimpedance amplifier (TIA). This solution intend to exploit loop gain (G_{loop}) in order to reduce the distortion. At the same time, a loop designed with a phase margin (PM) lower than 60°, results in high frequency peak for the closed-loop transfer function. The simulated THD for 1.5 $V_{pp\text{-}diff}$ is frequency dependent, and it ranges from 0.3% at 1 GHz, up to 2% at 9 GHz. Fluctuations in the transfer function are below 3 dB up to 51 GHz, for all the gain configurations.
Not many CMOS works can be found in literature, making these two works a proof that this technology is viable even in terms of performance.

Acknowledgments

A special thanks to professor Danilo Manstretta and professor Rinaldo Castello for the chance of being part of this PhD program and for the helps during these years.

An acknowledgment to Huawei for the partnership in this project. A special thanks to all the Milano Huawei R&D guys, who taught me a lot during these years.

Thanks to all the new people met during this journey, who became friends.

Thanks to my special family, who never lets me down.

Thanks to each one of you, who meant, means and will mean something important to me. I am grateful to have you in my life.

Contents

List of Figures

List of Tables

Introduction

Forecasts say that in the upcoming years (up to 2023) nearly 5.3 billion of people will have Internet access. In average, each person, will connect to the network 3.6 devices. An important share of these numbers will be the growth of Machine-to-Machine (M2M) connections, which will cover half of the global connections. Within this category, also referred as Internet of Things (IoT), connected home applications will have the largest share, while connected car applications will be the fastest to grown up. Together with the growing number of on-line devices, networks performance are expected to improve. The average mobile connection speed will reach 43.9 Mbps, while for the fresh 5G the data rate will hit 575 Mbps [1]. Taking into account these growing broadband requirements of individuals, homes and enterprises, fiber networks are expected to deliver to these users 10-gigabit connections. To get this possible, future access network and backbone equipments will need to support terabit-level interfaces. Especially the second one will support from 40 to 100 Tbit/s. Terabit-level speed will also interest many other parts of the network besides the backbone, as data center. So far 200G and 400G Ethernet connections are already available, but to cope with the previous requirement, interface technology that support speeds of 800 Gbit/s or even 1.6 Tbit/s has to be standardized. Two ways are under investigation, pluggable optics modules and co-packaged optics (CPO). Both of them will have place into this market, but the CPO is preferable because of the power and density issues of the pluggable solutions. Furthermore, the demand of long-distance transmission capacity of more than 100 Tbit/s per fiber will push the development of wavelength division multiplexing (WDM) equipments and newer high-baud rate electro-optic modulation schemes. For both backbone and home connections, coherent detection technology will be used. This will significantly improve the receiver sensitivity, while supporting modulation formats with higher spectral rates. More complex schemes as quadrature shift keying (QPSK) and m-quadrature amplitude modulation (m-QAM), will be available, in order to achieve higher data rates [2].

Design of electrical and optical components are no more stand alone process. For short-reach applications, as data center networks, silicon photonics (SiPh) solutions are already available [3]. The availability of always more scaled and aggressive silicon technology, allows to acquire very high-speed electrical signal. This enables digital signal process (DSP) cores to equalize linear transmission impairments. CMOS and FinFET give the chance of integrating on the same die both the acquisition and processing function, lowering the system costs. Optical links are proving to be the proper infrastructure, capable to bear and even to push this massive demand of connections between devices, machines and people.

The next pages will be organized as described:

In **Chapter 1:** an overview of an optical communication link is reported, and why coherent applications are moving a lot of interests. To get familiar with the topic optical components as EOMs, fibers and photodiodes are introduced. Theory about coherent transmission and detection are reported, together with the most used modulation schemes. Then the focus is moved on the silicon world, introducing transmitter and receiver, and what they are supposed to do. The electrical specifications required to these devices are highlighted, with a brief dissertation on why CMOS has been preferred against the commonly exploited BiCMOS.

In **Chapter 2:** a linear Mach-Zenhder modulator driver is presented. This work has been fabricated and electrically fully characterized. A four stages cascade compose the transmission chain, the first two of them provide most of the gain, while the last two are designed for bandwidth and linearity purposes. To improve the linearity of each stage, the transistor triode region has been exploited. A continuous 10 dB gain variation is provided, moving the MOS among the triode biasing. The resulting THD is always lower than 1.8 % at 1.5 $V_{pp\text{-}diff}$, and it is reduced for larger input amplitude. The -3 dB electrical bandwidth reach 58 GHz, and resonant networks have been introduced to extend it. The overall power consumption is 297 mW.

In **Chapter 3:** a second linear modulator driver is presented. This chapter reports post-layout simulations, because the chip fabrication is on going. The design is mostly based on closed-loop circuits. An input voltage-to-current conversion is realized through a transconductor, then part of the gain in realized in the current domain, with a current mirror-like solution. The output current-to-

voltage conversion is realized by a closed-loop TIA, so over a resistor which is linear in principle. Designing loops with a phase margin lower than 60° results in high frequency peaking for the closed-loop transfer function. The distortion now is frequency dependent, and ranges from 0.3% at 1 GHz, to 2.1% at 9 GHz. The power consumption is 235 mW, while the -3 dB bandwidth is 52 GHz.

Chapter 1

Introduction of Optical Communications

Abstract
Through the years fibers have been preferred to coaxial cables when it comes to transport high-speed and large volumes of data. By the way, low losses and large bandwidth are not enough to stand the ever growing demand for always more capable link. Spectral efficiency has became a key parameter in the last decade, introducing the need of always more complex modulation schemes. This chapter deals with an introduction to optical systems, describing the main building blocks and how they works. Advantages and requirements of coherent detection are introduced. Transmitter and receiver electrical features are described, with the required performance. To conclude, some usual transistor level solutions with benefits and drawbacks are presented.

1.1 Optical Links

1.1.1 A brief introduction

The reasons behind the widespread use of optical communication for high-speed data, should be found on the large bandwidth and the poor losses provided by optical fiber. To make a comparison, at 1 GHz, coaxial cable losses can reach 500 dB/km, while fiber attenuation at 50 GHz is 0.2 dB/km. Considering also wireless communications, for carriers around GHz the losses per meter reach several decibels, with 100 Mb/s as data rates. The large available free bandwidth, allows to cast several channels over different wavelengths (frequencies), on the same physical mean. Historically, this has started the Tb/s data rate

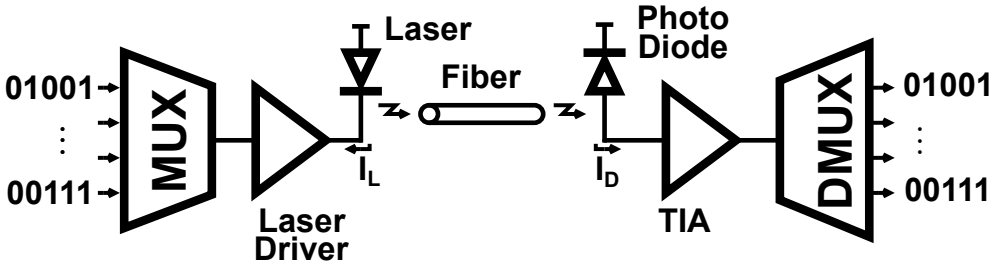


FIGURE 1.1: Simplified communication optical system.

era. This can easily clear up why when it comes to long reach communication links (e.g. the internet traffic between Europe and the United States), there is no better solution than exploiting the light. Theory in the next sections are inspired by [4].

1.1.2 Optical systems

Figure 1.1 shows a very simplified optical system. The communication starts with a multiplexer (MUX), which serialize the parallel bit streams coming from a DSP. A driver takes the bit stream, and it feeds the electro-optical transducer with the right power level. The transducer (e.g. a laser) converts the electrical power into optical form (e.g. light on for logical ONEs and light off for ZEROs), making the data suitable to travel through the fiber. On the receiver side, light is back converted into current through a photodetector (e.g. a photodiode). A TIA turns this current into voltage, allowing the demultiplexer (DEMUX) to restore the parallel bit streams. The system in Figure 1.1 is still far away from a proper optical link, but it introduces enough elements to get familiar with the topic and for the purpose of this dissertation. Through the years, the introduced blocks have changed a lot, because of newer technologies, architectures and requirements in both the electrical and optical fields, but still the overall system can be represented as Figure 1.1. The next sections will deal briefly with lasers, photo-diodes and fibers, then the focus is moved to the electrical part.

1.1.3 Laser diodes

A laser is an electro-optical transducer, based on semiconductor material, capable to turn electrical signal into light. The spectrum of this light is very sharp, it means that the energy provided is heavily concentrated around one frequency. Furthermore, the beam produced is very focused on space, so it can travel for long distance without scattering or spreading. It is composed by *pn*

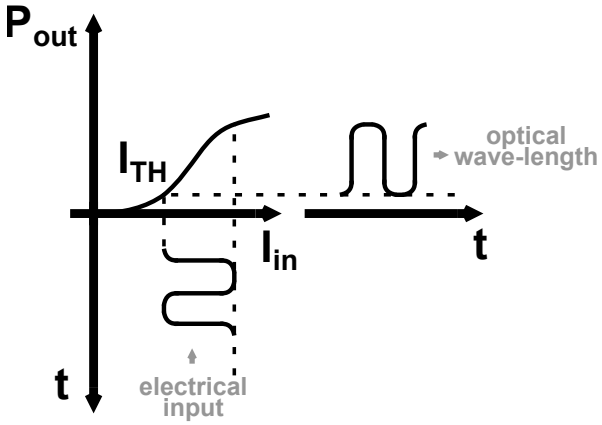
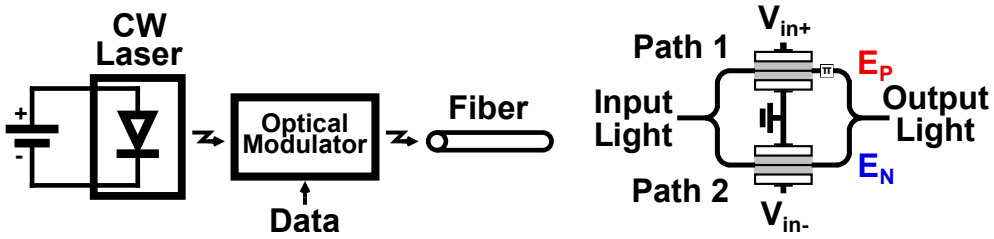


FIGURE 1.2: Laser diode input-output characteristic.

junction and mirrors. While current flows through the junction, electrons jump from conduction to valence band, releasing energy as photons. Mirrors and lens create an *oscillation* which is responsible of the spectrum sharpness. The input-output laser characteristic is reported in Figure 1.2. I_{TH} is the threshold current, and while the current is below this value no output power is generated. Exceeding I_{TH}, the output power changes almost linearly with the input current, up to the saturation level. The more efficient the laser, the lower is the current required for the same amount of output power. The *quantum efficiency* is given by the ration of the output photons and the input electrons, for a given time interval. So this defines the required input power to provide a given optical power. As told, in principle a laser generates a single wave-length, so a perfect monochromatic light. Actually, the light spectrum contains side modes, which lead to other issues while propagating through the fiber. I_{TH} is a biasing current, so no information is carried by this current. Lowering as much as possible this current means increasing the efficiency. Furthermore, moving in this direction, also the ratio between high and low output power is increased, making the detection between ONEs and ZEROs easier. Voltage drop across the device is defined by the threshold current and the signal current, ranging from 1.5 to 3 V. This means that high supply voltages are required, making the transistor breakdown voltage an issues. Fiber attenuations and receiver sensitivity defines the required output power from the laser. To provide high power level, the semiconductor area is increased, introducing higher input parasitic capacitance, lowering the speed.



(a) External laser modulation. (b) Mach-Zehnder modulator.

FIGURE 1.3: Optical communication system with an external optical modulator.

1.1.4 Electro-optical modulator (EOM)

Laser diode has several limits as turn-on delay, relaxation oscillation, frequency chirping. This dissertation does not deal with such phenomena because more related to the physic of the device. Nonetheless, given these non idealities, directly driving the laser results in limitations for data rate and fiber length. For high-speed applications is common to have a continuous source of light provided by a laser, which can be considered as the *carrier*, while an external modulator provides the information as shown in Figure 1.3a. This kind of devices are also called interferometer, because through them an electrical signal can *interfere* with light. For our purposes the EOM used is a Mach-Zehnder Modulator (MZM). In this device the propagation velocity depends by the applied field across it. This allows light phase shifting based on the electrical signal applied. As shown in Figure 1.3b the same source of light can be splitted in different paths which experience different phase shifts. Recombining them together, the output amplitude will depend by the delay, and so a function of the electrical signal. This allows to exploit complex modulation as m-QAM and m-QPSK. V_π is the voltage required by the MZM to introduce 180° of phase shift. This value trades with the device length, increasing it will reduce the V_π. At the same time, a wider MZM will introduce higher parasitic capacitance limiting the speed. So to define the electrical requirements is mandatory to know the modulator involved. Figure 1.4 shows how to proper bias Figure 1.3b to obtain a phase shift keying modulation from a driver V_{RF} signal. V_{RF} is equal to the difference between V_{in+} and V_{in-} from Figure 1.3b. To provide the PSK modulation, the MZM should be biased at the null bias point (N). The two optical paths are affected by signals with the same magnitude but opposite phases, this enables the phase modulation of the optical field. V_{RF} is a NRZ driving signal. With a common mode signal as V_{RF} means that E_P

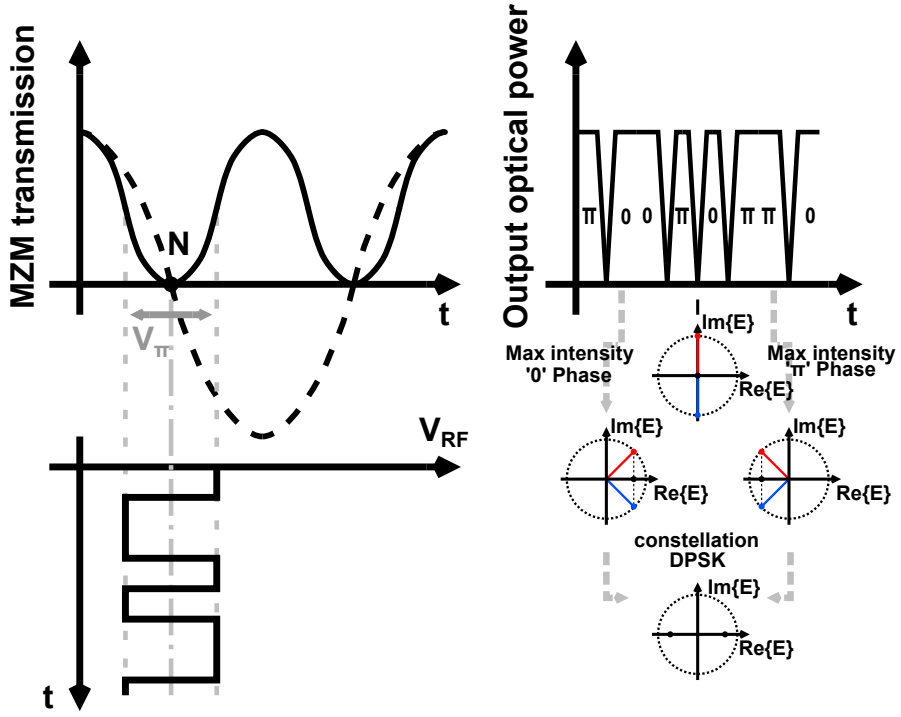


FIGURE 1.4: PSK modulated signal from a V_{RF} one.

and E_N experiences the same phase shift, resulting with opposite phases at the combiner, yielding a zero output optical power. While, when a differential signal representing a logic ONE is applied as V_{RF}, the phase shifts of E_P and E_N would be in opposite directions, meaning a non-zero optical signal and a point on the real axis of the constellation map. A logic ZERO is represented by a V_{RF} with opposite phase, resulting in a output signal with the same magnitude as the ONE but with a π phase shift. For this modulation, ONEs and ZEROs have the same magnitude while a π phase shifted optical field. To further increase the spectral efficiency, the NRZ amplitude modulation can be substitute with a PAM-4 signal, making the constellation a 4-PSK [5]. Deeper analysis about modulations, constellations and spectral efficiency are available in the next sections.

1.1.5 Optical fibers

In optical systems, light travels through fibers. As introduced, for long reach communications, fibers are preferred to twisted and coaxial cables, because of

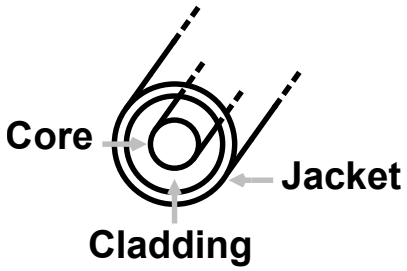


FIGURE 1.5: Fiber section.

their wider bandwidth and the lower attenuation. A section of a fiber is represented in Figure 1.5. The laser beam travels along the *core*, made by *silica* (a material derived by silicon dioxide), and it is confined there thanks to the *cladding*. The *jacket* works as shield, to protect the fiber. Core diameter ranges from 5 to 10 μm, a jacket can reach around 100 μm. The small dimension makes the alignment between fibers very hard, and results in poor stiffness. Losses introduced by fibers directly define the maximum distance between transmitter and receiver. Two kind of losses can be found. Absorptive losses, when the travelling wavelength excites atomic resonances in the fiber material or in the impurities. Radiative losses, when, because of the scattering, light exits the core radiating through the cladding. The higher cost and mechanical difficulties have pushed the development of different material than silica. *Plastic* materials as, *polymethylmethacrylate*, *polystyrene* and *polycarbonate* are used for fibers. These materials allow to have larger core diameter, solving stiffness and mechanical issues. One of the most important drawbacks are the higher losses introduced.

1.1.6 Photodiodes

Light or photons travelling through the fiber are converted into electrical signal by means of a photodiode. As the EOM for the transmission side, the photodiode defines some receiver electrical requirements as speed and sensitivity. Photons can be seen as packs of energy. These packs hitting the photodiode *pn* junction enable electrons to jump from the valence to the conduction band. Electrons and holes are formed in this way, and reverse biasing the diode a current flow can be generated. In Figure 1.6 it is highlighted that reverse biasing in the proper way the junction, the presence of light lets current flows.

The current generated, I_P, is proportionally linear with the optical power P_{OP}

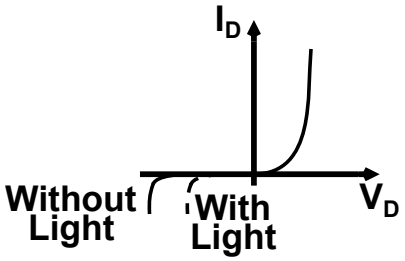


FIGURE 1.6: Voltage-current photodiode characteristic.

$$I_P = R_{PH} \times P_{OP}, \tag{1.1}$$

where R_{PH} is the diode *responsivity*. This value can be increased with wider junction, introducing higher parasitic capacitance. In the latest systems, to have higher performance, an optical amplifier is placed between the fiber and the photodiode.

1.2 Coherent Optical Applications

1.2.1 Coherent optical communication through the years

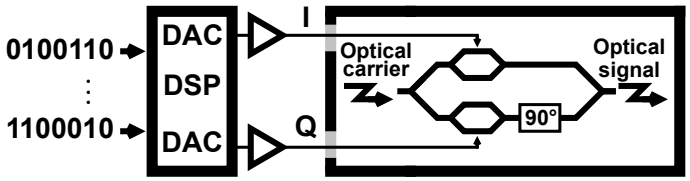
In optical communications, coherent solutions have always been considered for the receiver high sensitivity, so for the unrepeated transmission distance. The counterpart of this solution is the intensity-modulation and direct-detection (IM·DM), which attracted lots of interests during the '90, thanks to the high-capacity wavelength-division multiplexing (WDM). Digital carrier-phase estimation in coherent receivers, has moved back interest for coherent applications in the last fifteen years. Such an interest is manly due because of the possibilities of exploiting m-PSK and m-QAM, meaning an increased spectral efficiency compared with IM·DM. Coherent detection allows to preserve phase information after detection, so linear transmission impairments, as group-velocity dispersion (GVD) and polarization-mode dispersion (PMD), can be equalized thanks to DSP. Coherent detection assisted with high-speed DSP, together with WDM channels with 50 GHz spaced grids, prove a capability up to 8.8 Tb/s through a single fiber. The request for the coming years, are bit rates close to 400 Gb/s per WDM channel. The next sections will follow [6].

1.2.2 Coherent and IM·DD

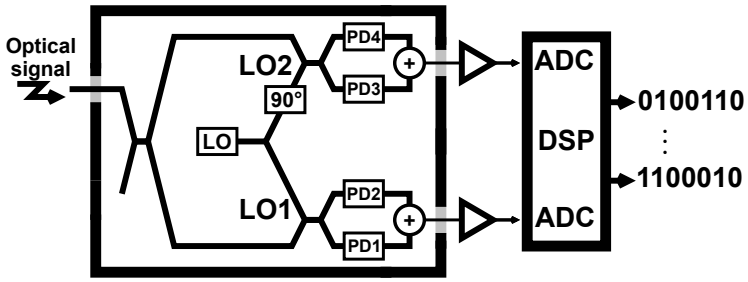
IM·DD is a widely employed optical communication scheme. It is based on the intensity modulation of a semiconductor laser, transmitted through an optical fiber then detected by a square-law detector. Since the detection relies on the received amplitude, carrier phase and state of polarization (SOP) of the light does not affect the sensitivity, making this solution the preferred one. On the other hand, coherent detection involves a local oscillator (LO) to retrieve the phase information, which is defined by the in-phase and quadrature (IQ) components (or amplitude and phase) of the complex amplitude and the SOP of the incoming signal. This makes the coherent receiver very sensitive to phase and polarization fluctuations. So coherent detection tends to be more complicated than IM·DD. The SOP receiver dependency has been solved detecting each polarization of the transmitted signal through orthogonally polarized LO lasers, and post-processing. This is known as polarization-diversity scheme. In order to further increase the unrepeated transmission distance, quantum-noise-limited receiver has been introduced. This limit can be hit increasing sufficiently the LO power injected into the coherent receiver. Heterodyne systems involved a down conversion to an intermediate-frequency (IF). The most common modulation was the frequency-shift keying (FSK), because the easiness of modulating the laser frequency by changing the biasing current. The required IF frequency should be much higher than the signal bit rate. For homodyne receivers, the downconversion falls directly on the base band, so no high frequency IF is required. Here the carrier phase should be tracked in the optical domain by the LO, so an optical phase-locked loop (OPLL) is required. The phase error between the LO and the carrier takes a while before closing the loop on the LO controller. Because of such loop delay, it is not easy to maintain the stability and the bandwidth is usually limited to 1 MHz. So for large frequency drift, tracking results very hard. The high IF required and the difficulty in tracking carrier with large frequency fluctuation, make the heterodyne and homodyne solutions much more complex than the IM·DD one.

1.2.3 Coherent transceiver

From the previous section, looking for simplicity, the IM·DD is the best choice. But trends and forecasts say that the target is the link capability. A viable solution has been found in combining WDM and coherent detection. WDM allows to use a number of optical carrier signals onto a single optical fiber by using different wavelengths of laser light. This increases straightforward the amount of data that can travel through a link. Despite the already introduced struggles,



(a) Optical transmitter.



(b) Optical receiver.

FIGURE 1.7: DSP based optical transceiver.

coherent broadens the data processing chance. Functions as compensation for GVD and PMD of fibers can be implemented, and multi-level modulation formats can be introduced. For example, with a QPSK modulation/demodulation scheme, with optical IQ modulation (IQM), the bit rate can be doubled with the same baud rate [7]. These *equalization* operations have been made available thanks to very high speed DSPs. Figure 1.7 shows the main building blocks of a transceiver. The data come to the transmitter as parallel streams of bit (Figure 1.7a). A DSP serializes these streams and groups bits to provide the I and Q signals. The modulated signals are impressed on the carrier by an EOM driven through an electrical buffer. Mixing and 90° carrier phase shift are performed in the optical domain. So now we talk about optical IQ components. On the receiver side (Figure 1.7b), the modulated optical carrier is down-converted at baseband by optical mixers. The electrical I and Q signal are restored after photodiodes and TIAs. A DSP processes and de-serializes the bit streams [8] [9]. The introduced homodyne receiver block diagram does not deal with the already told optical phase locking issue. This because DSP itself provides a reliable and efficient carrier phase estimation, removing the stability concerns introduced by the OPLL. Because of all of these post-detection processing, this has been renamed *digital coherent receiver*. This introduces the requirement for very high-speed ADC and DSP.

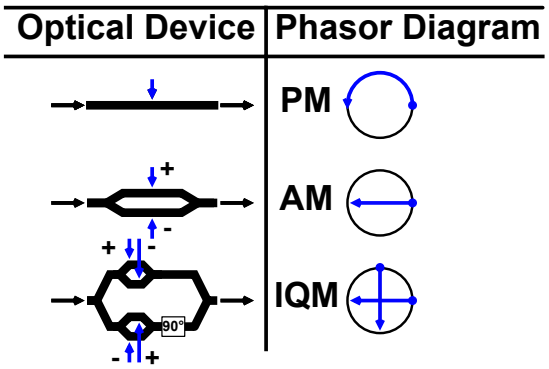


FIGURE 1.8: Phasor diagram and optical device structures for PM, AM and IQM.

1.2.4 Multi-level modulation formats

Coherent detection opens the possibilities to exploit any kind of multi-level modulation formats [10]. Phase modulation (PM), amplitude modulation (AM) and (IQM) lead to different phasor diagrams and they require different optical device structures as shown in Figure 1.8. Light phase-modulation can be achieved through non-centrosymmetric crystal, introducing a refractive-index variation linearly proportional with the applied voltage. Light phase can also be modulated through interferometer as MZM, driven in push-pull mode. Then recombining paths with different phases results in AM. The IQM can be provided by phase modulating lights with MZMs, while introducing a phase shift of $\pi/2$. The last one can perform any kind of multi-level modulation format. Another degree of freedom can be introduced by light polarization. Electromagnetic wave can travel with different spatial orientations, called polarizations. This enable to send two orthogonally polarized laser beams on the same fiber, obtaining a polarization multiplexed-signal. SOP of the incoming signal can be estimated thanks to digital signal processing. WDM, multi-level modulations and light polarizations are all uncorrelated modes, meaning that they introduce more degrees of freedom in data transmission and detection. *Spectrum efficiency* (SE) is a figure of merit defined as bit/s/Hz/polarization, so it normalizes the bit rate to the light bandwidth (WDM) and polarization. For a binary modulation format the spectral efficiency is 1 bit/s/Hz/polarization. In a multi-level format with m bits of information per symbol, the spectral efficiency reaches m bit/s/Hz/polarization. As examples, Figure 1.9 represents the constellation distributions for BPSK, QPSK, 8PSK and 16QAM schemes. Respectively, these formats can group 1, 2, 3, 4 bits for each symbol.

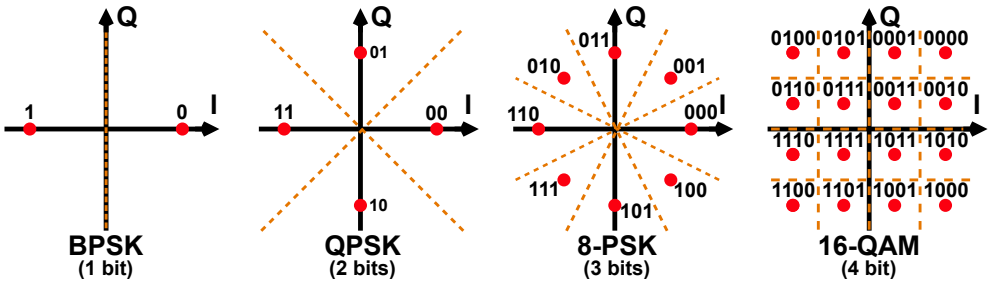


FIGURE 1.9: Constellation masks for BPSK, QPSK, 8PSK and 16QAM modulation formats.

The single channel link capacity C is defined by the *Shannon theorem* [11]

$$C = \frac{WD}{2} log_2(1 + \frac{S}{N}), \tag{1.2}$$

in which W is the channel bandwidth, D the modulation format dimension and S/N is the signal to noise ratio. As examples, for an IQ single polarization transmission the dimension is 2, becoming 4 for dual polarization transmission. Writing (1.2) as

$$\frac{C}{W(D/2)} = log_2\left[1 + \frac{C}{W(D/2)}\frac{E_b}{N_0}\right], \tag{1.3}$$

where the SNR has been rewritten as the Shannon limit of the spectral efficiency ($SE_{lim} = C/[W(D/2)]$) multiplied by the ratio of energy-per-bit to noise spectral density. So the (1.2) becomes

$$SE_{lim} = log_2\left[1 + SE_{lim}\frac{E_b}{N_0}\right]. \tag{1.4}$$

Once defined the Shannon limit of the spectral efficiency provided by the channel, the required energy-per-bit to noise spectral density ratio can be defined as

$$\frac{E_b}{N_0} = \frac{2^{SE_{lim}} - 1}{SE_{lim}}. \tag{1.5}$$

Given a specific modulation format, with M as number of symbols, the SE can be written as

$$SE = \frac{log_2 M}{D/2}. \tag{1.6}$$

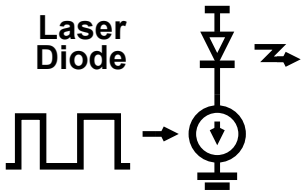


FIGURE 1.10: Laser driver schematic.

Another important specification is the *bit error rate*, which defines how many wrong bit detections are allowed. The incoming signals are corrupted by noise, phase drifts and others non idealities. Hence the detected symbols can be described with a *Gaussian density function*, centered around the ideal values reported in Figure 1.9. The stronger the non idealities the higher is the possibilities that one symbol crosses the thresholds, leading to a wrong detection. There is only one bit difference between adjacent symbols (Gray coding), in this way wrong detection means just one bit error. Spreading the Gaussian because of non idealities can increase the BER as much as reducing distances between levels. Multilevel formats help to increase the SE as proven by (1.6) but it also requires higher E_b/N_0 (1.5) to maintain the same BER. Increasing the energy per bit improves the spacing between levels, while reducing the noise spectral density squeezes the Gaussian. Therefore, decided or given the modulation format, and the BER required by the standard, the E_b/N_0 can be found by simulations.

1.3 Laser and Modulator Drivers

1.3.1 Requirements and challenges

The easiest way to describe a driver is to consider it as a simple current source for the electro-optical device (EOD), switching between on and off based on the bit stream to be transmitted (Figure 1.10).
There are several important requirements to be provided. Switching speed is fundamental to ensure light modulation with minimal inter-symbol interference. To generate enough optical power corresponding to logical ONEs, high output current is required. The high current generates voltage swing across the diode, so the driver output impedance is preferred to be high, in order to have as less as possible current variation. For what concern EOM drivers, previously introduced, speed is still a mandatory specification, while regarding the electrical signal to be generated there is something different. As reported

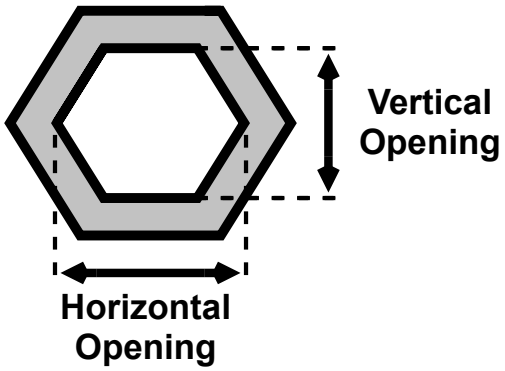


FIGURE 1.11: Eye diagram mask.

in Figure 1.3a, an external generator provides the optical power, while the EOM modulate the light amplitude and phase. The electrical signal should be capable to generate an electrical field strong enough to introduce the needed phase drift into the optical system. The impedance of these EOMs is very low, ranging from 30 to 50 Ω. This leads to large voltage and current signals. Based on the applications, distortion becomes relevant. PAM4 modulations are not so demanding in terms of linearity, while m-QPSK and m-QAM are based on poor distortion design. Speed and large swing go in opposite direction in terms of technology. Short channel transistors are mandatory to reach high frequencies. The shorter the channel the lower the breakdown voltage available, which is not suitable for large amplitude applications. Matching these two specifications with the same technology is a tough design challenge. At this large amplitude, transistor small signal modelling is good to understand whether the proposed solution is suitable or not. However, to assess a design goodness other tools are preferred. Eye diagram together with inter-symbol interference (ISI), allow a reliable glance to the system performance. Rise and fall times should be below the symbol period. Time is not the only constrain if multilevel modulation is involved. Amplitude overshoot and ringing can lead to detection impairments. In order to evaluate if the transmitted signal is suitable for a specific standard, masks are defined (Figure 1.11). Maximum tolerable eye closure in vertical and horizontal directions are defined by these tools. Since the high frequencies involved, these applications can be defined as millimeter-wave. This involves broadband matched terminations even for short distances. The silicon die and the EOM are usually co-packaged, or mounted one on the top of the other (flip-chip), so, matching for this termination is not required. Whereas for the input, the DSP which generates the data bit stream can be placed in a differ-

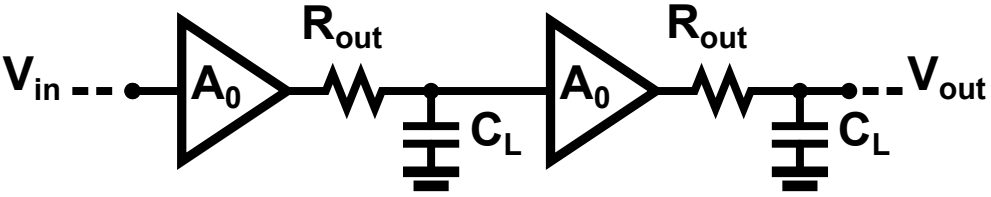


FIGURE 1.12: Small signal model for two stages cascaded amplifiers.

ent die and package, and connections are realized through transmission lines. Broadband input matching is then mandatory, to avoid back reflection and power losses.

1.3.2 Design approaches

This paragraph reports several guidelines, in order to properly start a driver design. Given the required amplification, considerations about the number of stages involved can be done. Small signal analysis is a good approach at this level. Each stage can be represented as a voltage amplifier A_0, an output resistance R_{out} and a load capacitance C_L, as shown in Figure 1.12, and it behaves as low-pass filter, because of the single pole introduced.
The limited bandwidth affects the eye opening both horizontally and vertically, introducing ISI. In a two levels modulation, when a series of ZEROs are followed by a ONE (or the other way around) the settling voltage at each output can be described as

$$V_{out} = V_0\left(1 - e^{-\frac{t}{\tau}}\right), \tag{1.7}$$

where τ is the time constant defined as $R_{out}C_L$. Given the bit period T_b, the error between V_{out} at $t = T_b$ and the final value is

$$\begin{aligned} V_0 - V_{out}(T_b) &= V_0 \cdot e^{-\frac{T_b}{\tau}} \\ &= V_0 \cdot e^{-\frac{2\pi f_{-3dB}}{R_b}}, \end{aligned} \tag{1.8}$$

writing $T_b = 1/R_b$ and $f_{-3dB} = 1/(2\pi R_{out}C_L)$. It is straightforward that, for a given f_{-3dB}, the error increases with the bit rate. Choosing R_b close to $2f_{-3dB}$ leads to a 8.32% normalized amplitude error (taking into account both the high and low level ISIs), hence a total eye closure of $|20log(1 - 8.32\%)| = 0.754$ dB. In a one-pole system is quite easy to relate the bandwidth to the eye opening,

as in this case. Considering more poles and zeros, as in Figure 1.12, system level simulations are used to estimate the transmitter speed requirement. The small signal transfer function from V_{in} to V_{out} (with R_{out}, C_L and A_0 equal through the chain) can be defined as

$$H(s) = \left(\frac{A_0}{1+\frac{s}{\omega_0}}\right)^2, \tag{1.9}$$

where the the -3 dB bandwidth of each stage is $\omega_0 = 1/(R_{out}C_L)$. -3 dB bandwidth can be used as a small signal measure for the circuit speed. Applying this attenuation to the amplitude of the (1.9),

$$\left[\frac{A_0}{\sqrt{1+(\frac{\omega_{-3dB}}{\omega_0})^2}}\right]^2 = \left(\frac{A_0}{\sqrt{2}}\right)^2, \tag{1.10}$$

the cascade ω_{-3dB} results

$$\omega_{-3dB} = \omega_0\sqrt{\sqrt{2}-1} \approx 0.644\omega_0. \tag{1.11}$$

The (1.11) shows that cascading two identical stages, means almost a 35% of bandwidth reduction. Repeating for N identical stages, the resulting -3 dB bandwidth can be defined as

$$\omega_{-3dB} = \omega_0\sqrt{\sqrt[N]{2}-1}. \tag{1.12}$$

So, the bit rate and eye opening knowledge can be used to understand the transmitter ω_{-3dB} required, and then the ω_0 of each stage. A gain-bandwidth (GBW) trade-off should be found in order to decide a proper number N of stages. Given the overall gain (A_{tot}), it can be achieved with a large number of stages with wide bandwidth and poor gain, or the other way around. The GBW product can be defined as $A_0\omega_0$ and assumed to be constant for the same technology and power consumption. The transfer function of each stage can be then defined as

$$H(s) = \frac{\frac{GBW}{\omega_0}}{1+\frac{s}{\omega_0}}. \tag{1.13}$$

With N identical stages, $A_{tot} = (GBW/\omega_0)^N$ and so $\omega_0 = B/\sqrt[N]{A_{tot}}$, results in a overall bandwidth approximatively

$$\omega_{-3dB} \cong GBW\frac{0.9}{\sqrt{N}\sqrt[N]{A_{tot}}}. \tag{1.14}$$

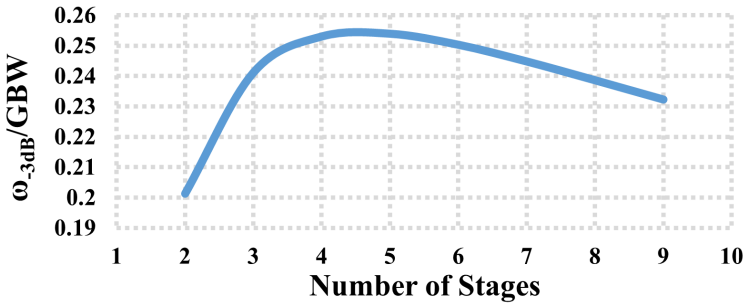


FIGURE 1.13: Normalized bandwidth as a function of N for $A_{tot} = 20dB$.

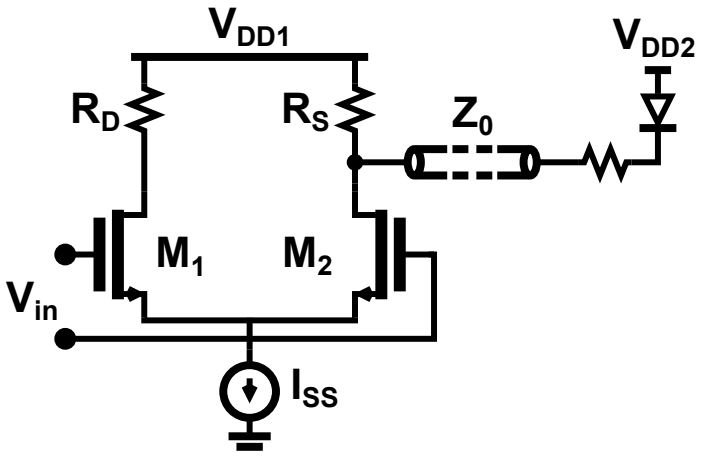


FIGURE 1.14: Laser diode current steering.

The (1.14) maximum can be achieved at the denominator minimum, which is not a monotonic function, therefore an optimum in function of N can be found. As shown in the curve reported in Figure 1.13, suitable N values are 4 and 5.

Since the last stage is asked to drive the laser or the electro-optical modulator, several constraints relay on this block. Depending on the kind of modulation and on the electro-optical transducer involved, the signal specifications can be different. For m-QAM modulation at the far-end, to retrieve the original data, amplitude and phase are used, hence the distortion introduced by the transmitter can corrupt the transmitted information. A laser requires a current signal to work properly, while a Mach-Zehnder modulator is a voltage driven device. This means that the last stage design is strongly related to the

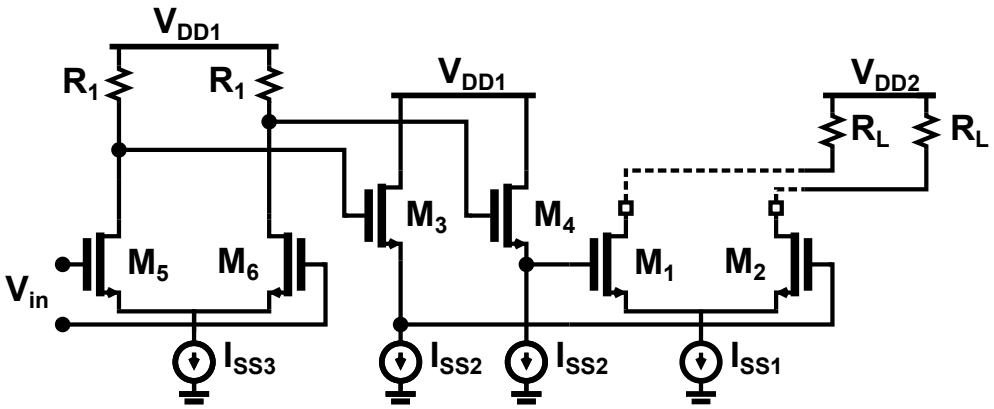
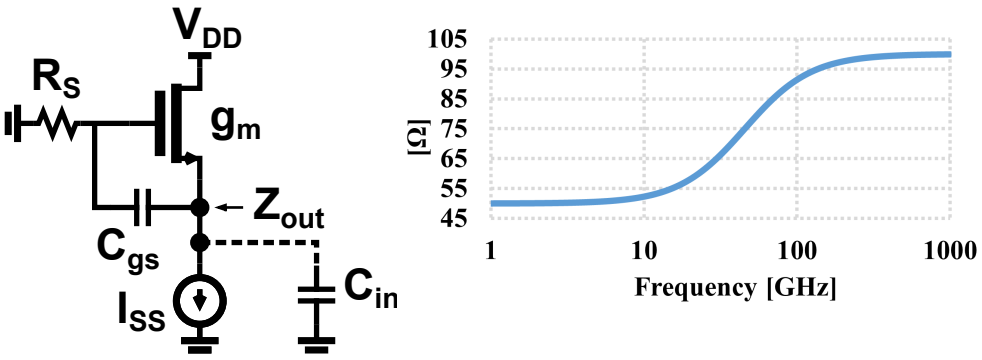


FIGURE 1.15: Cascade of a main driver, pre driver and a gain stage.

following optical systems. In Figure 1.14 a possible implementation of a laser driver is reported. Even though the laser diode requires a single ended (SE) signal, differential signals are preferred for many reasons. SE signals cannot be distinguished from common mode, so any corruption coming from the supply (noise, supply fluctuation...) directly affects the information carried. While differential structures allow to delete any common mode impairment as long as the symmetry between the two anti-phase signals holds. Since a laser diode is a SE device just one side is taken as output, while the other one is terminated over a resistance R_D to maintain the symmetry.

In the earlier transceiver the electrical and optical parts were realized in different packages, requiring impedance matching to avoid back reflection. From the laser side, the impedance showed is much lower than the characteristic impedance Z_0, therefore a series resistance is added. Since in Figure 1.14 the current steering is realized by an open-drain, a resistor R_S lowers the output impedance ensuring matching. This results in a two times larger current to be provided, because half of the signal is "wasted" on R_S. Silicon photonics overcome this issue, making available highly integrated photonic systems. Photonic and electronic functions are not realized on the same process, because they have requirements, sizes and costs very different (electronic requires advanced and fine CMOS processes which are not required for photonic components). Yet hybrid approaches have been implemented. The electronic integrated circuit responsible to drive the photonic modulators is a discrete component flip-chip mounted on the silicon photonic platform. Flip-chip integration ensure high-speed operations, and matching is no longer a requirement [12].



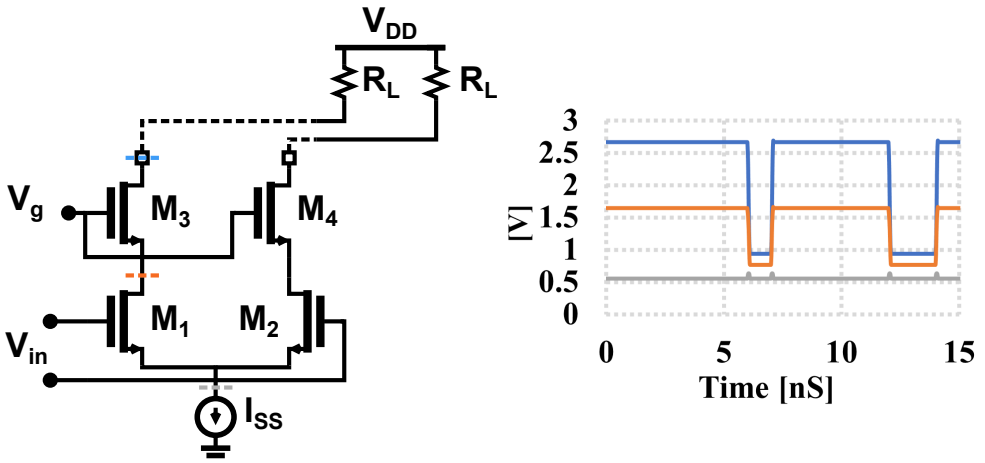
(a) Loaded source follower. (b) Source follower output impedance.

FIGURE 1.16: Source follower output impedance analysis.

Figure 1.15 shows an example of driver chain. Since matching is no longer required the main driver is designed as an open drain, and R_L is the off-chip loading provided by the electro-optical modulator. The output stage design begins with the signal to be provided to the EOM. Assuming a load impedance R_L=50 Ω, and a required differential output amplitude of 750 mV, results in a minimum tail current I_{SS1} of 15 mA. The transistors M_1 and M_2 must be sized in order to steer the previous current. The smaller the MOS size ratio W/L the higher is the overdrive $(V_{gs} - V_{th})$ required to drive the whole current. This allows to have less parasitic capacitances from M_1 and M_2, while demanding a larger input swing, provided by increasing R_1. Since the R_1 grows faster than the parasitics reduction, a pre-driver can be used to preserve the behaviour in frequency. Implementing this pre-driver as a source follower, as in Figure 1.15, allows to have a lower impedance driving M_1 and M_2, hence an higher frequency pole. Nonetheless this solution has some drawbacks. In order to provide enough gain R_1 should be large enough, ending in a voltage drop defined as $R_1 \cdot I_{SS3}/2$. Then $V_{gs,M3/4}$ and $V_{gs,M1/2}$ shifts down the DC voltage. So an higher V_{DD1} can be required to leave some voltage headroom to I_{SS1} to work properly. Besides the headroom consumption, also stability concern is introduced. The output impedance of the follower reported in Figure 1.16a can be described as

$$Z_{out} = \frac{1}{g_m} \frac{1 + sC_{gs}R_S}{1 + s\frac{C_{gs}}{g_m}}. \tag{1.15}$$

Comparing Figure 1.16a toFigure 1.15, R_S is meant to be higher than g_m. This leads to an inductive behaviour over frequency for the source follower output impedance, as shown in Figure 1.16b. Since the input of the main driver can be



(a) Main driver cascoded. (b) Voltages distribution for a cascode.

FIGURE 1.17: Voltage swing improvements in a cascoded solution.

modelled as a big capacitance C_{in}, the resonance between this capacitance and the output impedance should happen out of band in order to avoid instability.

In long reach-applications, where the number of parallel optical links is a tight constraint, the bandwidth of the EOM becomes crucial. This is mainly defined by the parasitics introduced by the optical device, making the component size a bottle neck for speed. Hence smaller components lead to higher bit rates. Considering a MZM, the interferometer length affect both the bandwidth and the V_π, but in opposite direction. The shorter the MZM the higher is the voltage required to generate an electrical field capable to change the light phase. This can introduce some issues from the transistor reliability point of view. The latest CMOS technologies allow to have channel length up to tens of micrometers, enabling the chance to process millimeter wave signals. While the speed is increased, the junction break-down voltage is reduced. Technology knots that can reach hundreds of GHz of f_t can support voltages up to 1 Volt (even less considering thin-oxide options). Figure 1.17 shows how cascoding can help to increase the swing efficiency avoiding junction failure. Especially in Figure 1.17b, the achievable peak-to-peak single ended voltage is wider than the drop over a single transistor. Thanks to $M_{3/4}$ the theoretical maximum voltage achievable is $V_{ds,I_{SS}} + V_{dsmax,M_1} + V_{dsmax,M_3}$, while for the main driver in Figure 1.15 is $V_{ds,I_{SS}} + V_{dsmax,M_1}$. This newer upper voltage boundary can be used as a V_{DD} value. The main driver power consumption is defined as

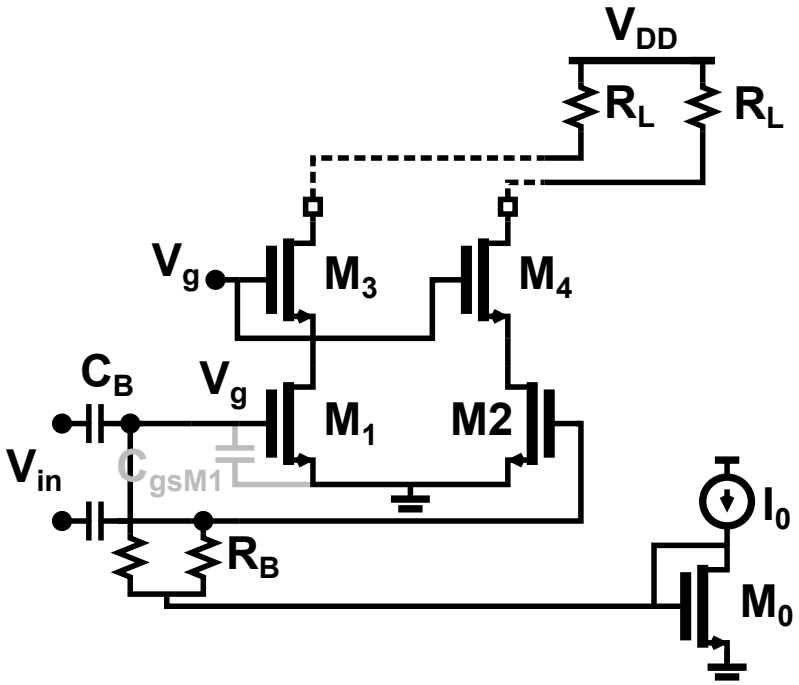


FIGURE 1.18: Main driver with no current source.

$V_{DD}I_{SS}$, where I_{SS} is mainly defined by the required output voltage swing while V_{DD} by the number of stacked transistors (in order to have them all working in saturation). Then, with regard to the power consumed, cascoding is a weakness. As reported in Figure 1.18, I_{SS} can be removed and $V_{ds,I_{SS}}$ can be spared. The current is defined by the size of M_1 (M_2) and the gate level at the first order. DC coupling the gate with the rest of the chain introduces a strong dependency of the current from process variations. AC coupling is therefore preferred, while the gate level is set through a diode connection, resulting in no effects over the current because of process. The proper design of R_B and C_B is not trivial, because the AC coupling introduce an attenuation and high-pass behaviour. Considering the parasitic $C_{gs,M1}$, the signal V_g is defined as

$$V_g = V_{in} \times \frac{C_B}{C_B + C_{gs,M1}}, \tag{1.16}$$

hence choosing $C_B = C_{gs,M1}$ results in a 6 dB attenuation from V_{in} to V_g. To avoid any attenuation, $C_{gs,M1}$ should be negligible compared with C_B. $C_{gs,M1}$ is proportional with M1 width, resulting in large amount of parasitic since it has to carry all the main driver current. C_B cannot be arbitrarily high

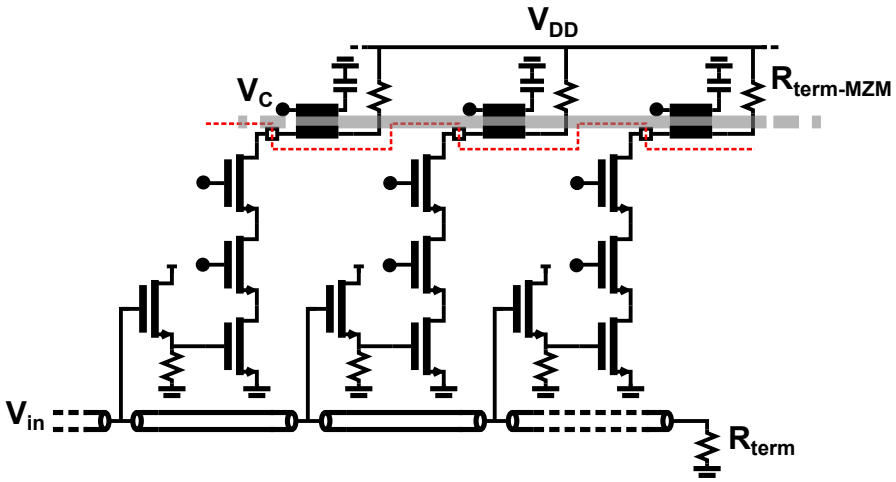


FIGURE 1.19: Schematic solution proposed by [13].

for two reasons, first, integration of large capacitor is not easy and can lead to manufacturing issues, second, the capacitor parasitics between the bottom plate and the substrate are proportional with the size. So these are the trade-off for C_B. Assuming a two-levels modulation (ONE or ZERO) non-return to zero (NRZ), the high-pass behaviour limits the number of consecutive ONEs. The time constant $1/R_BC_B$ defines the maximum number of ONE periods in a row before the voltage crosses the threshold resulting in a wrong detection.

1.4 State-of-the-art solutions

In this section a couple of already fabricated and published solutions are briefly described and discussed. The literature is quite poor about works which address the design of CMOS optical driver for coherent applications, but still it is useful to understand the main circuit solutions involved in the modulator driver field.

The need of very large transistors to be capable to steer all the current required to generate the output voltage swing introduces a no negligible bandwidth limitations. One available solution is to exploit the properties of a *transmission line* [4]. A lossless transmission line shows an infinite bandwidth and a constant delay, so a linear behaviour in phase. The characteristic impedance Z_0 and the propagation velocity are respectively defined as

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{1.17}$$

$$v = \frac{1}{\sqrt{L_0 C_0}} \tag{1.18}$$

where L_0 and C_0 are the inductance and capacitance per unit length. A large transistor can then be sliced m times in m times smaller transistors and it can be distributed along the transmission line. In this way the parasitic input capacitance of each slice is reduced by a factor of m and can be considered together with the C_0, which in turns can be redesigned to get back the desired line characteristic input impedance. The same holds for the output side of the transistor. So ideally a *distributed amplifier* shows infinite bandwidth and input and output low impedance, which are useful features for a MZM driver. The main limitation of a real transmission line comes from the metal resistivity which introduces losses (and so bandwidth limitation) and the finite range of characteristic impedance achievable (defined by the metal stack made available by the technology). An example of this technique is reported in [13]. In this case a distributed MZM driver has been fabricated in a 45-nm CMOS SOI technology, reaching an electrical bandwidth of 26 GHz. As shown in Figure 1.19 (a single ended version of the circuit is reported), instead of driving a MZM through a single large electrode, it has been broken in several smaller segments each one driven by single slice of the integrated distributed amplifier. The amplifier input transmission line should be designed to match the phase delay introduced by the MZM. In case of differences between the input and output phase delay, the transfer function will suffer from ripple. Each slice is realized by a source follower, which reduces the loading over the input line. A stack of three transistors provides a 2.2 V_{pp} single-ended signal for the MZM. Stacking more than one transistors is required to avoid any breakdown given the high voltage involved. This solution is open collector, so the supply voltage comes from the resistive electro-optical modulator terminations. This work shows how co-design between electrical and optical components can be used to improve the system performance. Distributed solution can results in very broadband circuits, but it is very expensive in terms of area and power consumption. Transmission line requires a lot of space to be effective (the line should be electrically long compared with the wave-length of the signal). Furthermore, cascade of more stages (e.g. for gain control) could becomes an issue because of the low impedance provided by the driver input transmission line.

The MZM driver reported in [14] and shown in Figure 1.20, has been fabri-

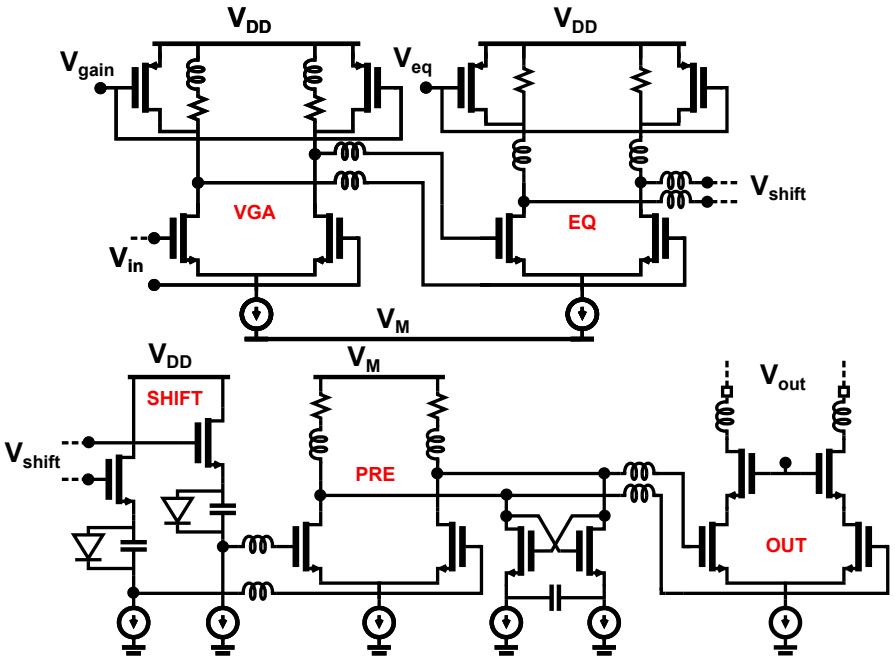


FIGURE 1.20: Schematic solution proposed by [14].

cated in a 65-nm CMOS technology, and it is intended for coherent applications. The differential output swing provided is 2.9 V_{pp} for a differential load ranging from 50 to 100 Ω, with an electrical bandwidth close to 35 GHz. The distortion measured at 2 $V_{pp,diff}$ is 5% at 1 GHz. The transmitter is realized as a four stages chain, involving a variable gain amplifier, an equalization stage, a pre-amplifier and an output stage implemented as an open-drain. To reduce power consumption current reuse has been implemented by stacking the first two stages with the pre amplifier. A level shifter has been used to accommodate the DC common mode between the equalizer and the pre amplifier. Gain control is implemented at the first stage by a gilbert-cell to reduce as much as possible the distortion along the chain. All the stages are implemented as differential pair with passive loads realized by resistors and inductors to extend the bandwidth. The equalizer allows to control the frequency behaviour tuning the amount of peaking by changing the resonance quality factor. The pre amplifier is usually a 0 dB gain block which feeds the main driver without loading to much the previous stages. A negative capacitance compensates part of the parasitics coming from the last differential pair. It is implemented by an explicit capacitance and closing in a positive loop two transistors. The output amplifier

is open drain and cascoded, to allow large swing avoiding breakdown. In this publication, most of the known techniques to extend the bandwidth have been implemented. It is also interesting because a fully electrical characterization is provided, reaching a good eye opening for 50 Gb/s and an optical measure of a 56 Gb/s QPSK constellation. This can help to relate electrical and optical performance, in case of lack of system level measurements.

Chapter 2

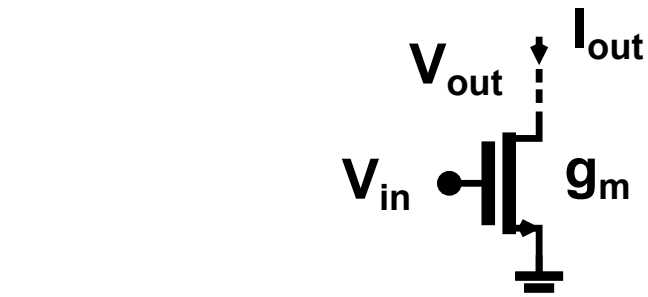
A 58 GHz Bandwidth, Linear, Mach-Zehnder Driver

Abstract
In the following pages the design and realization of a linear Mach-Zehnder modulator driver is presented. The aim of such a design is to prove that, even if the mainstream technologies for this application are Silicon-Germanium BiCMOS (SiGe-BiCMOS) and Indium Phosphide Double Hetero-junction Bipolar Transistor (InP-DHBT), CMOS is a viable solution. The main benefits on doing this would be the lower technology cost. Looking at the future, this can bridge the gap between digital-oriented highly scaled processes, such as fin field-effect transistor (FinFET), and purely analog functions. The chance to integrate all the functionalities on the same die would strongly reduce the system costs while enhancing the performance because of the interconnections removal between discrete components. The chapter describes specifications and how they have been satisfied, through schematics, simulations and testing. The driver is required to have a voltage swing of 1.5 $V_{pp,diff}$ over a 50 Ω impedance with a distortion below 1.8 %. The gain can be tuned from 20 to 10 dB (for the same output signal amplitude) with a better linearity for the lower values. The power consumed at maximum gain is 297 mW with a single supply voltage of 2.4 V.

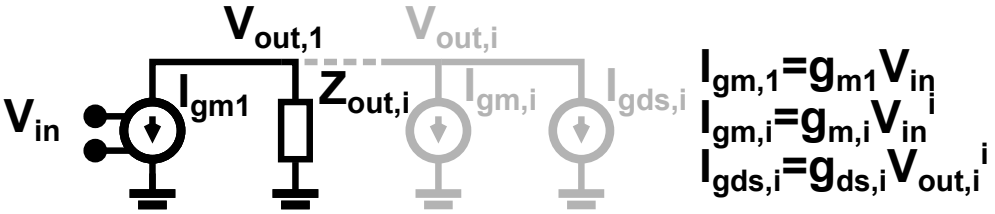
2.1 Linearity and Distortion

2.1.1 Harmonic distortion

A small signal approach is often used for integrated circuit design. It is useful in order to estimate the frequency behaviour of schematic solutions and it is



(a) Transconductor.



(b) Transconductor model with non-linear contributors.

FIGURE 2.1: Simple non-linear model for a transconductor.

reliable when the involved amplitude is not so large. When the signal amplitude is no more negligible, modelling the transistor with an input transconductance and output conductance at the fundamental frequency is not enough. Figure 2.1b shows a possible way to model also non linear components coming from the transconductor in Figure 2.1a [15]. The output voltage is then defined as

$$V_{out} = \sum_{i=0}^{n} V_{out,i}, \tag{2.1}$$

where the index i refers to the components placed at ω_{in}, $2\omega_{\text{in}}$, ..., $\text{n}\omega_{\text{in}}$. ω_{in} is the input tone frequency. $\text{V}_{\text{out,1}}$ is the desired element, defined as

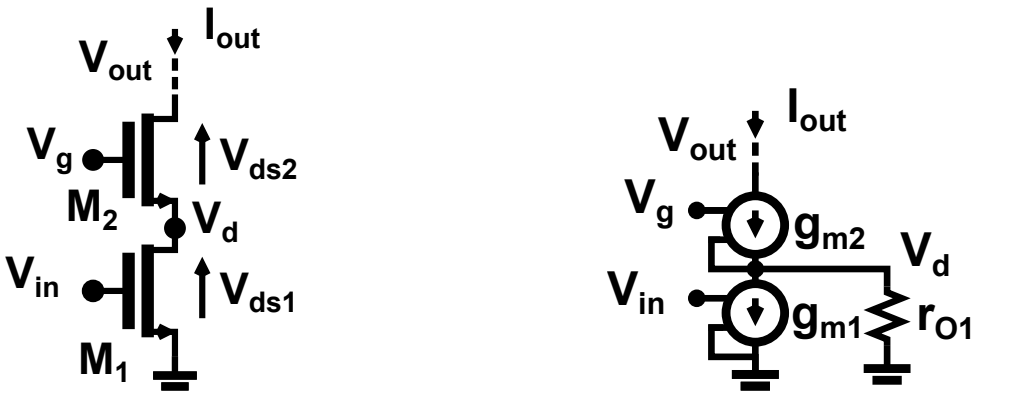
$$V_{out,1} = V_{in} \cdot g_{m1} \cdot Z_{out,1} \tag{2.2}$$

$$= V_{in} \cdot A_V, \tag{2.3}$$

and A_V is the linear gain. The spurious harmonics are defined as

$$V_{out,i} = I_{out,i} \cdot Z_{out,i} \tag{2.4}$$

$$= (I_{gm,i} + I_{gds,i}) \cdot Z_{out,i}. \tag{2.5}$$



(a) Cascoded transconductor. (b) Model of a cascoded transconductor.

FIGURE 2.2: Cascoded transconductor analysis.

From (2.5) Figure 2.1b, it is easy to notice the two distortion sources. An input component is described by $g_{m,i}$, and an output one by $g_{ds,i}$. Hence, knowing the frequency behaviour of the output impedance Z_{out}, a rough model of Figure 2.1a including non-linearity can be realized. Since $g_{m,i}$ and $g_{ds,i}$ are non-linear coefficients, the model is reliable for a bounded amplitude range. These coefficients can be derived from $I_{out,i}$ as

$$\begin{cases} g_{m,i} = \frac{I_{out,i}}{V^i_{in}} & \text{with } V_{out} = 0; \\ g_{ds,i} = \frac{I_{out,i}}{V^i_{out,1}} & \text{with } V_{in} = 0; \end{cases} \tag{2.6}$$

Through the relation between V_{in} and $V_{out,1}$ of (2.3), the coefficients of the (2.6) can be referred to the input or to the output in order to make a fair comparison.

$$\begin{cases} g_{m,i-out} = \frac{I_{out,i}}{V^i_{in,1}} \cdot A^i_V & \text{with } V_{out} = 0; \\ g_{ds,i} = \frac{I_{out,i}}{V^i_{out,1}} & \text{with } V_{in} = 0; \end{cases} \tag{2.7}$$

As an example in (2.7), both the coefficients are referred to the output. If the dynamic range to be covered becomes large, the coefficients $g_{m,i}$ and $g_{ds,i}$ turns to be amplitude dependent, so more complex modelling would be required. Still, Figure 2.1b is a good approximation to understand which is the main distortion source. For instance, if the main contributor results to be the input side, increasing the gain (so reducing the input amplitude for a given output swing) may help to increase the performance in term of linearity.

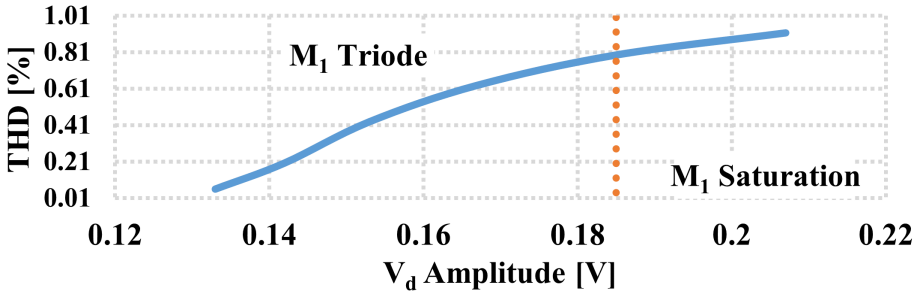


FIGURE 2.3: THD versus V_d amplitude.

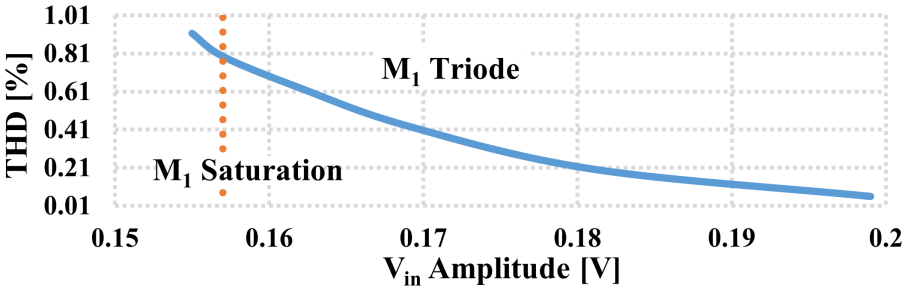


FIGURE 2.4: THD versus V_{in} amplitude.

2.1.2 Triode region

In the previous paragraph a tool to understand which is the main source of distortion is reported. As told, in order to reduce the input distortion the amplitude can be reduced by increasing the gain. This cannot work for the output component in case of fixed swing. The fabricated design is intended to propose a way to improve the transmitter behaviour at large signal regime. Figure 2.2 shows a cascoded transconductor (Figure 2.1a) and its model (Figure 2.1b). M_1 and M_2 have the same size, and the node V_g can be arbitrarily decided. The two transistors are interested by the same current I_{out} defined by V_{in}, V_{ds1} and the transistor size. The gain from V_{in} to V_d can be written as

$$A_{V_{in},V_d} = \frac{g_{m1}}{g_{m2} + \frac{1}{r_{o1}}}, \tag{2.8}$$

since M_1 and M_2 work in saturation, g_{m1} and g_{m2} are the same and $1/r_{o1}$ is negligible, hence (2.8) becomes 1. This means that the amplitudes of V_{in} and V_d are the same. It is straightforward that, the larger the input amplitude the larger the voltage swing at V_d, which in turn increases the current modulation

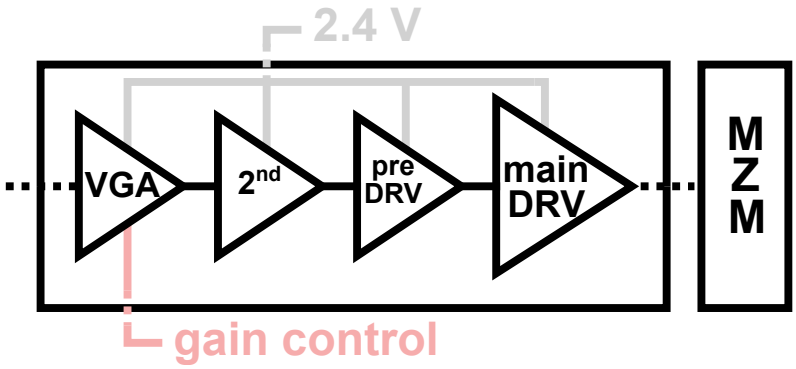
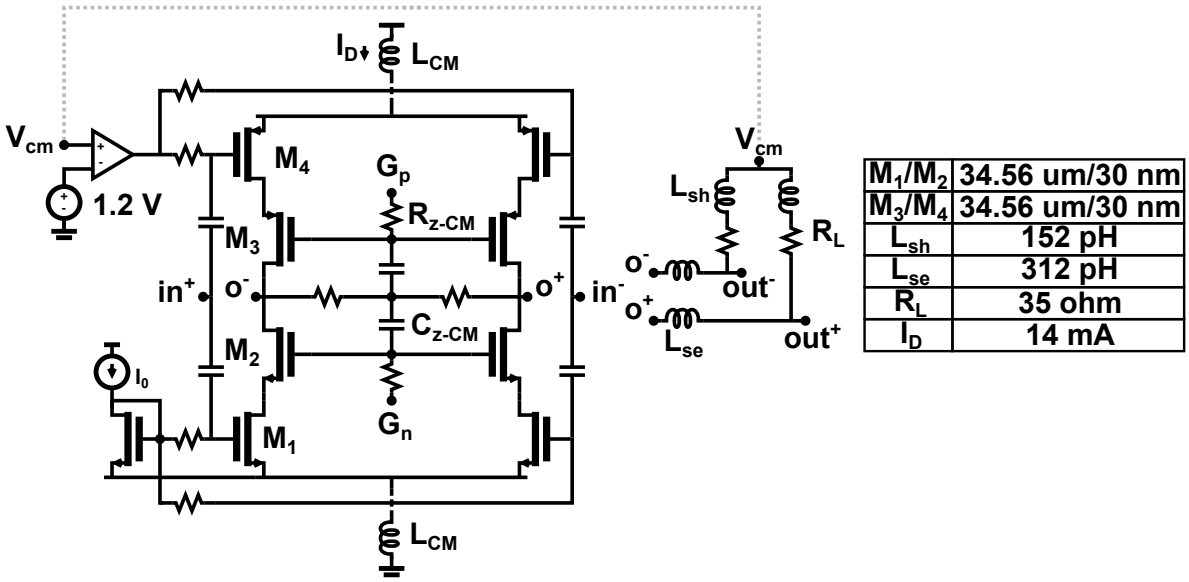


FIGURE 2.5: Transmitter block diagram.

and so the distortion (Figure 2.1). Lowering the V_g node, for a fixed I_{out} current, lowers the V_d voltage of the same amount. This allows to decide in which region M_1 works, triode or saturation. Towards the triode region g_{m1} and r_{o1} are both reduced, while g_{m2} is almost kept constant. Back to the (2.8), it means that an attenuation is introduced from V_{in} to V_d, so the I_{out} is less affected by the drain modulation. In Figure 2.3 the linearity behaviour of Figure 2.2a is reported as a function of the V_d amplitude, maintaining the output swing V_{out} constant. The amplitude reduction is achieved pushing M_1 in triode. The orange dotted line is the triode threshold, and it can be noticed how the linearity is improved working below this limit. Working in triode means a lower g_{m1} so an attenuation in term of gain. To have a constant output a larger input amplitude is then required. Figure 2.3 shows how the distortion is reduced, while the input amplitude is increased for the same output swing. This is interesting, because usually, larger signal amplitude means linearity impairments. This behaviour is exploited in the fabricated solution to perform gain variation without introducing linearity degradation.

2.2 Transmitter Design

The transmitter proposed is made of four stages, where the first, the second and the last one are implemented exploiting the transistor triode region as described in the previous paragraph. The third one, a pre-driver, is a source follower which is responsible to feed the parasitic capacitances of the fourth big stage, without affecting the bandwidth. The transmitter has been designed to drive a Mach-Zehnder Modulator terminated over 50 Ω(a behavioural model has been provided by the company, but we are not allowed to share any graph or



M_1/M_2	34.56 um/30 nm
M_3/M_4	34.56 um/30 nm
L_{sh}	152 pH
L_{se}	312 pH
R_L	35 ohm
I_D	14 mA

FIGURE 2.6: Variable gain amplifier schematic.

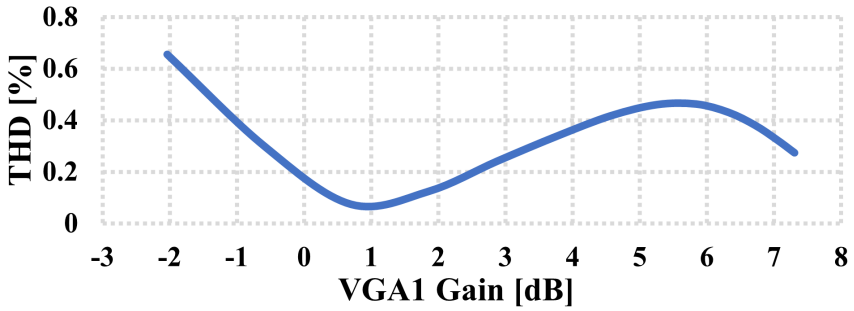


FIGURE 2.7: Variable gain amplifier THD versus gain.

related information about it). At this stage, the gain is hand controlled taking DC signals off-chip and the whole variation is provided by the first amplifier. In next realizations, the gain control will be performed automatically through a feedback loop made by a photodiode and a peak detector. A single 2.4 V supply voltage has been used, provided by an external low drop-out (LDO) regulator. Since we are not yet able to integrate the digital part, the digital-to-analog converter and the analog transmitter, input matching is required to reduce the return loss (and also for testing purpose)

2.3 Variable Gain Amplifier

The first stage (Figure 2.6) provides the whole 10 dB gain variation. In this way the signal amplitude for the following stage is constant through all the gain configurations, so they can be optimized in term of linearity. In Figure 2.3 the proposed schematic is reported. An inverter-like solution is proposed, exploiting in this way both the p- and n- side g_m saving current. To spare voltage headroom the biasing current is defined by M_1 so the common mode current mirror is removed. AC coupling helps to fit all the four transistor stacking without reaching the break-down voltage.

2.3.1 Gain programmability

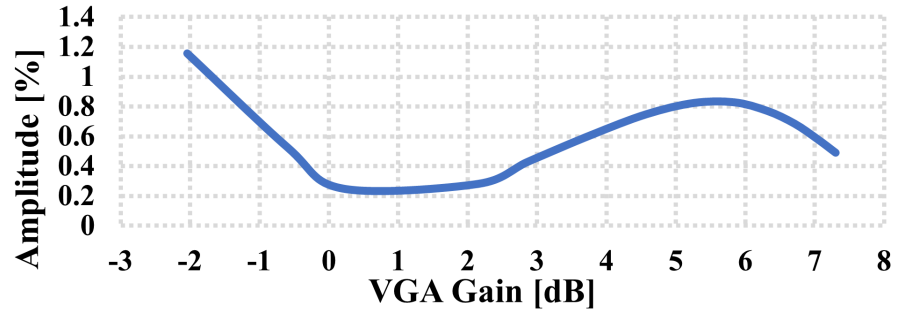
Terminal G_p and G_n are taken off-chip and used as knob for the gain variability. Gain variation is performed by pushing M_1 and M_4 from linear to triode region, as explained in the previous paragraph. As shown in Figure 2.7 the VGA has better linearity performance at lower gain, and this holds for the positive range. Below 0 dB, when the VGA is attenuating the signal, the distortion get worse. The main distortion contributor is the third harmonic, and in Figure 2.8 it is reported how it changes with the gain. In Figure 2.8a, the third harmonic amplitude drops with the gain in the positive range, while it increases when an attenuation is introduced. From gain to attenuation, the phase of this component experiences 180° shift, as in Figure 2.8b. Since all the following stages introduce gain, the third components injected are in anti-phase with this first one, so a cancellation happens through the overall transmitter. Hence, while attenuating, a pre-distortion mechanism is provided by the VGA.

2.3.2 Reverse triple resonant network

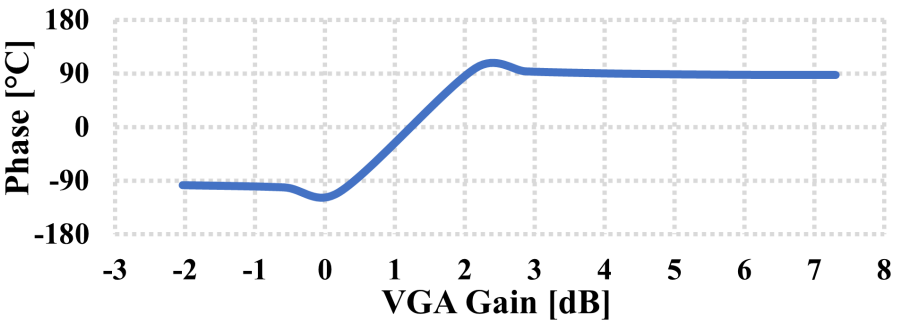
A differential resistor R_L is used to achieve the desired gain by this stage. Bandwidth limitations are mostly defined by parasitic capacitances coming from the stage itself and from the following stage. A simple small signal model of Figure 2.6 is reported in Figure 2.9, which helps to understand the frequency behaviuor. C_{out} and r_{out} are respectively the capacitive and resistive loading coming from the VGA itself while C_{in} comes from the next stage. Without considering the explicit inductors the -3 dB frequency would be

$$\omega_{-3dB} = \frac{1}{(C_{in} + C_{out})(R_L || r_{out})}. \tag{2.9}$$

The purpose of the series (L_{se}) and shunt (L_{sh}) inductors is to create resonances together with the parasitic capacitances to compensate the gain drop over



(a) Amplitude of the third harmonic component versus gain.



(b) Phase of the third harmonic component versus gain.

FIGURE 2.8: VGA third harmonic component versus gain.

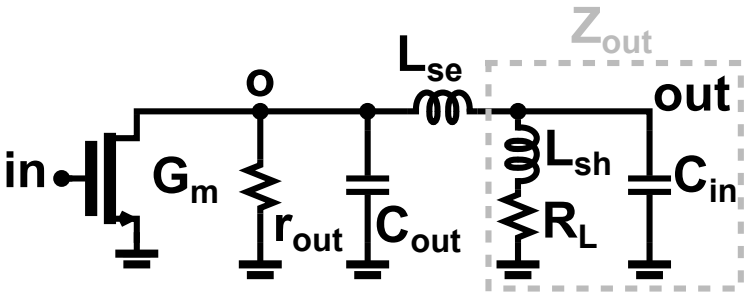


FIGURE 2.9: Small signal model for Figure 2.6.

frequency, increasing the -3 dB crossing. This circuit is called Reverse Triple Resonant Network (RTRN) because three resonances can be found [16]. During circuit design, the modelling of Figure 2.9 is still rough. Assuming the parasitics as grounded capacitors is not sufficient to proper fit the Figure 2.6 behaviour,

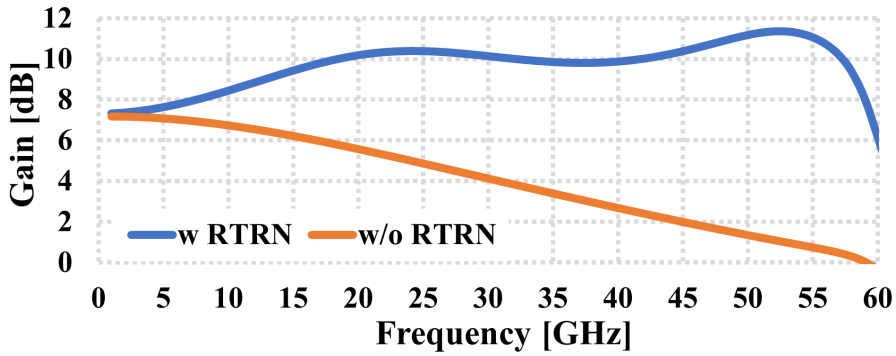


FIGURE 2.10: VGA gain with and without the reverse triple resonant network.

because the whole chain affects these impedance values. However, simulation tools are available and reliable for a fine design, which means that Figure 2.9 is enough to get an idea whether the network would be of help or not. (2.9) defines the starting bandwidth, while the DC gain is $g_m(r_{out}||R_L)$. The first resonance is given by the parallel of L_{sh}, C_{in} and C_{out} at $\omega_1 \cong 1/\sqrt{L_{sh}(C_{in}+C_{out})}$, hence the node "o" can be considered an high impedance. The gain at ω_1 can then be written as

$$A_{V,RTRN}(\omega_1) \cong G_m \cdot r_{out} \cdot \frac{Z_{out}(\omega_1)}{Z_{out}(\omega_1) + j\omega_1 L_{se}}, \tag{2.10}$$

where $Z_{out}(\omega_1) = C_{in}||(R_L + j\omega_1 L_{sh})$. A series resonance happen at $\omega_2 \cong \sqrt{L_{se}C_{in}}$, where most of the G_m current flow into C_{in} giving approximately

$$A_{V,RTRN}(\omega_2) \cong G_m \cdot \frac{1}{j\omega_2 C_{in}}. \tag{2.11}$$

The last resonance is again a series resonance between L_{se}, C_{in} and C_{out} at $\omega_3 \cong 1/\sqrt{L_{se}\frac{C_{in}C_{out}}{C_{in}+C_{out}}}$, giving

$$A_{V,RTRN}(\omega_3) \cong G_m \cdot r_{out} \cdot \frac{Z_{out}(\omega_3)}{Z_{out}(\omega_3) + j\omega_3 L_{se}}. \tag{2.12}$$

A proper design of these three resonances allows to increase considerably the bandwidth, as shown in Figure 2.10.

2.3.3 Common-mode gain

While saving voltage headroom, the use of pseudo-differential stage as in Figure 2.6 could introduce common-mode (CM) troubles. Furthermore the so far

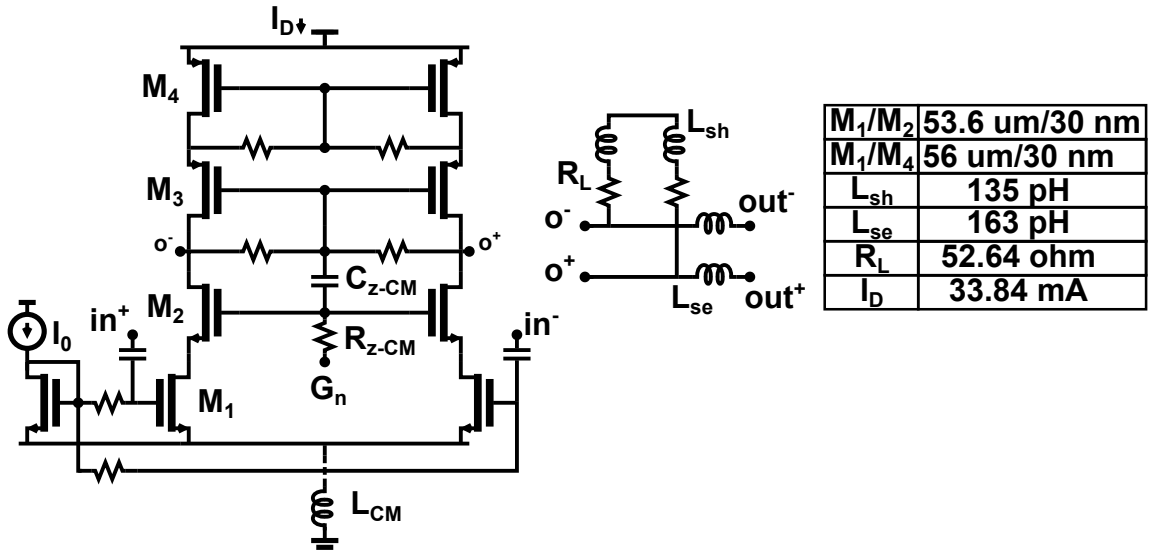


FIGURE 2.11: Second amplification stage.

discussed load is differential, meaning that the CM gain of Figure 2.6 is the intrinsic gain of an inverter. To avoid oscillations coming from high gain value, both the CM transconductance and impedance are reduced. Degeneration CM inductors are placed for the p- and n-side, making the CM transconductance to be

$$g_{m,CM}(\omega) = 2 \cdot \frac{g_{m,M1}}{1 + g_{m,M1} \cdot j\omega L_{CM}}. \tag{2.13}$$

A zero at $\omega_{z,CM} = 1/R_{z,CM}C_{z,CM}$, turns transistor M_2 and M_3 from common-gate to diode connected for the common-mode.

2.4 Second amplification stage

For the second amplification stage a n-only solution has been preferred, as reported in Figure 2.11. This allows to have a lower CM gain from this stage. A pseudo-differential structure AC coupled is exploited to spare voltage headroom. The G_n terminal has been taken off-chip to manage the working region of M_1. As for the VGA, transistor M_1 is biased in triode exploiting the linearity advantages previously reported.

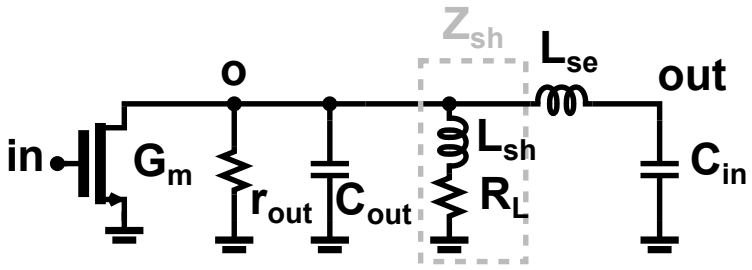


FIGURE 2.12: Small signal model for Figure 2.11.

2.4.1 Triple resonant network

A resonant network is used to compensate the parasitic and to enhance the bandwidth. A small signal model is reported in Figure 2.12. As for the previous resonant network this circuit, thanks to the three resonances, allows to compensate the gain drop coming from parasitic. This circuit is called triple resonant network (TRN) and it is slightly different from Figure 2.9 [17]. The starting -3 dB bandwidth is still defined by (2.9), and also the three resonances ω_1, ω_2 and ω_3 are at the same frequencies as for the RTRN. The gain at DC is $g_m(r_{out}||R_L)$, then at the parallel resonance ω_1 it becomes

$$A_{V,TRN}(\omega_1) \cong G_m \cdot r_{out} \cdot \frac{1}{1-\omega_1^2 L_{se} C_{in}}, \tag{2.14}$$

which is higher than (2.10), where the output branch is the parallel between $1/j\omega_1 C_{in}$ and $R_L + L_{sh}$, so a lower impedance value compared with the TRN one. The behaviour at the second resonance is the same as for the RTRN, so most of the G_m current flow into C_{in}, giving

$$A_{V,TRN}(\omega_2) \cong G_m \cdot \frac{1}{j\omega_2 C_{in}}. \tag{2.15}$$

At the last series resonance the gain is

$$A_{V,TRN}(\omega_3) \cong G_m \cdot (Z_{sh}||r_{out}) \cdot \frac{1}{1-\omega_3^2 L_{se} C_{in}}, \tag{2.16}$$

where $Z_{sh} = R_L + j\omega L_{sh}$. At ω_3 the RTRN Z_{out} is dominated by $1/j\omega_3 C_{in}$, as the TRN case. Since the TRN equation presents the parallel between Z_{sh} and r_{out} the (2.16) is lower than the (2.12). These considerations hold assuming the same model values for both TRN and RTRN (with the same G_m, r_{out} and parasitic values). This helps in choosing the network which compensates

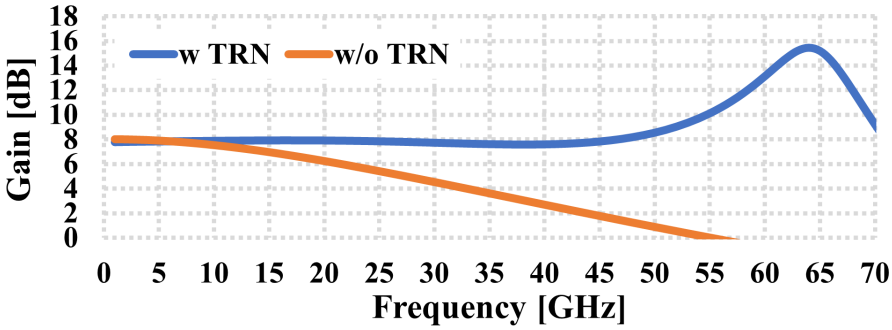


FIGURE 2.13: Second stage gain with and without the triple resonant network.

better the gain drops in frequency. Figure 2.13 reports the second stage gain with and without the designed network. The peak at high frequency is used to compensate losses coming from the previous stage, so the resulting signal amplitude level at the output of this stage is quite the same through all the bandwidth, avoiding unwanted clipping or compression.

2.4.2 Common-mode gain

A n-only schematic has been used to introduce a small amount of common-mode gain. A degeneration inductor L_{CM} has been placed between the M_1 source and the ground to reduce the CM transconductance. A zero placed at $\omega_{z,CM} = 1/R_{z,CM}C_{z,CM}$ makes the output CM impedance to be

$$r_{out,CM} = \left[\left(\frac{1}{g_{m,M3}} + \frac{1}{g_{m,M4}}\right)||\left(\frac{1}{g_{m,M2}} + \frac{g_{m,M1}}{g_{ds,M1}} \cdot j\omega L_{CM}\right)\right], \qquad (2.17)$$

which is lower than a cascode output impedance (in this case further increased by the common mode degeneration inductor).

2.5 Pre-Driver

The main driver is the biggest stage of the chain, therefore, to avoid to much bandwidth limitations coming from the input parasitic capacitances a dedicated block is placed after the gain stages. In this implementation the pre-driver is a pn source follower (Figure 2.14), exploiting in this way current reuse. To reach high f_t the transistors are biased with high current, resulting in low impedance current sources (M_2), leading to a significant attenuation in

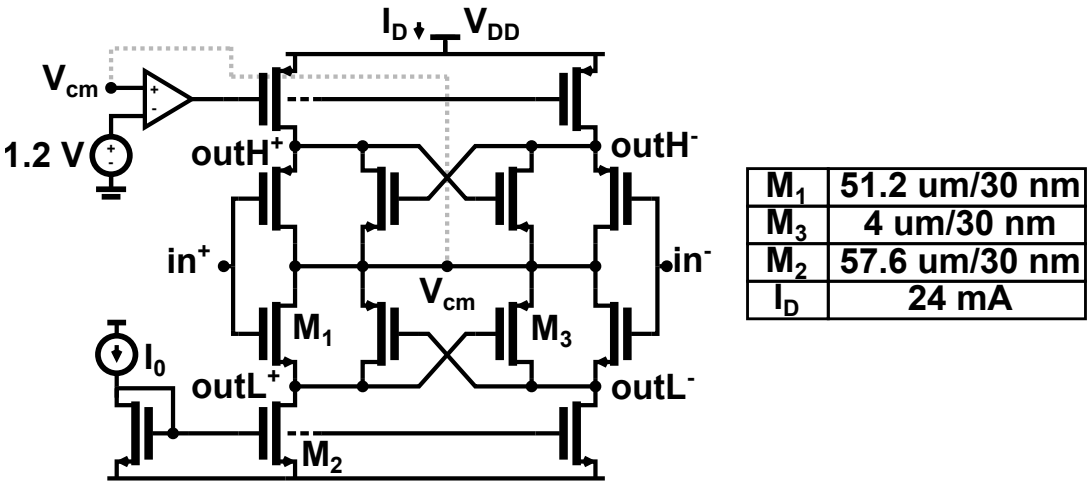


FIGURE 2.14: Pre-driver schematic

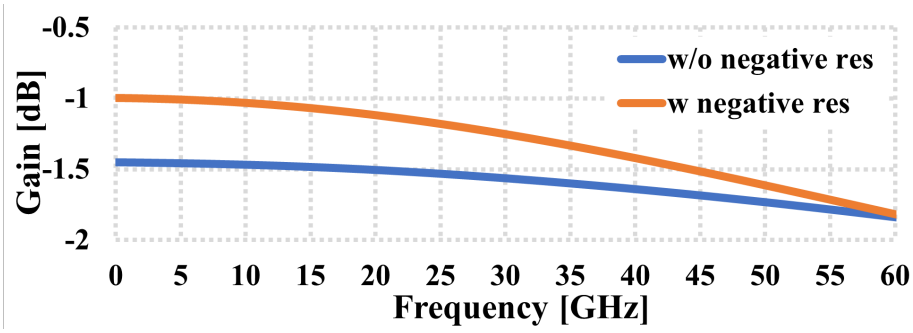


FIGURE 2.15: Source follower gain, with and without negative resistance.

the source follower. To mitigate this issue, a negative resistance is added as loading realized closing in a positive loop two transistors.

$$A_{V-n} = \frac{g_{m,M1}}{1 + \frac{g_{m,M1}}{g_{ds,M2} - g_{m,M3}}} \cdot \frac{1}{g_{ds,M2} - g_{m,M3}}. \tag{2.18}$$

From (2.18), the smaller the difference $g_{ds,M2} - g_{m,M3}$ the lower is the follower attenuation. The resulting open-loop gain can be written as

$$G_{loop} = \left(g_{m,M3} \cdot \frac{1}{g_{ds,M2} + g_{m,M1}} \right)^2 \tag{2.19}$$

To avoid a latch behaviour, the (2.19) should be always lower than one. Hence

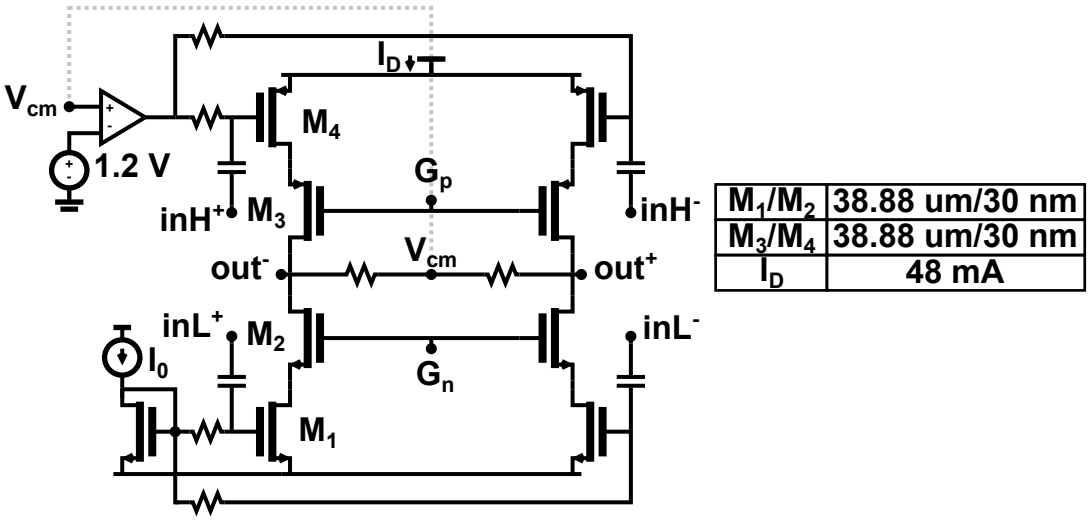


FIGURE 2.16: Main driver schematic.

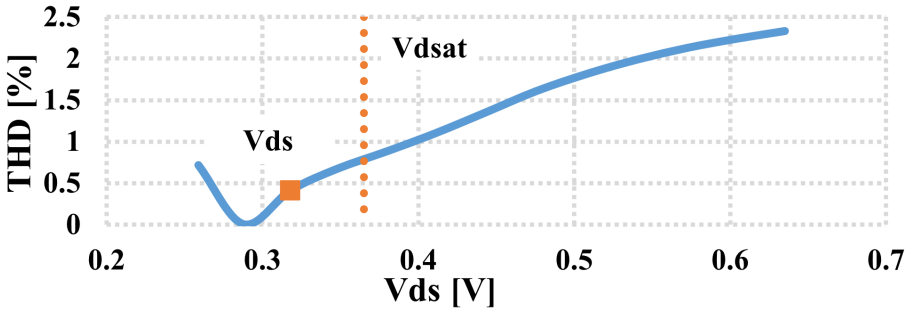


FIGURE 2.17: Common sources triode biasing distortion for 1.5 V_{ppdiff}.

stability is ensured when

$$g_{m,M3} < g_{ds,M2} + g_{m,M1}. \tag{2.20}$$

2.6 Main driver

The last stage is the one in charge to provide the driving signal for the electro-optical modulator. Here the signal amplitude is the largest through the transmitter, meaning that introducing low distortion becomes critical. The circuit shown in Figure 2.16, is a pseudo-differential pn cascoded amplifier, AC coupled

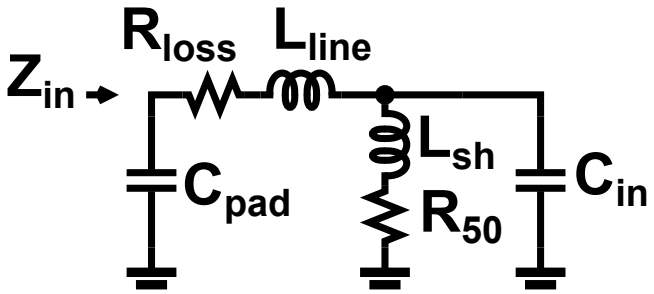
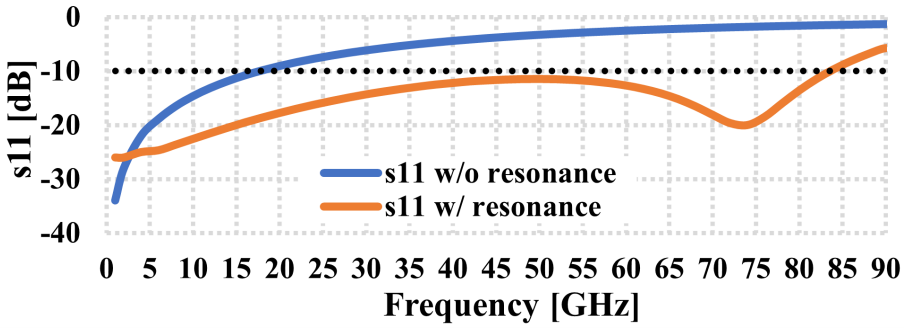


FIGURE 2.18: Input line model.

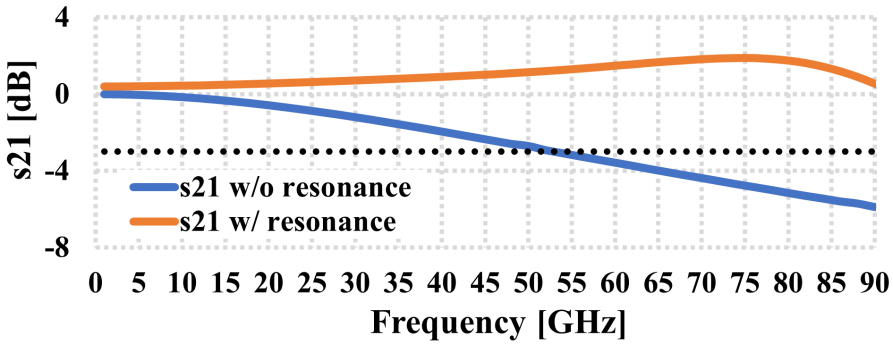
with the previous block. AC coupling allows to optimize the DC gate-to-source voltage of the common source for the best linearity. The DC current is defined by a diode connection, and the reference current is taken off-chip to have full control on this stage biasing. Figure 2.17 shows the biasing of the common sources, highlighting the better performance in term of linearity working with a V_{ds} below the triode threshold for a fixed output amplitude of 1.5 $V_{pp,diff}$.

2.7 Input line

Since we are not yet able to provide the digital part and the DAC integrated on the same die with the transmitter, broadband input matching is required. The return loss s_{11} should be lower than -10 dB over the entire design bandwidth. The matching has been realized with passive components, and it is described by the model in Figure 2.18. L_{se} is the parasitic inductance introduced by the input line, proportional to the length of the line, L_{sh} is an explicit inductor in series with the 50 Ω matching resistor. Capacitance C_{pad} models the pad and the ESD (electrostatic discharge) protections, while C_{in} is the parasitic input capacitance of the first stage. At $\omega_{se} \cong 1/\sqrt{L_{line}(C_{in}||C_{pad})}$, the parasitics resonate, making Z_{in} an high impedance. The quality factor of this resonance is reduced thanks to R_{loss}, i.e., the parasitic series resistance inversely proportional to the line width. Hence, given the parasitic capacitances C_{pad} and C_{in}, a broadband 50 Ω matching can be achieved carefully designing the input line (Figure 2.19a). While improving input matching, the input line introduces attenuation in frequency for the s_{21}, affecting the bandwidth. For this reason an explicit inductor has been placed in series with the 50 Ω matching resistor. The resulting network is a RTRN, which frequency behaviour has been described in



(a) Simulated s_{11} of the proposed model, with and without the resonance.



(b) Simulated s_{21} of the proposed model, with and without the resonance.

FIGURE 2.19: S-parameters of the input line model proposed in Figure 2.18.

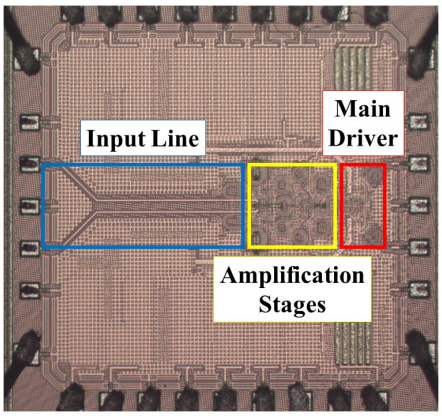


FIGURE 2.20: Fabricated die microphotography.

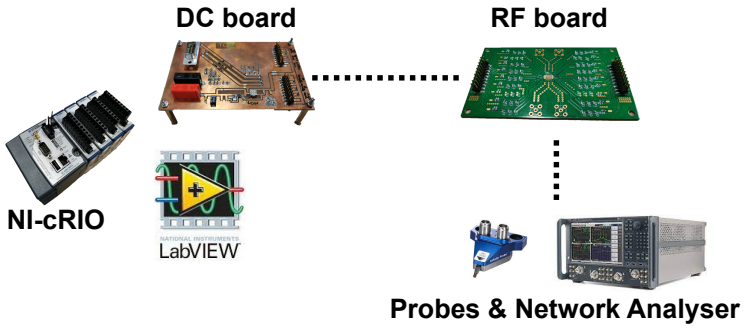


FIGURE 2.21: Measurements setup.

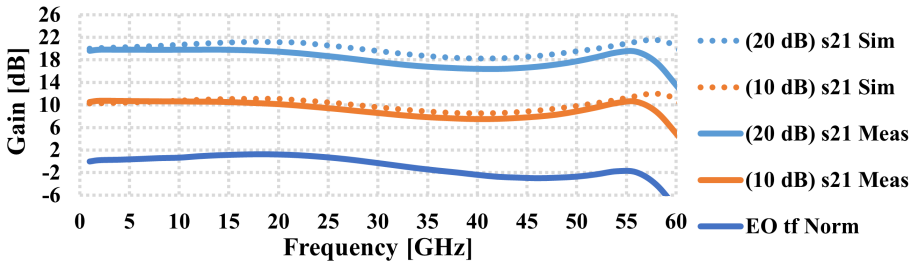


FIGURE 2.22: s_{21} measured and simulated.

a previous section, leading to a broadband s_{21} (Figure 2.19b). Hence a careful design of the input line can extend in frequency the s_{21} and the return loss as shown in Figure 2.19.

2.8 Sample measurements and validations

The proposed design has been fabricated in 28-nm CMOS TSMC-hpc+ technology. The die, shown in Figure 2.20, is a 1x1 mm^2, and it is directly mounted on a dedicated PCB. Testing has been performed using differential *Cascade Dual Infinity Probes*, with a bandwidth of 67 GHz and a *Keysight N5247B* Network Analyser. Figure 2.21 shows the setup used for testing. DC signals for biasing are provided through *CompactRIO Real-Time Controller* (National Instruments) and an auxiliary board. The CompactRIO device runs a *LabVIEW* routine, which allows to control in real-time the sample biasing. A bus cable connects these signals to the testing board and die. The radio-frequency signals come from the Network-Analyser, through the differential probes. The same setup is used both for the small and large signal tests.

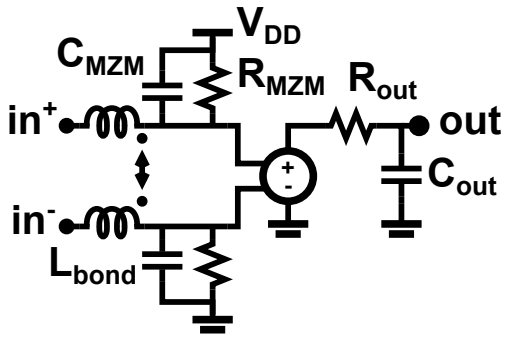


FIGURE 2.23: MZM model used as loading for the electro-optical simulation.

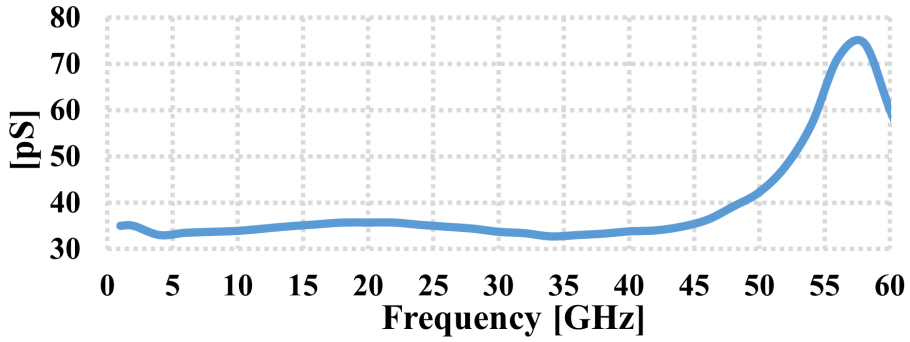


FIGURE 2.24: Measured group delay over frequency.

The measured and simulated s_{21}, reported in Figure 2.22, are in good agreement. From 10 dB to 20 dB, the transfer function shape is the same and all the values in this range can be covered thanks to the first stage continuous way programmability. The measured s_{21} variations are bounded in 3 dB up to 58 GHz, from the low to the high gain configuration. An electro-optical simulation normalized at the 1 GHz gain value is also reported, and the -3 dB bandwidth is 56 GHz. This has been simulated loading the measured device with a MZM model (Figure 2.23), where parasitics coming from bonding and the modulator itself are considered (details about parasitic sizes are not available). The group delay is not affected by gain variation, and it stays almost constant increasing smoothly by 40 pS at the band edge, as in Figure 2.24. Linearity is tested from 20 dB to 10 dB, for a fixed output swing of 1.5 $V_{pp,diff}$ at 3, 5, 7, 9 GHz. THD is always below 1.8 %, and the trend towards better distortion at lower gain is visible in Figure 2.25.

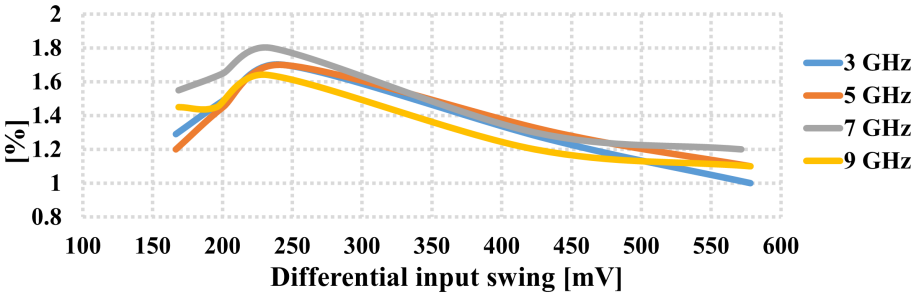
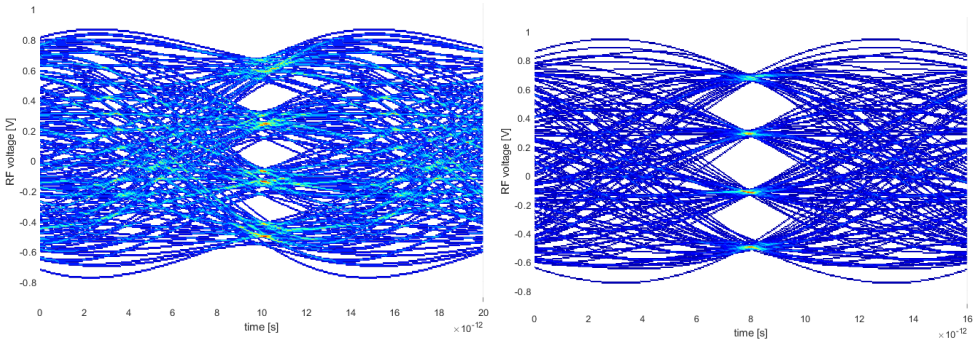


FIGURE 2.25: THD with a fixed output swing of 1.5 V_{ppdiff}.



(a) 80 GBaud, PAM-4 eye-diagram without equalization.

(b) 100 GBaud, PAM-4 eye-diagram with equalization.

FIGURE 2.26: Simulated PAM-4 eye-diagrams at the MZM model output.

The 58 GHz bandwidth makes this design suitable for data rate up to 100 GBaud. PAM-4 eye diagram simulations have been carried out for 100 and 80 Gbaud (Figure 2.26). Figure 2.26a shows that for 80 GBaud equalization is not required in order to have a good eye opening, while a feed-forward one has been used for the 100 GBaud one (Figure 2.26b). The swings are lower than the 1.5 V_{ppdiff} at the MZM input, because of the R_{MZM} used into the model. The power consumed at 20 dB is 297 mW.

Chapter 3

A MZM Driver Based on Closed-Loop Solutions

Abstract
This chapter presents a driver design based on closed-loop solutions. Given the high frequency required from the application, a closed-loop is not a straightforward solution because it trades bandwidth for other features. The following pages will show that even at such high frequencies closed-loop systems can be of help. Testing and measurements are not yet available because at the time of this dissertation the chip fabrication is ongoing. As told in the previous chapter, this design is also helpful in order to prove CMOS as viable solution in applications where SiGe-BiCMOS and InP-DHBT are dominant. The next paragraphs explain how closed-loops are used to increase the performance and in which way they have been implemented. Since measurements cannot be reported yet, post-layout simulations are considered as a proof of design functionalities and reliabilities. The output voltage swing required is 1.5 $V_{pp,diff}$ over a 50 Ω impedance. The design provides the chance of tuning the gain from 10 to 20 dB in a continuous way, with constant output amplitude. At maximum gain the power consumed is 259 mW with a single supply voltage of 2.4 V.

3.1 Closed-loop Distortion and Bandwidth

3.1.1 Distortion in closed-loop systems

Figure 3.1 shows two gain stages closed in a feedback loop through R_{fb}. The input source is $G_{m,in}$ assumed as an ideal transconductor. So the loop in Figure 2.1 can be described as a transimpedance amplifier turning I_{in} into V_{out}

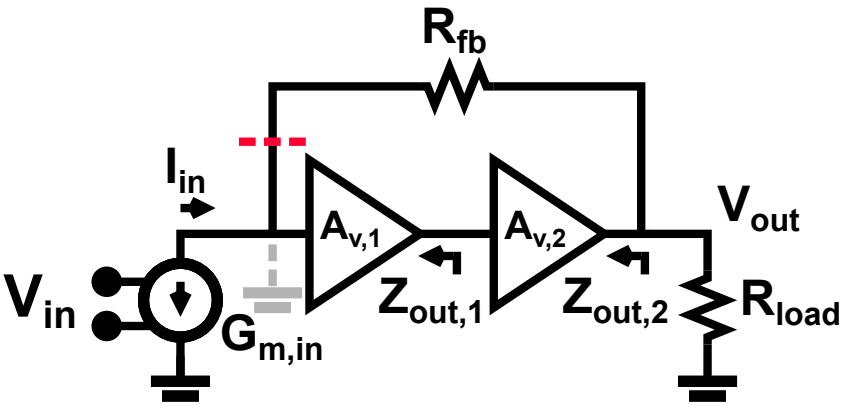


FIGURE 3.1: Two stages loop implementation

through the feedback resistor R_{fb}. The open loop gain G_{loop} is defined by $A_{v,1}$ and $A_{v,2}$, while the closed loop gain from V_{in} to V_{out} is

$$\frac{V_{out}}{V_{in}} = G_{m,in} \cdot R_{fb} \cdot \frac{G_{loop}}{1 + G_{loop}}. \tag{3.1}$$

Designing G_{loop} to have a DC gain of 30 dB means that the (3.1) can be written as $0.96 \cdot G_{m,in} \cdot R_{fb}$, so mostly defined by $G_{m,in}$ and R_{fb}. $A_{V,1}$ and $A_{V,2}$ can be described with the non-linear model reported in Figure 2.1 in the previous chapter, in order to better understand how the distortion behaves in a closed-loop scheme. The spurious voltage components introduced by each stage are defined as

$$V_{out,i} = I_{out,i} \cdot Z_{out,i} \tag{3.2}$$

$$= (I_{gm,i} + I_{gds,i}) \cdot Z_{out,i}. \tag{3.3}$$

where i identifies the term at the frequency ω_{in}, $2\omega_{in}$, ..., $n\omega_{in}$, and ω_{in} is the frequency of the input tone. From the (3.3), it can be noticed that each components is defined by I_{out} and Z_{out} at the considered spurious frequency. Hence, having $\omega_{in} = 1GHz$, $V_{out,3}$ can be written as

$$V_{out}(3GHz) = I_{out}(3GHz) \cdot Z_{out}(3GHz), \tag{3.4}$$

meaning that a spurious component can be reduced either lowering the current or the output impedance at the spurious frequency. As explained in the previous chapter, all the contributors in the amplifier model presented in Figure 2.1 can

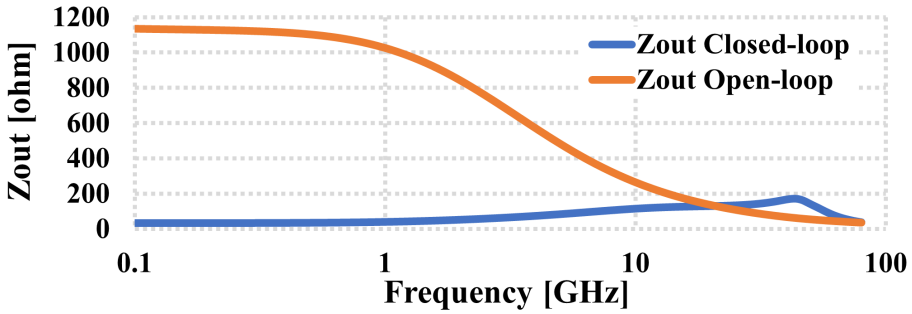


FIGURE 3.2: Open-loop and closed-loop output impedance

be defined. While the distortion coefficients $I_{gm,i}$ and $I_{gds,i}$ can be considered the same in the open-loop and closed-loop cases, this is not true for the output impedance. Figure 3.2 shows the output impedance Z_{out} of the first stage when the loop in Figure 3.1 is open and closed (breaking the loop on the red dashed line). A strong impedance reduction happens when the loop is closed, and the closed-loop impedance can be defined as

$$Z_{out,closed-loop} = \frac{Z_{out,open-loop}}{1 + G_{loop}}. \tag{3.5}$$

Hence, until the loop can be considered *closed* (a G_{loop} high enough), the impedance at each node of the loop is reduced. This together with the (3.3), results in an amplitude attenuation of the spurious components [18]. Assuming the third harmonic to be the heaviest distortion contributor in the THD computation, the loop should be closed up to $3\omega_{in}$, where ω_{in} is the highest fundamental component meaningful to asses the transmitter linearity behaviour.

3.1.2 Bandwidth in closed-loop systems

The gain contribution of the first and second stage in Figure 3.1 can be written as

$$A_{V,1}(\omega) = \frac{A_{0,1}}{1 + \frac{s}{\omega_1}}, \tag{3.6}$$

$$A_{V,2}(\omega) = \frac{A_{0,2}}{1 + \frac{s}{\omega_2}}, \tag{3.7}$$

where $A_{0,1}$, $A_{0,2}$ are the low frequency gain and ω_1, ω_2 are the real poles introduced. The G_{loop} can then be simplified as

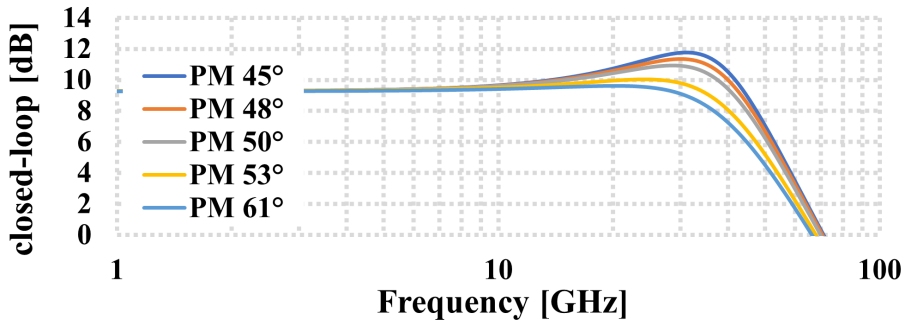


FIGURE 3.3: Closed-loop transfer function at different phase margin value

$$G_{loop} = \frac{A_{0,1}A_{0,2}}{1 + s\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right) + \frac{s^2}{\omega_1\omega_2}}. \tag{3.8}$$

This holds assuming the current source of Figure 3.1 to be ideal, hence an high impedance. If this is not true, the G_{loop} experiences an attenuation based on the impedance divider between R_{fb} and the current source output impedance. The two poles in the (3.8) if properly designed can be exploited to enhance the closed-loop bandwidth. Considering again Figure 3.1, the closed-loop transfer function from V_{in} to V_{out} can be defined as

$$\frac{V_{out}}{V_{in}} = G_m R_{fb} \cdot \frac{A_{0,1}A_{0,2}}{A_{0,1}A_{0,2} + 1} \cdot \frac{1}{1 + \frac{s}{A_{0,1}A_{0,2}+1}\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right) + \frac{s^2}{\omega_1\omega_2(A_{0,1}A_{0,2}+1)}}. \tag{3.9}$$

If ω_1 and ω_2 are close to each other, from real they become complex poles, introducing in this way an overshoot in the closed loop transfer function. This overshoot can be described as the complex poles Q, approximated by

$$Q \cong \frac{\sqrt{\omega_1\omega_2(A_{0,1}A_{0,2} + 1)}}{\omega_1 + \omega_2}, \tag{3.10}$$

which defines the amount of peaking introduced in the transfer function. This happens at a frequency close to ω_0, which in turn is defined as

$$\omega_0 = \sqrt{\omega_1\omega_2(A_{0,1}A_{0,2} + 1)}. \tag{3.11}$$

From the loop stability point of view, moving the two poles to be close to each other means reducing the phase margin (PM). For instance, if the poles are placed at the same frequency, the phase shift introduced would make the

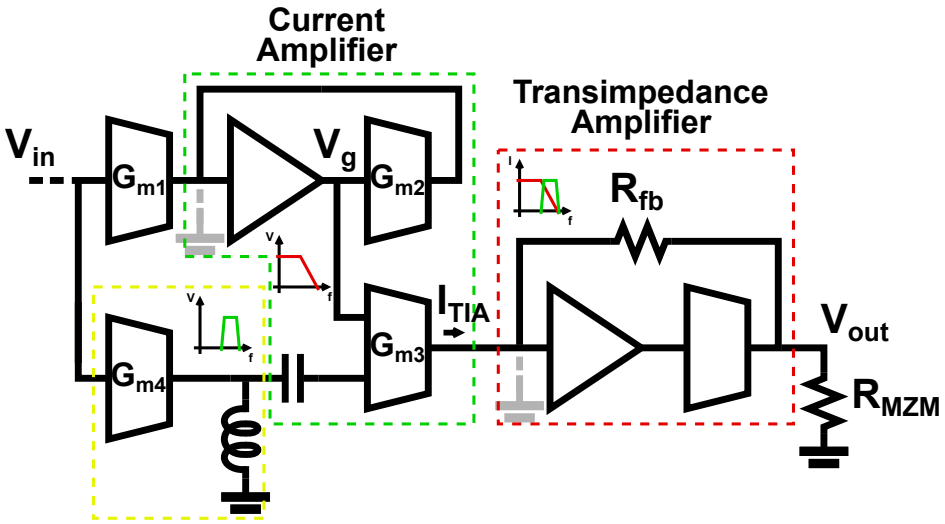


FIGURE 3.4: Proposed transmitter block diagram.

system to oscillate. This trade-off between PM and bandwidth is graphically explained in Figure 3.3. Here the bandwidth is increased by a 20 % from a PM of 61° to a PM of 45°.

3.2 Transmitter block diagram

The proposed design tried to exploit closed-loop features to provide a more linear signal and a wider bandwidth. Figure 3.4 shows a block diagram where the loops are highlighted. The input signal, here defined as V_{in}, drives a first transconductor G_{m1}, which turns the voltage into a current. Since the signal is at the beginning of the chain, the voltage amplitude is small and the amount of distortion introduced by this V/I conversion is poor. A loop designed as a two stages is showed in the green dashed box. The virtual ground provided by this loop increase the linearity of the G_{m1} V/I conversion. Since the null voltage amplitude at this node, the g_{ds} distortion contribution is cancelled out. The current provided by G_{m1} flows into the low impedance provided by G_{m2}, generating a voltage swing at V_g defined as

$$V_g = V_{in} \cdot \frac{G_{m1}}{G_{m2}}. \tag{3.12}$$

This holds until the loop can be considered closed. The (3.12) voltage is then turned into a current through G_{m3}. Since G_{m3} is driving a closed-loop tran-

simpedance amplifier, at its own output a virtual ground can be found. So, G_{m2} and G_{m3} experience the same voltage swing both at the input and at the output, calling back the behaviour of a current mirror, where the mirror ratio is defined by G_{m3}/G_{m2}. The current delivered to the output transimpedance amplifier can be written as

$$I_{TIA} = V_g \cdot G_{m3} \tag{3.13}$$

$$= V_{in} \cdot \frac{G_{m1}}{G_{m2}} \cdot G_{m3}. \tag{3.14}$$

The last loop is a TIA, loaded by the MZM impedance R_{MZM}. The analysis of this loop is the same as the one already done for the Figure 3.1. It is a two stages loop closed in feedback through R_{fb}. The transimpedance gain is defined by R_{fb} while the loop is closed, so the overall low frequency transmitter gain, can be defined as

$$\frac{V_{out}}{V_{in}} = R_{fb} \cdot \frac{G_{m1}}{G_{m2}} \cdot G_{m3}. \tag{3.15}$$

In parallel with this path, an high frequency signal is injected as a current into the TIA through G_{m3}. To have a *narrowband* high frequency signal, the transconductor G_{m4} is loaded with an inductor. The resulting I_{TIA} is defined by a low frequency path when all the loops are closed, and a narrowband high frequency component.

3.3 Transconductor G_{m1}

The input transconductor is an inverter-like structure, which allows to have two times the transconductance for the same biasing current. AC coupling allows to spare voltage head-room, in this way a common gate can be used both for p- and n-side. The 10 dB gain variation is provide by this stage, varying the overall transconductance by pushing in triode M_1 and M_4. As in the previous design, the gain is hand controlled by taking off-chip G_p and G_n. As already explained in the previous chapter, cascoded structure with common source in triode helps in reducing the amount of spurious components. Future steps include the design of an electro-optical loop capable to detect peak and automatically adjust the gain (even for the high frequency as reported in the next sections).

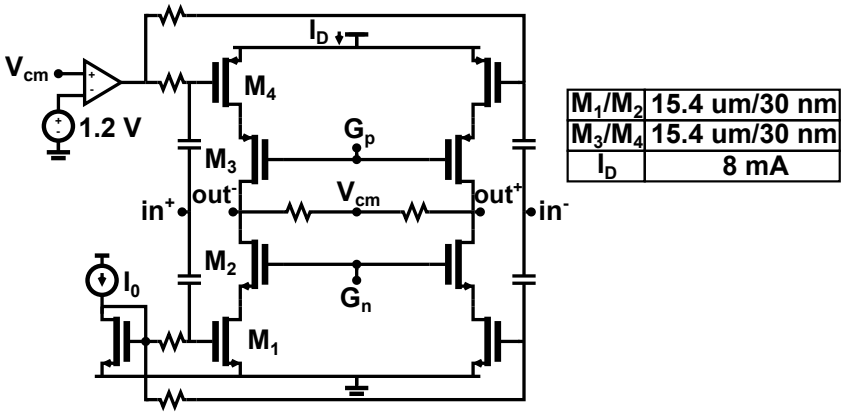


FIGURE 3.5: Transconductor G_{m1}.

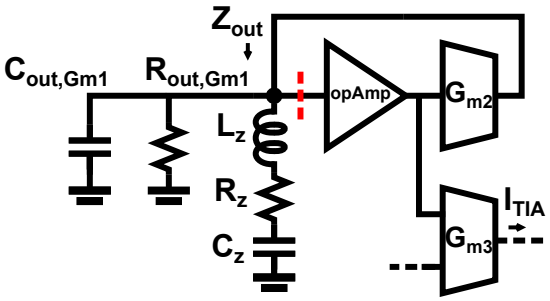


FIGURE 3.6: Closed-loop current amplifier.

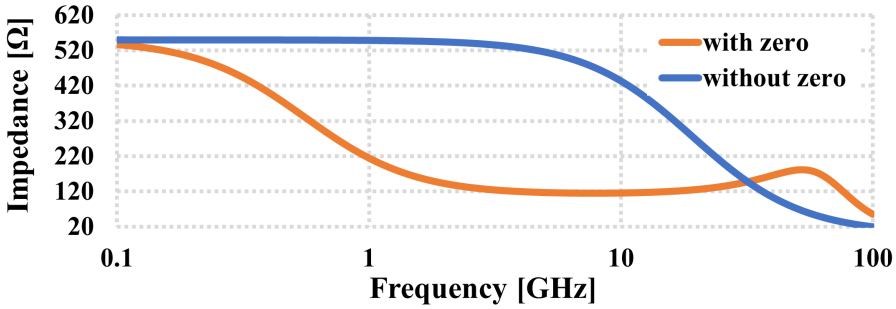


FIGURE 3.7: Z_{out} with and without the zero.

3.4 Closed-loop Current Amplifier

The first amplification stage is in the current domain, as highlighted in the green box of Figure 3.3. Working in current avoids to have large voltage swings,

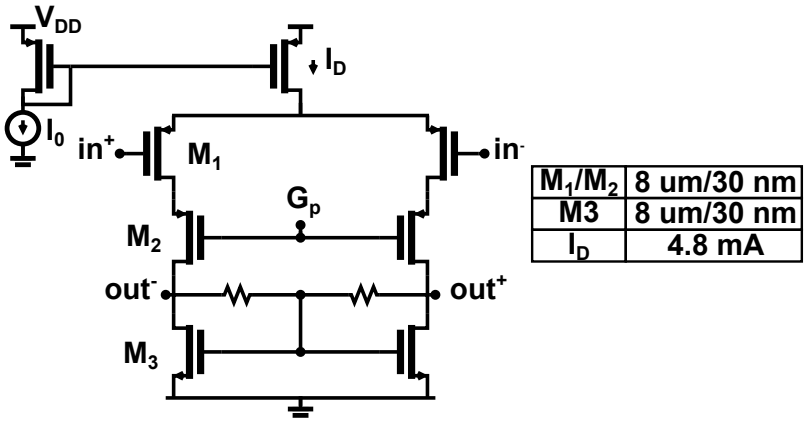


FIGURE 3.8: First stage Operational amplifier.

preventing in this way unwanted current modulations. The proposed loop is defined by two stages, in order to have enough G_{loop}. While the loop is closed all the current provided by G_{m1} is sinked into G_{m2}. An insight of the designed loop is reported in Figure 3.6, and here it can be noticed that in order to have a wide unity gain bandwidth (UGBW) and stability, a zero is introduced through L_z, R_z and C_z, avoiding any compensation capacitor. $R_{out,Gm1}$ stands for the G_{m1} output impedance, which loads G_{m2} in parallel with the zero. Since G_{m1} is a cascode, the output impedance $R_{out,Gm1}$ is very high. The introduced zero reduces this value to $R_{out,Gm1}||R_z$, for frequencies above $1/(R_zC_z)$, making the loop stable. Furthermore, choosing L_z in order to have $1/\sqrt{L_zC_z}$ lower than $1/(R_{out}||R_z)C_{out}$, results in an impedance peak at high frequencies. An this can be exploited to increase the UGBW while preserving the stability. The behaviour of Z_{out} described so far is reported in Figure 3.7. The designed loop has 30 dB of DC gain, an UGBW of 15.22 GHz and a phase margin of 68.9°.

3.4.1 Operational Amplifier

The first stage of the loop is an operational amplifier (Figure 3.8). The input is on the p-side, to allow DC coupling with the previous stage. The active load is realized through M_3 which also set the biasing for the following stages, G_{m2} and G_{m3}. G_p is generated from a resistive divider inside the chip.

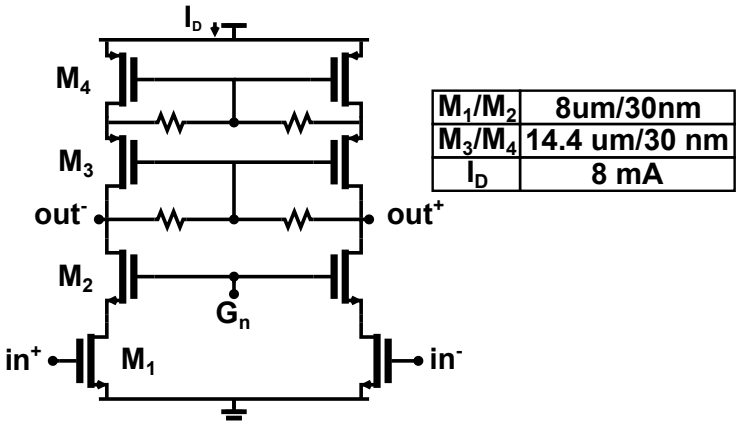


FIGURE 3.9: Second stage, transconductor G_{m2}.

3.4.2 Transconductor G_{m2}

The second stage of the loop is an n-only amplifier with an active load reported in Figure 3.9. It is DC biased with the previous one, while the n-side common gates are biased through an internal resistive divider through G_n. The p-side is also a cascode and the common mode diode connections allow to have self-biasing. These diode connections reduce the common mode gain avoiding instability given the CM positive loop. The output is shared with G_{m1}, which CM loop set the DC value at this node, avoiding large voltage drift due to process and corner variations. While the gain provided by the operational amplifier and G_{m2} is larger than zero this loop can be considered as a diode connection, in which all the current injected by G_{m1} flows into G_{m2}, and given the virtual ground the output node is not allowed to move. To accommodate this injected current, at the input of G_{m2} a voltage is generated, with an amplitude given by the ratio between the signal current and the transconductance provided by M_2.

3.4.3 Transconductor G_{m3}

The gates of G_{m2} are connected to the M_1/M_2 gates of G_{m3}. The ratio between the transistor size defines the gain of the closed-loop current mirror which in this case is 2.5. In Figure 3.10 the p-side is shaded because from the signal point of view it is responsible of the high frequencies. The n-side is responsible of the current mirroring with G_{m2}. The output of this stage loads the following TIA open-loop gain, the high output impedance introduced by cascoding both the p- and n-side reduce the impedance divider with the feedback resistor R_{fb}.

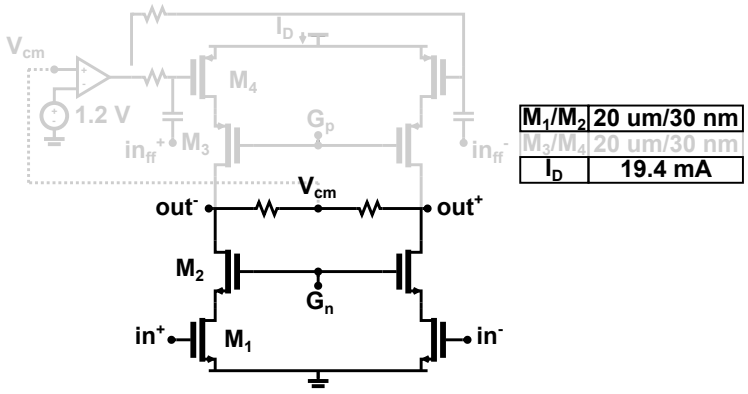
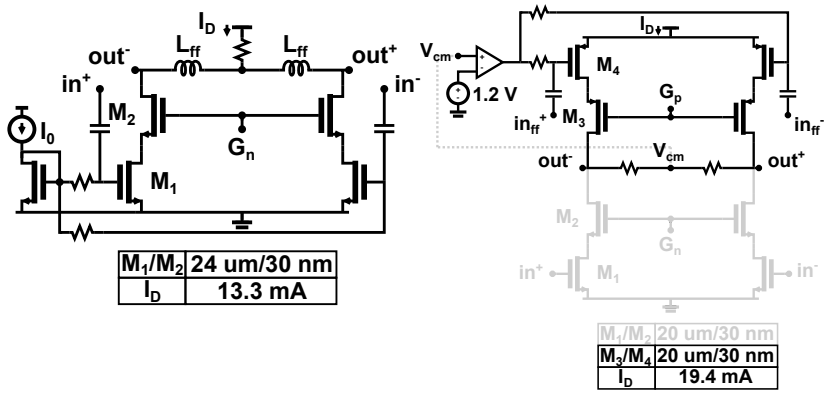


FIGURE 3.10: Transconductor G_{m2}.



(a) Feed-forward amplifier.

(b) High frequency side of transconductor G_{m3}.

FIGURE 3.11: VGA third harmonic component versus gain.

3.5 Narrowband High Frequency Amplifier

To meet the bandwidth requirements, besides the extension resulting from the closed-loop phase margin a feed-forward path has been introduced. The input of this amplifier is the same as G_{m1}, then the amplified signal is injected through G_{m3} as a current into the TIA. The schematic reported in Figure 3.11a is an n-only amplifier loaded with differential inductors. The narrowband gain can be described as

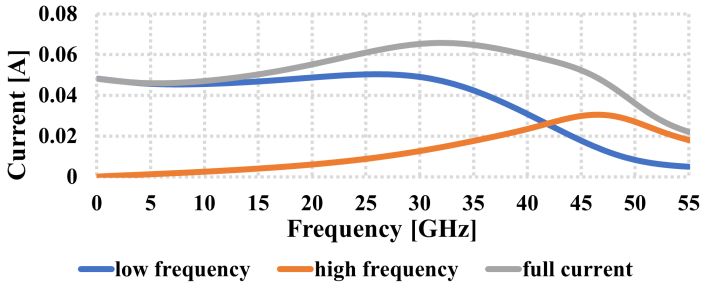


FIGURE 3.12: Currents flowing into the out TIA over frequency.

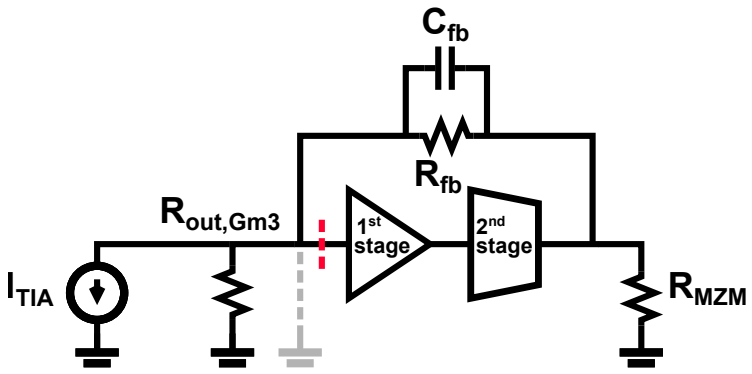
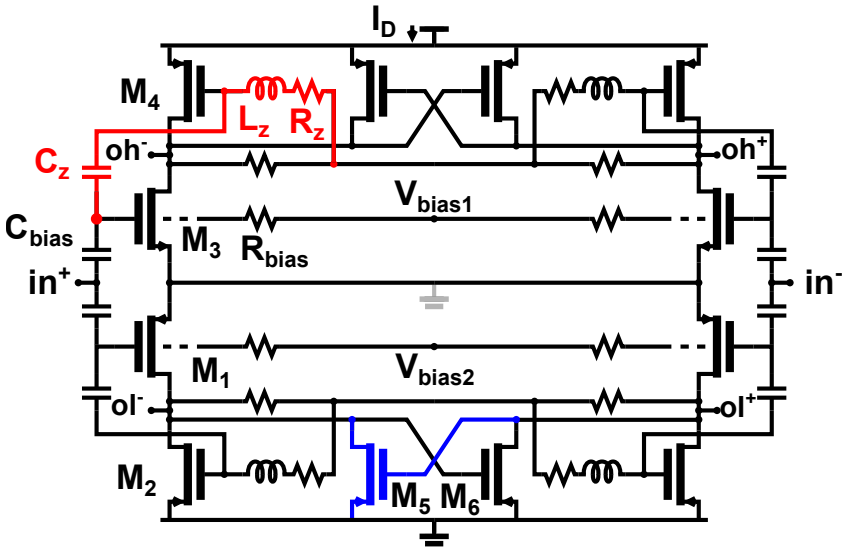


FIGURE 3.13: Output TIA.

$$A_{V,ff}(s) = g_{m,M1} \cdot \frac{sL_{ff}}{1 + s^2 C_{par} L_{ff}}, \tag{3.16}$$

so it increases with frequency until L_{ff} resonates with the parasitic capacitances. To control the magnitude of the (3.16), G_n is taken off-chip, in this way changing the working region of M_1 from saturation to triode modulates the stage transconductance. This allows to control the high frequency gain to have flat transfer function through all the gain configurations. A n-only solution has been preferred to the inverter-like one to reduce the common-mode injection at high frequency. The narrowband signal at the inductor outputs is then injected as a current through M_4 of G_{m3} as shown in Figure 3.11b. The current flowing into the output TIA can be described with a low and an high frequency components as shown in Figure 3.12, and the resulting magnitude is the sum of the two contributors.



M_1/M_3	8 um/30 nm
M_2/M_4	4.5 um/30 nm
M_5/M_6	2 um/30 nm
I_D	7 mA

FIGURE 3.14: TIA 1st stage schematic.

3.6 Output TIA design

The last stage performs the output I/V conversion, providing the required swing to the modulator. Here the amplitude of the signal is the largest and the linearity is critical. To ensure all the specifications together with the bandwidth a TIA is proposed and reported in Figure 3.13. It is a two stages loop, in which the MZM loads a loop inner node. This impose a strict constrain on the MZM impedance that can be driven by this solution. Changing R_{MZM} involves a different loop behaviour affecting the stability and the UGBW. For this reason, this design is thought for a 50 Ω load (also for testing purposes, considering 50 Ω terminated instrumentations). To further extend the UGBW keeping the loop stability, several zeros are used. From Figure 3.13 one can be recognized on the feedback branch, and it is effective at frequencies above $1/R_{fb}C_{fb}$. The open loop gain is 30 dB, with 26 GHz as UGBW and a PM of 46°.

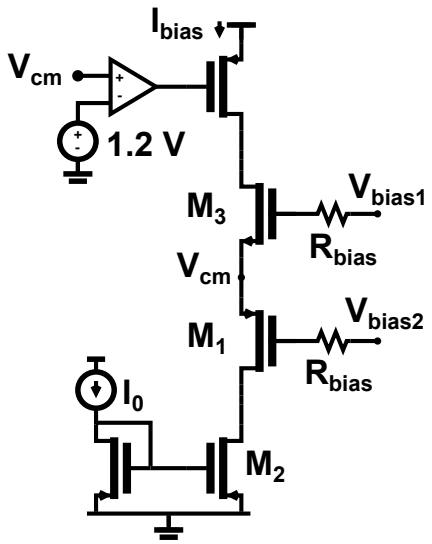


FIGURE 3.15: Biasing replica.

3.6.1 TIA 1st stage

The 1st stage amplifier, reported in Figure 3.14, is a stacked solution of two amplifiers with a virtual ground for the signal in the middle. The upper and lower side inputs are respectively defined by a n-MOS and p-MOS differential pairs. AC coupling helps to fit all the transistors into the supply voltage avoiding devices in triode or switched-off. The biasing is defined by a scaled replica of the branch, in which a scaled version of the current I_D flows and defines the V_{gs} of M_1 and M_3 (Figure 3.15).
These two stacked amplifiers allow to have two outputs at different DC levels, which are used for the biasing of the following stage. The supply voltage is 2.4 V and it is shared between the two amplifiers, so the available voltage for each one is 1.2 V. To increase the gain without increasing the supply voltage a negative resistor is used in parallel with the load, and it is highlighted in blue in Figure 3.14. Considering the lower side, the DC gain can be then written as

$$A_V = g_{m,M1} \cdot \frac{1}{g_{ds,M1} + g_{ds,M2} + g_{ds,M5} - g_{m,M5}}, \tag{3.17}$$

showing an higher output impedance thanks to $g_{m,M5}$. The biasing of this extra transistor costs a small amount of DC current. This negative resistor is realized closing in a positive loop M_5 and M_6, introducing metastability concerns. The loop gain of these two transistors, considering the same biasing current and

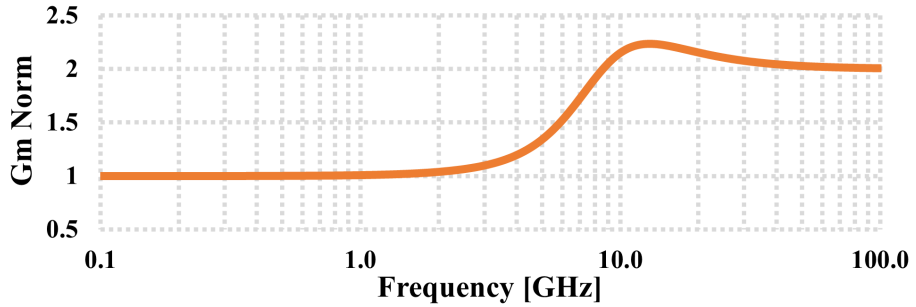


FIGURE 3.16: TIA 1st stage, transconductance normalized to g_m ($g_{m,M3/M4}$).

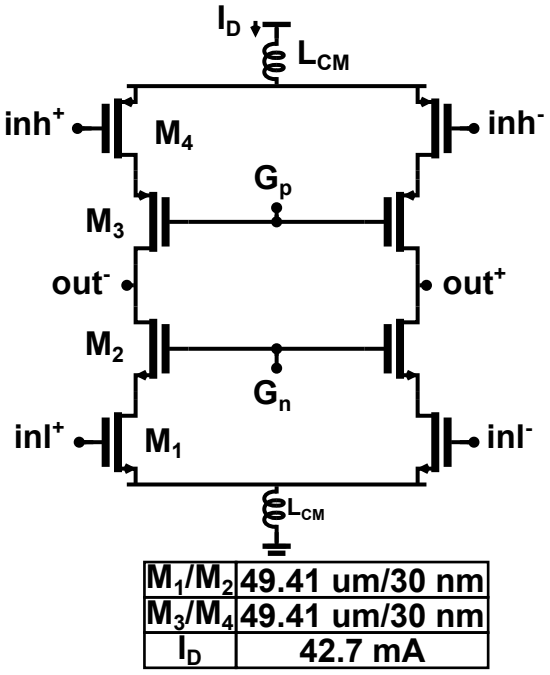


FIGURE 3.17: TIA 2nd stage schematic.

transistor size, can be defined as

$$G_{loop,M5/M6} = \left(\frac{g_{m,M5}}{g_{ds,M5} + g_{ds,M2} + g_{ds,M1}} \right)^2. \tag{3.18}$$

A latch condition will happen when $G_{loop,M5/M6}$ is larger than one, so the condition to be satisfied in order to avoid this becomes

$$g_{m,M5} < g_{ds,M5} + g_{ds,M2} + g_{ds,M1} \tag{3.19}$$

To increase the UGBW while maintaining enough phase margin a zero has been introduced in this stage, highlighted in red in Figure 3.14. Considering $g_{m,M3}$ and $g_{m,M4}$ to be the same and equal to g_m, the upper side transconductance becomes

$$g_m(s) = g_m\left(1 + sC_zR_z \cdot \frac{1 + s\frac{L_z}{R_z}}{1 + sC_zR_z + s^2C_zL_z}\right), \tag{3.20}$$

where moving at higher frequencies a zero at $1/R_zC_z$ can be found, then two complex poles at $1/\sqrt{C_zL_z}$, and finally a real pole at R_z/L_z. The transconductance frequency behaviour normalized to g_m is reported in Figure 3.16. It can be noticed that at low frequency the overall transconductance is g_m, while at high frequency it becomes $2 \times g_m$. Furthermore, if the complex poles are placed closed to the open-loop unity gain frequency, the peaking resulting from Figure 3.16 results in a UGBW extension.

3.6.2 TIA 2nd stage

The 2nd stage is an inverter based transconductor biased by the two different DC voltages provided by the previous stage. The schematic is reported in Figure 3.17. The common gate voltage G_p and G_n are generated from a resistive divider inside the chip. This stage should be capable to provide enough current to generate the required swing around the feedback resistor R_{fb} and to drive the R_{MZM} load coming from the modulator. R_{MZM} load the output of this stage, which happens to be inside the loop. This does not allow, or makes very difficult the chance to drive several value of R_{MZM}. So for this case, since all the testing would be performed with 50 Ω terminated instrumentations, the loop is designed to work properly with R_{MZM} equal to 50 Ω.

3.7 Design Simulations

Since a fabricated sample is not already available, in this section simulations are reported to prove the proposed design performance. The technology used for the fabrication is a 28-nm CMOS TSMC-hpc+ technology. The following results regard post-layout simulations. Figure 3.18 shows the s_{21} for different gain configurations, from 20 to 10 dB. As already introduced the gain can be tuned in a continuous way, with full control over the low and high frequency shares. For all the gain values the transfer function results to be flat, with

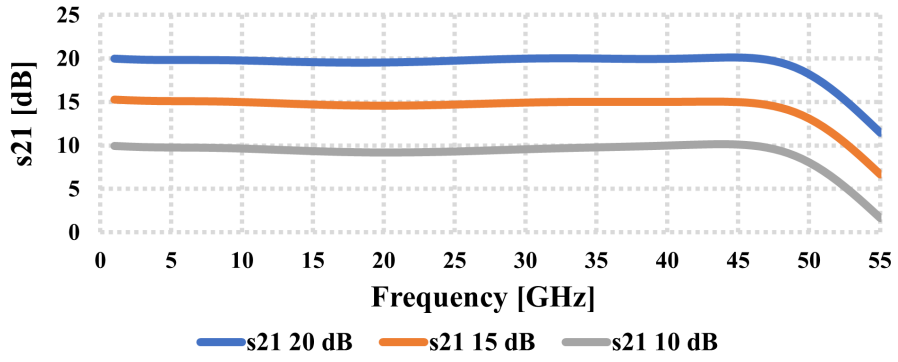


FIGURE 3.18: Simulated s_{21} for different gain configurations.

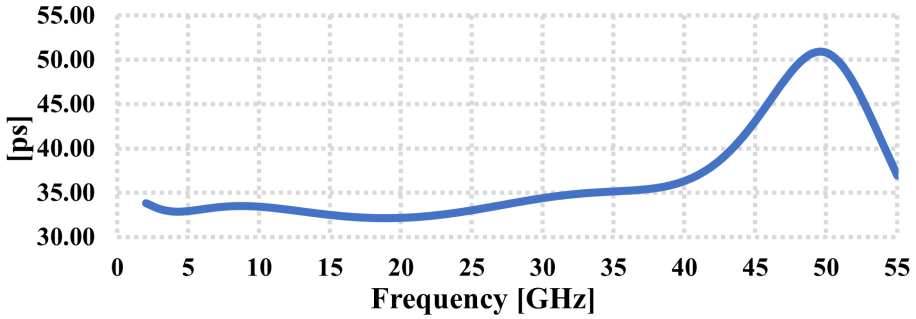


FIGURE 3.19: Simulated group delay over frequency.

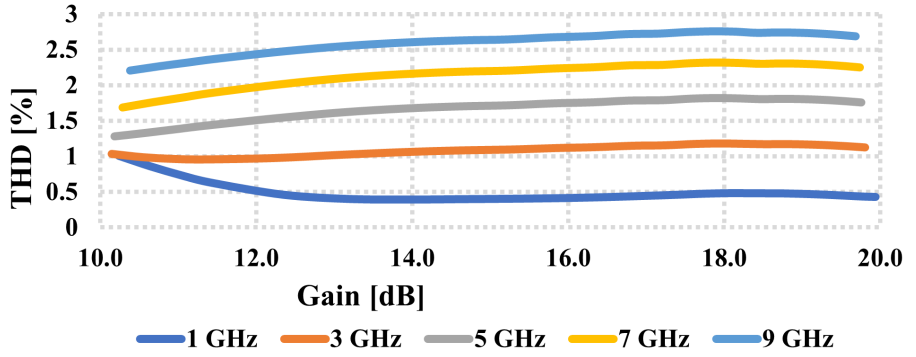
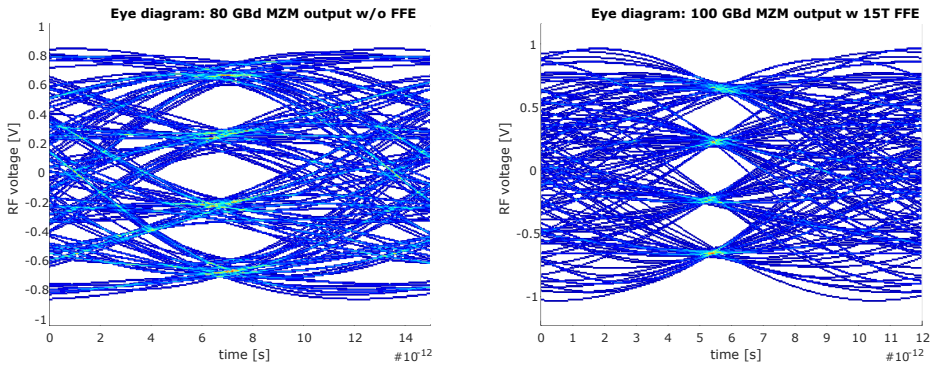


FIGURE 3.20: THD with a fixed output swing of 1.5 V_{ppdiff}.



(a) 80 GBaud, PAM-4 eye-diagram without equalization.

(b) 100 GBaud, PAM-4 eye-diagram with equalization.

FIGURE 3.21: Simulated PAM-4 eye-diagrams at the MZM model output.

almost 0 dB fluctuation, while the -3 dB cut-off frequency is always above 51 GHz. Group delay is flat up to the band edge, where a smooth 15 pS variation happens as reported in Figure 3.19. The linearity is tested at fixed output swing of 1.5 $V_{pp,diff}$, from low to high gain and for 1, 3, 5, 7 and 9 GHz input signals. Results are reported in Figure 3.20, and a poor distortion can be appreciated for the lower frequency tones where the loop are still closed also for the higher harmonic components. Using the transconductor G_{m1} in triode to lower the gain keeps the distortion constant while increasing the amplitude involved. PAM-4 eye diagram simulations have been performed for 80 and 100 GBaud data rates, as reported in Figure 3.21. For the 80 GBaud test (Figure 3.21a) a good eye opening is achieved without equalization, while equalization is required for the 100 GBaud (Figure 3.21b). Power consumption for the 20 dB gain configuration is 257 mW, while for the 10 dB it reaches 229 mW.

Conclusions

The focus of this thesis is to prove that CMOS, more in general, scaled technologies, are viable solutions in coherent optical application. In the field of long reach communication, the dominant technologies are BiCMOS and SiGe, which provides higher breakdown voltages and transconductance efficiency. The main benefits in introducing scaled technologies, is the chance to lower the cost and increase the integration between the digital, the analog and the optical domain. Having digital and analog functionalities co-packaged or even on the same die can be really cost effective. In order to make this possible, digital oriented technologies should replace analog based one. The first step towards this aim is to prove CMOS as an effective candidate (the final target would be to have everything integrated in FinFET technology). Regarding the optical side, Silicon-photonic is emerging as solution but still, integration on the same die of the electronic and optical part is not available. Instead, co-packaging through flip-chip solutions show very good performance (no need of matching is an example) and lower costs. So this dissertation is just the first step of a longer journey.

The transmitter in Chapter 2 is a first attempt to prove CMOS technology. The structures and schematics proposed in this design are quite simple and easy to understand. A different approach for the gain variability has been introduced and tested. This is based on moving transistor from saturation to triode in order to reduce the transconductance and to make the V/I conversion more linear. This results in a trend for the linearity which is better for larger swing. This first chip has been electrically characterized, and the performance are comparable and even better than several SiGe or BiCMOS works reported in the state of the art of Table I. The only CMOS design to our knowledge is reported in [19], where amplitude, bandwidth and linearity are in our favour. Unfortunately we are not yet able to provide eye-diagram or optical measurements, but a fair comparison can be done with [19]. They provide an electrical bandwidth around 48 GHz which becomes 43 GHz when loaded by a

MZM, so a 10% reduction. We reach 58 GHz of electrical bandwidth (applying the behavioural model provided by the company the electro-optical bandwidth turns to be 55 GHz), assuming the same 10% degradation it results 52 GHz. The linearity behaviour provided is constant over frequency and always below 1.8% for all the gain configuration, making this feature competitive with the 2.2% provided by [19]. The eye opening reported in Figure 2.26a and Figure 2.26b suggests that a PAM-4 modulation at 80-GBaud can be performed (simulations and measurements are in good agreement for all the others electrical parameters). Given all these assumptions we belive that a 64-GBaud 16QAM can be performed by the chip fabricated ([19] successfully reports a 64-GBaud dual polarization 16-QAM). [20] and [21] propose solutions based on lumped stage fabricated respectively in a 130 nm and 55 nm SiGe technology, while [22] shows a distributed toplogy realized in 250 nm InP DHBT. In order, the f_t of these processes are, 250 GHz, 330 GHz and 400 GHz, while for the 28 nm CMOS is 240 GHz. It is not wise to bias a CMOS at the f_t peak because it means a g_m/I_D lower than 3, so a lot of current is involved to provide gain leading to a metal routing which will be the bandwidth bottleneck. The highest f_t that we are able to reach is 200 GHz. With these assumptions, we can state that the circuital solution that we proposed is very interesting in terms of bandwidth. About linearity and output swing it is not easy to have a comparison. Because of the device reliability, with our technology it is very dangerous to go above 2.4 V as a supply voltage and in turns also the output swing would be limited. For this reasons making a distortion comparison with different swing amplitudes would not be fair.

In Chapter 3, a different kind of approach is reported. For this design measurements are not yet available, because at the time of this thesis the chip fabrication is on going. This design is based on closed-loop solutions, in which usually bandwidth is traded with other features, in this case linearity. Exploiting loops with very high frequency unity gain bandwidth (tens of GHz), distortion compression is performed in order to provide a linear output signal. Still the transmitter overall bandwidth can be considered competitive, thanks to the complex poles introduced by the closed-loop systems and a parallel high frequency narrowband path. This transmitter is designed to be tested electrically, so for specific 50 Ω load impedance (instrumentation loading). The next step for such a design would be the chance to have different loading as the one provided by a Mach-Zehnder modulator.

To conclude, we can state that CMOS can be exploited in long reach coherent optical link and it can be competitive with already established technology.

	Chapter 2	Chapter 3	ISSCC 2020 [19]	ISSCC 2019 [20]	IMS 2017 [21]	IMS 2016 [22]
Technology	28 nm CMOS	28 nm CMOS	65 nm CMOS	130 nm SiGe BiCMOS	55 nm SiGe BiCMOS	0.25 μm InP DHBT
Electrical BW [GHz]	58	58	48	40	57.5	67
Gain(1GHz) [dB]	10-20 (continuous)	10-20 (continuous)	13-22.5	20-30	18.8	0.9-10.7
Supply [V]	2.4	2.4	2.6	3.6	2.5/3.3/6	5
THD [%]	1.8	0.5 (1 GHz)	2.2	3.6	6	-
P_{dc} [mW/Ch]	297	257	225	1000	820	840
Diff. Out Swing [V]	1.5	1.5	1.5	6	6	1.8
Integrated Noise (80GHz) [mV_{rms}]	3.28 (20 dB) 2.89 (10 dB)	-	-	-	-	-

TABLE 3.1: Comparison with State of the Art.

The benefits are not just related to the cost effectiveness but also in terms of performances. The future steps would be testing into an electro-optical system the proposed designs, to provides a BER with all the impairments introduced by an optical link. While from the design point of view beginning the studies of FinFET prototypes in which digital and analog sides are merged together. This technology is not suitable for long reach applications because of the limitation already faced with CMOS (swing required by MZM modulator, extreme value of f_t, ...). While it provides advantages in short reach communication as data-center applications (involving complex modulations). Here the integration between analog front-end and digital functionalities has a paramount importance, while bandwidth and swing performance are relaxed. So a transmitter would turn to be a sort of DSP followed by a power DAC, in which the driving features (swing, speed, linearity, ...) are performed by the digital-to-analog converter itself.

Bibliography

[1] Cisco, "Cisco Annual Internet Report (2018-2023) White Paper," https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html.

[2] Huawei, "Communications Network 2030," https://www.huawei.com/en/giv/communications-network-2030.

[3] P. Ossieur, H. Ramon, J. Lambrechts, M. Vanhoecke, L. Breyne, S. Zhou, S. Facchin, P.D. Townsend, G. Torfs, X. Yin, J. Bauwelinck, "Electronic ICs for Silicon Photonic Transceivers," *2018 IEEE 15th International Conference on Group IV Photonics (GFP)*, August 2018.

[4] B. Razavi, "Design of Integrated Circuits for Optical Communications", Hoboken, NJ, USA: Wiley, 2012.

[5] A. H. Ahmed, A. Moznine, D. Lim, Y. Ma, A. Rylyakov, S. Shekhar, "A Dual-Polarization Silicon-Photonic Coherent Transmitter Supporting 552 Gb/s/wavelength," *IEEE Journal of Solid-State Circuits,* September 2020.

[6] K. Kikuchi, "Fundamentals of Coherent Optical Fiber Communications," *Journal of Lightwave Technology*, vol. 34, no. 1, January 2016.

[7] R.A. Griffin, A.C. Carter, "OPtical differential quadrature phase-shift key (oDQPSK) for high capacity optical transmission," *Optical Fiber Communication and Exhibit*, 2002.

[8] S. Shimotsu, S. Oikawa, T. Saitou, N. Mitsugi, K. Kubodera, T. Kawanishi, and M. Izutsu, "Single Side-Band Modulation Performance of $LiNbO_3$ Integrated Modulator Consisting of Four-Phase Modulator Waveguides," *IEEE Photonics Technology Letters*, vol. 13, April 2001.

[9] D.S. Ly-Gagnon, S. Tsukamoto, K. Katoh, K. Kikuchi, "Coherent Detection of Optical Quadrature Phase-Shift Keying Signals With Carrier Phase Estimation," *Journal of Lightwave Technology*, vol. 24, January 2006.

[10] S. Tsukamoto, K. Katoh, K. Kikuchi, "Coherent Demodulation of Optical Multilevel Phase-Shift-Keying Signals Using Homodyne Detection and Digital Signal Processing," *IEEE Photonics Technology Letters*, vol. 18, May 2006.

[11] C. E. Shannon, "A mathematical theory of communication," *Bell Sys. Tech. J.*, vol. 27, June 2015.

[12] N. Pavarelli, J.S. Lee, M. Rensing, C. Eason, P.A. O'Brien, "Optical and Electronic Packaging Process for Silicon Photonic Systems," *The European Conference on Optical Communication (ECOC)*, September 2014.

[13] Navid Hosseinzadeh, K. Fang, L. Valenzuela, C. Schow, J. F. Buckwalter, "A 50-Gb/s Optical Transmitter Based on Co-design of 45-nm CMOS SOI Distributed Driver and 90-nm Silicon Photonic Mach-Zehnder Modulator" *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, August 2020.

[14] S. Nakano, M. Nagatani, M. Nogawa, Y. Kawamura, K. Kikuchi, K. Tsuzuki, H. Nosaka, "A 2.24-mW/Gb/s 80-Gb/s-PAM4 linear driver with a single supply using stacked current-mode architecture in 65-nm CMOS" *2017 Symposium on VLSI Circuits*, June 2017.

[15] G. Pini, D. Manstretta, R. Castello, "Analysis and Design of a 20-MHz Bandwidth, 50.5-dBm OOB-IIP3, and 5.4-mW TIA for SAW-Less Receivers," *IEEE Journal of Solid-State Circuits*, vol. 53, May 2018.

[16] C. Liao, S. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broaband Data Receivers in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, February 2008.

[17] S. Galal, B. Razavi, "40 Gb/s Amplifier and ESD Protection Circuit in 0.18 μm CMOS technology," *IEEE International Solid-State Circuit Conference*, February 2004.

[18] G. Palumbo, S. Pennisi, "Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain," *ICECS 2001. 8th IEEE International Conference on Electronics Circuits and Systems,* September 2001.

[19] T. Jyo, M. Nagatani, J. Ozaki, M. Ishikawa, H. Nosaka, "A 48 GHz BW 225 mW/ch Linear Driver IC with Stacked Current-Reuse Architecture in 65nm CMOS for Beyond-400 Gb/s Coherent Optical Transmitters," *2020 IEEE International Solid-State Circuits Conference* February 2020.

[20] Abdelrahman H. Ahmed, D. Lim, A. Elmoznine, Y. Ma "A 6V Swing 3.6% THD >40 GHz Driver with 4.5xBandwidth Extension for a 272 Gb/s Dual-Polarization 16-QAM Silicon Photonic Transmitter," *2019 IEEE International Solid-State Circuits Conference,* February 2020.

[21] A. Zandieh, P. Schvan, S. P. Voinigescu, "57.5 GHz Bandwidth 4.8 V_{pp} Swing Linear Modulator Driver for 64 GBaud m-PAM Systems," *in 2017 IEEE MTT-S International Microwave Symposium (IMS),* June 2017.

[22] H. Wakita, M. Nagatani, K. Kurishima, M. Ida, "An Over-67-GHz-Bandwidth 2 V_{ppd} Linear Differential Amplifier with Gain Control in 0.25-μm InP DHBT Technology," *n 2016 IEEE MTT-S International Microwave Symposium (IMS),* May 2016.